ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

**Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)**
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 270 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Hyung-Keun Lee, Mapo-gu, KOREA, REPUBLIC OF;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.
PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail or Fax
Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
(571) 273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FAX ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

SHERR & VAUGHN, PLLC
620 HERNDON PARKWAY
SUITE 320
HERNDON, VA 20170

APPLICATION NO. FILING DATE
12/648,845 12/30/2009

FIRST NAMED INVENTOR
Hyung Kuen Lee

ATTORNEY DOCKET NO. CONFIRMATION NO.
601-0310 4727

TITLE OF INVENTION: EEPROM DEVICE AND METHOD OF MANUFACTURING THE SAME

APPLN. TYPE
nonprovisional

SMALL ENTITY
NO

ISSUE FEE DUE $1740

PUBLICATION FEE DUE $300

REVISED ISSUE FEE $0

TOTAL FEE(S) DUE $2040

DATE DUE 08/15/2012

EXAMINER
SANDVIK, BENJAMIN P

ART UNIT
2826

CLASS/SUBCLASS
257-316000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.36(a)).

☐ Change of correspondence address or Change of Correspondence Address form PTO/SB/12(A) attached.

☐ Fee Address indication or "Fee Address" indication form PTO/SB/147, Rev 03/29/08 or more recent attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

☐ the names of up to 3 registered patent attorneys or agents OR, alternatively,

☐ the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

Sherr & Vaughn, PLLC

3. ASSIGNOR NAME AND RESIDENCE: DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recording as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNOR

Chong Hu HiTech Co., Ltd.

(B) RESIDENCE: (CITY AND STATE OR COUNTRY)

Seoul, Republic of Korea

Please check the appropriate assignee category or categories (will not be printed on the patent):

☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☐ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

☐ A check is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number ____________________________ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above):

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27(a).

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature

Date

Registered No.

Daniel H. Sherr

46,425

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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PTOL-85 (Rev. 02/11) Approved for use through 08/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
# Electronic Patent Application Fee Transmittal

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## Utility under 35 USC 111(a) Filing Fees

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# Electronic Acknowledgement Receipt

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<td>Hyung-Keun Lee</td>
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<td>Daniel Hilary Sherr/Christina Frye</td>
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## Payment information:

| **Submitted with Payment** | yes |
| **Payment Type** | Credit Card |
| **Payment was successfully received in RAM** | $2040 |
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| **Deposit Account** | |
| **Authorized User** | |

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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.
NOTICE OF ALLOWANCE AND FEE(S) DUE

60803  7590  05/15/2012
SHERR & VAUGHN, PLLC
620 HERNDON PARKWAY
SUITE 320
HERNDON, VA 20170

EXAMINER
SANDVIK, BENJAMIN P

ART UNIT  PAPER NUMBER
2826

DATE MAILED: 05/15/2012

APPLICATION NO.  FILING DATE  FIRST NAMED INVENTOR  ATTORNEY DOCKET NO.  CONFIRMATION NO.

TITLE OF INVENTION: EEPROM DEVICE AND METHOD OF MANUFACTURING THE SAME

APPLN. TYPE  SMALL ENTITY  ISSUE FEE DUE  PUBLICATION FEE DUE  PREV. PAID ISSUE FEE  TOTAL FEE(S) DUE  DATE DUE
nonprovisional  NO  $1740  $300  $0  $2040  08/15/2012

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Page 1 of 3

PTOL-85 (Rev. 02/11)
PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

or Fax
(P51)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60803
7590
05/15/2012
SHERR & VAUGHN, PLLC
620 HERndon PARKWAY
SUITE 320
HERndon, VA 20170

Note: A certificate of mailing may only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571)-273-2885, on the date indicated below.

| Depositor's Name |
| Signature |
| Date |

APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|----------------|-------------|----------------------|---------------------|------------------|

TITLE OF INVENTION: EEPROM DEVICE AND METHOD OF MANUFACTURING THE SAME

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1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.353).
   - [ ] Change of correspondence address (or Change of Correspondence Address form PTOSB/122) attached.
   - [ ] "Fee Address" indication (or "Fee Address" Indication form PTOSB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
   (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
   (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)
   PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.
   (A) NAME OF ASSIGNEE
   (B) RESIDENCE: (CITY and STATE OR COUNTRY)

   [ ] Individual
   [ ] Corporation or other private group entity
   [ ] Government

Please check the appropriate assignee category or categories (will not be printed on the patent):

4. The following fee(s) are submitted:
   - [ ] Issue Fee
   - [ ] Publication Fee (No small entity discount permitted)
   - [ ] Advance Order - # of Copies
   - [ ] A check is enclosed.
   - [ ] Payment by credit card. Form PTO-2038 is attached.
   - The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number ______________ (enclose a copy of this form).

5. Change in Entity Status (from status indicated above)
   - [a.] Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
   - [b.] Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature

Date

Typed or printed name

Registration No.

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PTOL-85 (Rev. 02/11) Approved for use through 08/31/2013.

OMB 0651-0033

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 270 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 270 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.
Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.
Notice of Allowability

--- The MAILING DATE of this communication appears on the cover sheet with the correspondence address---

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 4/19/2012.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____. The restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-9.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All   b) ☐ Some*   c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____.
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE MAILING DATE of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftperson’s Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner’s Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner’s comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner’s Comment Regarding Requirement for Deposit of Biological Material
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____
7. ☐ Examiner’s Amendment/Comment
8. ☒ Examiner’s Statement of Reasons for Allowance
9. ☐ Other _____.
DETAILED ACTION

Response to Arguments

Applicant's arguments, filed 4/19/2012, with respect to the references used to reject claim 1 have been fully considered and are persuasive. The rejection of claim 1 has been withdrawn.

Election/Restrictions

This application is in condition for allowance except for the presence of claims 10-20 directed to a method invention that was non-elected without traverse.

Accordingly, claims 10-20 have been cancelled.

Allowable Subject Matter

Claims 1-9 are allowed.

The following is an examiner's statement of reasons for allowance: the best prior art of record does not teach or fairly suggest a device having conductive wells corresponding to tunneling region, read transistor, and control gate, wherein a gate oxide layer is formed to have a relatively smaller thickness at the control gate than at the tunneling region.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”
**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BENJAMIN SANDVIK whose telephone number is (571)272-8446. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Davienne Monbleau can be reached on 571-272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ben P Sandvik/
Primary Examiner, Art Unit 2826
**Notice of References Cited**

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**NON-PATENT DOCUMENTS**

Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages

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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).) Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.*
BIB DATA SHEET

** CONTINUING DATA ********************

** FOREIGN APPLICATIONS ***********************
REPUBLIC OF KOREA 10-2008-0137592 12/30/2008

** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **
01/26/2010

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APPLICANTS
Hyung-Keun Lee, Mapo-gu, KOREA, REPUBLIC OF;

ADDRESS
SHERR & VAUGHN, PLLC
620 HERNDON PARKWAY
SUITE 320
HERNDON, VA 20170
UNITED STATES

FILER: Authority has been given in Paper
No.__________ to charge/credit DEPOSIT ACCOUNT
No.__________ for following:

- All Fees
- 1.16 Fees (Filing)
- 1.17 Fees (Processing Ext. of time)
- 1.18 Fees (Issue)
- Other
- Credit

BIB (Rev. 05/07)
## Issue Classification

**Application/Control No.:** 12648945

**Applicant(s)/Patent Under Reexamination:** LEE, HYUNG-KEUN

**Examiner:** BENJAMIN SANDVIK

**Art Unit:** 2826

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### Cross Reference(s)

- None

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Hyung-Keun Lee
Docket No.: 601-0310
Confirmation No.: 4727
Application No.: 12/648,945
Group Art Unit: 2826
Filed: December 29, 2009
Examiner: Benjamin P. SANDVIK

For: EEPROM DEVICE AND METHOD OF MANUFACTURING THE SAME

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. BOX 1450
Alexandria, VA 22313-1450

REPLY AND AMENDMENT UNDER 37 C.F.R. § 1.111

Sir:

In response to the Non-Final Office Action mailed February 6, 2012, Applicants respectfully request reconsideration of the application in view of the following Amendments and Remarks.

Applicants believe that no extensions of time are required at this time. However, if extensions of time are necessary to prevent abandonment of this application, such extensions of time are hereby petitioned for under 37 C.F.R. §1.136(a).

Amendments to the Claims are reflected in the listing of claims which begins on page 2.

Remarks begin on page 6.
REMARKS

By the amendment set forth supra, claim 2 and 13 are amended. Accordingly, claims 1-20 are currently pending in the above-referenced patent application. Applicants respectfully contend that no issue of new matter is presented by this amendment.

In the Non-Final Office Action: Claim 2 was rejected under 35 U.S.C. §112, second paragraph, as purportedly being indefinite. Claims 1 and 2 were rejected under 35 U.S.C. §103(a) as purportedly unpatentable over U.S. Patent No. 6,788,574 to Han et al. ("Han '574") in view of U.S. Patent Application Publication No. 2007/0152262 to Han ("Han '262"). Claim 3 was rejected under 35 U.S.C. §103(a) as purportedly unpatentable over Han '574 and Han '262 in view of U.S. Patent No. 6,953,974 to Rathfelder et al. ("Rathfelder"). Claims 4, 5, and 7-9 were rejected under 35 U.S.C. §103(a) as purportedly unpatentable over Han '574 and Han '262 in view of U.S. Patent No. 6,841,447 to Logie et al. ("Logie"). Claims 4 and 6 were rejected under 35 U.S.C. §103(a) as purportedly unpatentable over Han '574 and Han '262 in view of U.S. Patent Application Publication No. 2006/0017094 to Kim et al. ("Kim").

In reply to the rejection of claim 2 under 35 U.S.C. §112, second paragraph, as purportedly indefinite Applicant respectfully requests reconsideration. Applicants have amended claim 2 (and similar recitation in withdrawn claim 13) to overcome this rejection. Specifically, claims 2 and 13 have been amended non-substantively to include structure. Accordingly, the Applicants respectfully request withdrawal of this rejection.
In reply to the rejection of claims 1 and 2 under 35 U.S.C. §103(a) as purportedly unpatentable over Han '574 in view of Han '262, the Applicant respectfully requests reconsideration. Claims 1 and 2 recite "a gate oxide layer that is formed to have a relatively smaller thickness at the control gate than at the tunneling region".

Han '574 relates to an electrically-alterable non-volatile memory cell, as specified in the title. As admitted on page 3 of the Office Action, Han '574 "does not teach that the gate oxide layer that is formed to have a relatively smaller thickness at the control gate than the tunneling region.

Han '262 relates to a non-volatile memory device, as specified in the title. The Office Action purport on page 3 that Han '262 "teaches a non-volatile memory wherein the control capacitor has a gate oxide that has a smaller thickness than the transistor". However, Han '262 does not teach or suggest the clear claim recitation that "a gate oxide layer .... [has] a relatively smaller thickness at the control gate than at the tunneling region". In fact, there is absolutely no disclosure in Han '262 of a tunneling region or an equivalent structure. Although the Office Action purported various statements regarding how the deficiencies of both Han '574 and Han '262 would be obvious to one of ordinary skill in the art, these statements do not accomodate for the fact that neither Han '574 and Han '262 teach or suggest the claim recitation of "a gate oxide layer .... [has] a relatively smaller thickness at the control gate than at the tunneling region".
At least for these reasons, a prima facie case of obviousness has not been established under 35 U.S.C. 103(a). Accordingly, the Applicants respectfully request withdrawal of the rejection of claims 1 and 2 under 35 U.S.C. 103(a).

In reply to the rejection of claim 3 under 35 U.S.C. §103(a) as purportedly unpatentable over Han '574 and Han '262, in view of Rathfelder, the Applicant respectfully requests reconsideration. Claim 3 recites "a gate oxide layer that is formed to have a relatively smaller thickness at the control gate than at the tunneling region", which is the same recitation discussed above for claims 1 and 2. As discussed above, neither Han '574 and Han '262 teach or suggest this claim recitation. Rathfelder relates to an EEPROM device and method for providing lower program voltage, as specified in the title. However, Rathfelder does not alleviate the above noted deficiencies of Han '574 and Han '262. Further, the Office Action does not purport that Rathfelder alleviates the deficiencies of Han '574 and Han '262. At least for these reasons, a prima facie case of obviousness has not been established under 35 U.S.C. 103(a) and the Applicants respectfully request withdrawal of the rejection of claim 3 under 35 U.S.C. 103(a).

In reply to the rejection of claims 4, 5, and 7-9 under 35 U.S.C. §103(a) as purportedly unpatentable over Han and '262, in view of Logie, the Applicant respectfully requests reconsideration. Claims 4, 5, and 7-9 recites "a gate oxide layer that is formed to have a relatively smaller thickness at the control gate than at the tunneling region", which is the same recitation discussed above for claims 1 and 2. As
discussed above, neither Han '574 and Han '262 teach or suggest this claim recitation. Logie relates to an EEPROM device having an isolation-bounded tunnel capacitor and fabrication process, as specified in the title. However, Logie does not alleviate the above noted deficiencies of Han '574 and Han '262. Further, the Office Action does not purport that Logie alleviates the deficiencies of Han '574 and Han '262. At least for these reasons, a prima facie case of obviousness has not been established under 35 U.S.C. 103(a) and the Applicants respectfully request withdrawal of the rejection of claims 4, 5, and 7-9 under 35 U.S.C. 103(a).

In reply to the rejection of claims 4 and 6 under 35 U.S.C. §103(a) as purportedly unpatentable over Han and '262, in view of Kim, the Applicant respectfully requests reconsideration. Claims 4 and recites "a gate oxide layer that is formed to have a relatively smaller thickness at the control gate than at the tunneling region", which is the same recitation discussed above for claims 1 and 2. As discussed above, neither Han '574 and Han '262 teach or suggest this claim recitation. Kim relates to a non-volatile memory devices with improved insulation layers and methods of manufacturing such devices, as specified in the title. However, Kim does not alleviate the above noted deficiencies of Han '574 and Han '262. Further, the Office Action does not purport that Kim alleviates the deficiencies of Han '574 and Han '262. At least for these reasons, a prima facie case of obviousness has not been established under 35 U.S.C. 103(a) and the Applicants respectfully request withdrawal of the rejection of claims 4 and 6 under 35 U.S.C. 103(a).
CONCLUSION

Applicants believe that a full and complete response has been made to the Office Action and respectfully submit that all of the stated objections and grounds for rejection have been overcome or rendered moot. Accordingly, Applicants respectfully submit that all pending claims are allowable and that the application is in condition for allowance.

Should the Examiner feel that there are any issues outstanding after consideration of this response; the Examiner is invited to contact the Applicant’s undersigned representative at the number below to expedite prosecution.

Prompt and favorable consideration of this Reply is respectfully requested.

Respectfully Submitted,

[Signature]

Daniel H. Sherr
Reg. No. 46,425

SHERR & VAUGHN, PLLC
620 Herndon Parkway
Suite 320
Herndon, Virginia 20170
Tel: 571-313-7556
Fax: 703-935-8473
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.
## PATENT APPLICATION FEE DETERMINATION RECORD

**For:** Substitute for Form PTO-875

### APPLICATION AS FILED – PART I

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**Application Size Fee (37 CFR 1.16(e))**

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(e).

### APPLICATION AS AMENDED – PART II

**04/19/2012**

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**First Presentation of Multiple Dependent Claim (37 CFR 1.16(g))**

Legal Instrument Examiner: **KIMBERLY PANNELL**

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*This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.*

*If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.*
AMENDMENTS TO THE CLAIMS

Please AMEND claims 2 and 13 as follows.

The following is a complete list of all claims in this application.

1. (Original) A device, comprising:
   a field oxide layer that defines an active region and a field region of a semiconductor substrate;
   conductive wells that respectively correspond to a tunneling region, a read transistor, and a control gate, under the active region of an upper surface of the semiconductor substrate;
   a gate oxide layer that is formed to have a relatively smaller thickness at the control gate than at the tunneling region, on the upper surface of the semiconductor substrate divided by the field oxide layer; and
   a polysilicon layer that is formed over the field oxide layer and the gate oxide layer from the tunneling region to the control gate.

2. (Currently Amended) The device of claim 1, wherein as the thickness of the control gate is minimized allowing reduces, the gate oxide layer to minimize reduces the area of the control gate.

3. (Original) The device of claim 1, wherein the conductive wells respectively
corresponding to the tunneling region and the control gate are first conductive types, and the conductive well corresponding to the read transistor is a second conductive type.

4. (Original) The device of claim 1, further comprising an interlayer dielectric layer formed over the polysilicon layer.

5. (Original) The device of claim 4, wherein the interlayer dielectric layer comprises tetra ethyl ortho silicate.

6. (Original) The device of claim 4, wherein the interlayer dielectric layer comprises undoped silicate glass.

7. (Original) The device of claim 4, wherein the interlayer dielectric layer comprises boron phosphorus silicate glass.

8. (Original) The device of claim 4, wherein the interlayer dielectric layer comprises phosphorus silicate glass.

9. (Original) The device of claim 4, wherein a top surface of the interlayer dielectric layer is planarized.

10. (Withdrawn) A method comprising:
forming conductive wells respectively corresponding to a tunneling region, a read transistor, and a control gate between field oxide layers formed on a semiconductor substrate;

forming a gate oxide layer over the conductive wells;

removing the gate oxide layer at a predetermined thickness from the control gate;

and

forming a polysilicon layer over the field oxide layer and the gate oxide layer.

11. (Withdrawn) The method of claim 10, wherein the removing of gate oxide layer from the control gate is performed by a deglaze process.

12. (Withdrawn) The method of claim 11, wherein the deglaze process is performed by using a photoresist pattern selectively exposing the gate oxide layer corresponding to the control gate.

13. (Currently Amended) The method of claim 10, wherein as the thickness of the control gate decreases, is minimized allowing the gate oxide layer to minimize reduces the area of the control gate.

14. (Withdrawn) The method of claim 10, comprising:

forming an interlayer dielectric layer over the polysilicon layer.

15. (Withdrawn) The method of claim 14, wherein the interlayer dielectric layer
comprises tetra ethyl ortho silicate.

16. (Withdrawn) The method of claim 14, wherein the interlayer dielectric layer comprises undoped silicate glass.

17. (Withdrawn) The method of claim 14, wherein the interlayer dielectric layer comprises boron phosphorus silicate glass.

18. (Withdrawn) The method of claim 14, wherein the interlayer dielectric layer comprises phosphorus silicate glass.

19. (Withdrawn) The method of claim 14, wherein forming the interlayer dielectric layer over the polysilicon layer includes chemical vapor deposition.

20. (Withdrawn) The method of claim 14, comprising:

planarizing an upper portion of the interlayer dielectric layer over the polysilicon layer.
Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.
Office Action Summary

Application No. 12/648,945
Applicant(s) LEE, HYUNG-KEUN

Examiner BENJAMIN SANDVIK
Art Unit 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on 12/23/2011.
2a)☐ This action is FINAL.
2b)☒ This action is non-final.
3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) 1-20 is/are pending in the application.
   5a) Of the above claim(s) 1-20 is/are withdrawn from consideration.
6)☐ Claim(s) _____ is/are allowed.
7)☒ Claim(s) 1-9 is/are rejected.
8)☐ Claim(s) _____ is/are objected to.
9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.
11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a)☒ All  b)☐ Some * c)☐ None of:
   1. ☒ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____.
   3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson’s Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO/SB/08)
4)☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date _____.
5)☐ Notice of Informal Patent Application
6)☐ Other: _____.
DETAILED ACTION

Claim Rejections - 35 USC § 112

Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Because the claim is statutorily in the device category, the claim limitations that manipulate or adjust the thickness/area of the control gate do not further define the structure; hence it is unclear as to what structure is being claimed as the device. Furthermore, it is unclear as to how a gate oxide layer “reduces the area of the control gate”.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Han et al (U.S. Patent #6788574), in view of Han (U.S. PG Pub #2007/0152262), hereinafter referred to as ‘262.

With respect to claim 1, Han teaches a field oxide layer (Fig. 7, STI regions that defines an active region and a field region of a semiconductor substrate; conductive wells that respectively correspond to a tunneling region (Fig. 7, 734b), a read transistor (Fig. 7, 734a), and a control gate (Fig. 7, 734c),
under the active region of an upper surface of the semiconductor substrate; a
gate oxide layer (labeled in Fig. 2 as 228) that is formed at each of the control
gate and the tunneling region, on the upper surface of the semiconductor
substrate divided by the field oxide layer; and a polysilicon layer (see Fig. 3, the
gates are formed by an integral polysilicon layer 308/320/326) that is formed over
the field oxide layer and the gate oxide layer from the tunneling region to the
control gate; but does not teach that the gate oxide layer that is formed to have a
relatively smaller thickness at the control gate than at the tunneling region. ‘262
teaches a non-volatile memory wherein the control capacitor has a gate oxide
that has a smaller thickness than the transistor (Fig. 5 and Paragraph 31). It
would have been obvious to one of ordinary skill in the art at the time the
invention was made to form the dielectric layer of the control capacitor of Han to
have a smaller thickness than the tunneling and read transistors as taught by
‘262 in order to allow for tunneling operation in the capacitor device portion
(Paragraph 39), and the shape of the oxide will prevent damage during formation
of the electrode (Paragraph 32)

With respect to claim 2, because the claim appears to be drawn to
modifying the structure, note that a "product by process" claim is directed to the
product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17
(footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523;
In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In
re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289
(CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear. As to the grounds of rejection under section 103, see MPEP § 2113

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Han and '262, in view of Rathfelder et al (U.S. Patent #6953974).

With respect to claim 3, Han teaches that the conductive wells respectively corresponding to the tunneling region and the control gate are first conductive types, but does not teach that the conductive well corresponding to the read transistor is a second conductive type. However, Han alternatively teaches that the read transistor can be formed in a P-substrate, but not that a well is provided for the read transistor. Rathfelder teaches that each of the tunneling region, control region, and read transistor region have a well, and wherein the read transistor has an opposite type well. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a P-well, opposite type to the tunnel and control region, for the read transistor of Han in order to achieve the predictable result of creating an NFET device.
Claims 4, 5, and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Han and ‘262, in view of Logie et al (U.S. Patent #6841447).

With respect to **claims 4, 5, and 7-9**, Han does not teach an interlayer dielectric layer formed over the polysilicon layer. Logie teaches a single-poly non-volatile device having an interlayer insulating layer (Fig. 1) formed over the transistors/polysilicon, wherein the interlayer insulating layer comprises TEOS, BPSG, PSG as a material (Col 4 Ln 33-40), and is a planarized layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a planarized interlayer insulating layer using any of the materials taught by Logie in order to insulate the devices below and to provide a surface for wiring conductor layers for making connections to the devices.

Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Han and ‘262, in view of Kim et al (U.S. PG Pub #2006/0017094).

With respect to **claims 4 and 6**, Han does not teach an interlayer dielectric layer formed over the polysilicon layer that comprises undoped silicate glass. Kim teaches a transistor device that is provided with an overlying interlayer dielectric layer, wherein the dielectric layer comprises undoped silicate glass (Paragraphs 21 and 49). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a planarized interlayer insulating layer using any of the materials taught by Kim in order to insulate the
devices below and to provide a surface for wiring conductor layers for making connections to the devices.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BENJAMIN SANDVIK whose telephone number is (571)272-8446. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Davienne Monbleau can be reached on 571-272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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### EAST Search History

#### EAST Search History (Prior Art)

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Hyung-Keun Lee
Docket No.: 601-0310

Application No.: 12/648,945
Confirmation No.: 4727

Filed: December 29, 2009
Group Art Unit: 2826

Examiner: Benjamin P. SANDVIK

For: EEPROM DEVICE AND METHOD OF MANUFACTURING THE SAME

Commissioner for Patents
P.O. BOX 1450
Alexandria, VA 22313-1450

REPLY TO RESTRICTION REQUIREMENT

Sir:

In response to the Restriction Requirement mailed November 25, 2011, Applicant elects Group I (Claims 1-9), without traverse.

It is not believed that any extensions of time or fees are required. If extensions of time are necessary to prevent abandonment of this application, such extensions of time are hereby petitioned for under 37 C.F.R. §1.136(a).

Respectfully Submitted,

[Signature]

Daniel H. Sherr
Reg. No. 46,425

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# Electronic Acknowledgement Receipt

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<td>First Named Inventor/Applicant Name:</td>
<td>Hyung-Keun Lee</td>
</tr>
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## Payment Information:

| Submitted with Payment | no |

## File Listing:

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## Warnings:

## Information:
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.
Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.
**Office Action Summary**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.  Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.  Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) □ Responsive to communication(s) filed on _____.
2a) □ This action is FINAL.  
2b) ☑ This action is non-final.
3) □ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
4) □ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

5) ☑ Claim(s) 1-20 are pending in the application.
   5a) Of the above claim(s) _____ is/are withdrawn from consideration.
6) □ Claim(s) _____ is/are allowed.
7) □ Claim(s) _____ is/are rejected.
8) □ Claim(s) _____ is/are objected to.
9) ☑ Claim(s) 1-20 are subject to restriction and/or election requirement.

**Application Papers**

10) □ The specification is objected to by the Examiner.
11) □ The drawing(s) filed on _____ is/are: a) □ accepted or b) □ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
12) □ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

13) □ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☑ All  
   b) ☑ Some *  
   c) □ None of:
      1. □ Certified copies of the priority documents have been received.
      2. □ Certified copies of the priority documents have been received in Application No. _____.
      3. □ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) □ Notice of References Cited (PTO-892)
2) □ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) □ Information Disclosure Statement(s) (PTO/SB/08)  
   Paper No(s)/Mail Date _____.
4) □ Interview Summary (PTO-413)  
   Paper No(s)/Mail Date _____.
5) □ Notice of Informal Patent Application  
6) □ Other: _____.
DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-9, drawn to a device, classified in class 257, subclass 316.

II. Claims 10-20, drawn to a method, classified in class 438, subclass 592.

The inventions are distinct, each from the other because of the following reasons:

Inventions 1 and 2 are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product can be made by a different method from that of claims 10-20; such as by growing the oxide between the field oxide layers in place of the steps of forming the oxide layer and subsequently removing portions of a predetermined thickness.

Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and/or examination burden if restriction were not required because at least the following reason(s) above apply.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a invention to be examined even though the requirement
may be traversed (37 CFR 1.143) and (ii) identification of the claims encompassing the elected invention.

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

The examiner has required restriction between product and process claims. Where applicant elects claims directed to the product, and the product claims are subsequently found allowable, withdrawn process claims that depend from or otherwise require all the limitations of the allowable product claim will be considered for rejoinder.
All claims directed to a nonelected process invention must require all the limitations of an allowable product claim for that process invention to be rejoined.

In the event of rejoinder, the requirement for restriction between the product claims and the rejoined process claims will be withdrawn, and the rejoined process claims will be fully examined for patentability in accordance with 37 CFR 1.104. Thus, to be allowable, the rejoined claims must meet all criteria for patentability including the requirements of 35 U.S.C. 101, 102, 103 and 112. Until all claims to the elected product are found allowable, an otherwise proper restriction requirement between product claims and process claims may be maintained. Withdrawn process claims that are not commensurate in scope with an allowable product claim will not be rejoined. See MPEP § 821.04(b). Additionally, in order to retain the right to rejoinder in accordance with the above policy, applicant is advised that the process claims should be amended during prosecution to require the limitations of the product claims. Failure to do so may result in a loss of the right to rejoinder. Further, note that the prohibition against double patenting rejections of 35 U.S.C. 121 does not apply where the restriction requirement is withdrawn by the examiner before the patent issues. See MPEP § 804.01.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BENJAMIN SANDVIK whose telephone number is (571)272-8446. The examiner can normally be reached on Mon-Fri.
If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Davienne Monbleau can be reached on 571-272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ben P Sandvik/
Primary Examiner, Art Unit 2826
Title: EEPROM DEVICE AND METHOD OF MANUFACTURING THE SAME
publication No: US-2010-0163956-A1
Publication Date: 07/01/2010

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO’s publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO’s Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101
This is to certify that the following application annexed hereto
is a true copy from the records of the Korean Intellectual
Property Office

Application Number

Filling Date

Applicant(s)

2010년 02월 23일

COMMISSIONER
서지사항

서류명: 특허출원서
참조번호: 0065
출원구분: 특허출원
출원인:

명칭: 주식회사 동부하이텍

대리인:

성명: 장성구
대리인코드: 9-1998-000514-8
포괄위임등록번호: 2007-041062-6

대리인:

성명: 김원준
대리인코드: 9-1998-000104-8
포괄위임등록번호: 2007-041061-9

발명의 국문명칭: 아이피롭 소자 및 그 제조 방법
영문명칭: EEPROM DEVICE AND ITS FABRICATION METHOD

발명자:

성명: 이형근
영문표기: LEE, HYUNG KEUN
주민등록번호: 791209-1XXXXXX
우편번호: 121-872
제출 일자 : 2008-12-30

【주소】 서울특별시 마포구 염리동 128-65 202호

【국적】 KR

위와 같이 특허청장에게 제출합니다.

대리인
장성구 (인)

대리인
김원준 (인)

【수수료】

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[요약사]

[요약]

본 발명은 이이피름(EEPROM) 소자를 제조하는 기법에 관한 것으로, 이를 위하여 본 발명은 터널형 영역과 컨트롤 게이트에서의 게이트 산화막의 두께가 동일하게 형성되는 환경 방법과는 달리, 컨트롤 게이트가 형성되는 영역의 게이트 산화막의 두께를 기 설정된 두께만큼 제거하여 터널링 영역의 게이트 산화막보다 상대적으로 얇은 두께를 갖는 이이피름 소자를 제조함으로써 컨트롤 게이트의 면적을 축소시켜 이이피름 소자의 집적도를 향상시킬 수 있는 것이다.

[대표도]

도 5

[설명서]

이이피름 (EEPROM : electrically erasable programmable read-only memory)에
소자
설명서

발명의 명칭

이어폰 소자 및 그 제조 방법(EEPROM DEVICE AND ITS FABRICATION METHOD)

발명의 상세한 설명

기술분야

본 발명은 이어폰(EEPROM : electrically erasable programmable read-only memory) 소자를 제조하는 기법에 관한 것으로, 더욱 상세하게는 이어폰 소자의 콘트롤 게이트의 얇음을 감소시키고 소자의 집적도를 증가시키는데 적합한 이어폰 소자 및 그 제조 방법에 관한 것이다.

배경기술

잘 알려진 바와 같이, 플래시 메모리는 전원이 중단되어도 저장된 데이터가 손실되지 않는 장점을 가지고 있어 PC Biao용, Set-top Box, 프린터 및 네트워크 서버 등의 데이터 저장용으로 많이 사용되고 있으며 그 후에는 디지털 카메라와 휴대폰 등에서도 많이 이용되고 있는 실정이다.

이러한 플래시 메모리 중에서도 전기적으로 메모리 셀의 데이터를 일괄적으로 또는 셀 단위로 소거하는 기능을 가지고 있는 이어폰(EEPROM)형 플래시 메모리 장치는 프로그램 시에는 드레인 측에 채널 열 전자(channel hot electron)를 형성시켜 전자를 플로팅 게이트(floating gate)에 충적함으로써 셀 트랜지스터의
문턱 전압을 증가시키는 반면에, 소거 시에는 소오스/기판과 플로팅 케이트간에 고전압을 발생시켜 플로팅 케이트에 촉각된 전자를 방출함으로써 셀 트랜지스터의 문턱 전압을 낮춘다.

이러한 종래의 이이퍼플 오자는 제조기술에 따라, 폴리 실리콘층의 사용 수에 따라 싱글 폴리 이이퍼플(single poly EEPROM)과, 더불 폴리 이이퍼플(double poly EEPROM) 등으로 구분된다.

도 1은 종래의 싱글 폴리 이이퍼플을 나타낸 도면이고, 도 2는 종래의 싱글 폴리 이이퍼플의 단면도로서, 싱글 폴리 이이퍼플은 크게 터널링 영역(tunneling region, A), 리드 트랜지스터(read transistor, B), 컨트롤 게이트(control gate, C) 등으로 구성되고, 이이퍼플이 프로그래밍 및 소거(programming & erase) 등의 수행하기 위해서는 터널링 영역(A)과 컨트롤 게이트(C) 사이에 큰 값의 정전 용량 비율(capacitance ratio)이 요구되며, 이러한 정전 용량의 차이는 각각 터널링 영역(A)에 따른 전압을, 컨트롤 게이트(C)에는 적은 전압을 인가하여야 한다.

이러한 정전 용량의 차이를 만들기 위해 터널링 영역(A)과 컨트롤 게이트(C) 위에 폴리 실리콘층(Poly), 오버랩(overlab, □)되는 면적이 차이가 나게 제조해야 하는데, 이와 같은 방식은 상대적으로 큰 면적을 가져야 하는 컨트롤 게이트(C)가 반도체 기판 상에 상대적으로 큰 면적을 차지하게 함으로써 결국 싱글 폴리 이이퍼플의 집적도 저하를 초래한다.

도 3은 종래의 싱글 폴리 이이퍼플의 회로도를 간략하게 나타낸 도면으로, 싱글 폴리 이이퍼플은 터널링 영역(A)과 컨트롤 게이트(C)에서의 폴리 실리콘층
(Poly)과 응티브 영역(Active)의 오버랩 면적을 다르게 하여 두 지역에서의 경전
용량을 다르게 한다는 것인데, 직렬로 연결된 두 개의 커패시터(capacitor, C1,
C2)는 커패시터의 면적 A1, A2가 달라지면서 경전 용량 C1, C2가 달라지게 되며,
프로그램 및 소거를 위한 외부 바이어스 전압(Bias Vc)은 두 개의 커패시터(C1,
C2)에서 각각의 경전 용량에 반비례하는 비율로 나뉘어 인가되고, 이는 경전 용량
이 작은(즉, 면적이 작은) C1이 C2보다 높은 전압(voltage)이 인가되어 터널링이
발생하게 된다. 즉, 두 개의 커패시터(C1, C2)는 C1= ε (A1/d), C2= ε (A2/d),
C1/C2=A1/A2=V2/V1 등의 관계를 갖는다.

여기에서, 상급 폴리 이이피름의 구조에서는 오버랩되는 면적 차이의 비율이
있어야 한 쪽에서 터널링이 일어나고, 다른 한쪽은 터널링이 일어나지 않게
되므로, 결국 터널링이 일어나면 안되는 지역인 컨트롤 게이트(C)는 상당한 면적을
필연적으로 가져야하는데, 실제로 터널링 영역(A)과 컨트롤 게이트(C) 지역에서
오버랩되는 폴리 실리콘층(Poly)의 면적(즉, a, c)은 수심 배의 차이가 있어야 하
므로, 컨트롤 게이트(C)의 면적이 상급 폴리 이이피름 면적의 상당 비율을 차지하
며 상급 폴리 이이피름의 접적으로 좋지 않게 만드는 요인이 된다.

【발명의 내용】

【해결하고자 하는 과제】

따라서, 상술한 바와 같은 상급 폴리 이이피름의 경우 프로그램 및 소거 등
작을 위해 터널링 영역(A)과 컨트롤 게이트(C) 상부에 형성되는 폴리 실리콘층(Poly)의 면적차이가 나게 제조해야 함으로써, 컨트롤 게이트(C)가 반도체 기판상에 상대적으로 큰 면적을 차지하게 되어 이로울 소자의 집적도를 저하시키는 요인으로 작용하고 있다.

이에 따라, 본 발명은 컨트롤 게이트가 형성되는 영역의 게이트 산화막의 두께를 조절하여 컨트롤 게이트의 면적을 감소시킴으로써, 이로울 소자의 집적도를 항상시킬 수 있는 이로울 소자 및 그 제조 방법을 제공하고자 한다.

【과제 해결 수단】

일반적으로 본 발명은, 반도체 기판의 활성 영역과 필드 영역을 정의하는 필드 산화막과, 상기 활성 영역에 대한 상기 반도체 기판의 상부 표면 아래에 터널링 영역, 리드 트랜지스터 및 컨트롤 게이트에 각각 대응하여 형성된 도전형 원과, 상기 필드 산화막으로 구분된 상기 반도체 기판의 상부 표면에 상기 터널링 영역보다 상기 컨트롤 게이트에서 상대적으로 더 얇은 두께를 갖도록 형성된 게이트 산화막과, 상기 터널링 영역에서 상기 컨트롤 게이트까지의 상기 필드 산화막 및 게이트 산화막의 상부에 형성된 폴리 실리콘층을 포함하는 이로울 소자를 제공한다.

다른 관점에서 본 발명은, 반도체 소자에 형성된 필드 산화막의 사이에 터널링 영역, 리드 트랜지스터 및 컨트롤 게이트에 각각 대응하여 도전형 셀을 형성하는 단계와, 상기 형성된 도전형 셀의 상부에 게이트 산화막을 형성하는 단계와, 상
기 컨트롤 게이트에서의 상기 게이트 산화막을 기 설정된 두께만큼 제거하는 단계
와, 상기 필드 산화막 및 게이트 산화막의 상부에 줄리 실리콘층을 형성하는 단계
를 포함하는 이의됨 소자의 제조 방법 제공한다.

【효과】

본 발명은, 터널링 영역과 컨트롤 게이트에서의 게이트 산화막의 두께가 동
일하게 형성되는 중래 방법과는 달리, 반도체 소자에 형성된 필드 산화막의 사이에
터널링 영역, 리드 트랜지스터 및 컨트롤 게이트에 각각 대응하여 도전형 웨를 형
성하고, 형성된 도전형 웨의 상부에 게이트 산화막을 형성하며, 컨트롤 게이트에서
의 게이트 산화막을 기 설정된 두께만큼 제거한 후에, 필드 산화막 및 게이트 산화
막의 상부에 줄리 실리콘층을 형성함으로써, 컨트롤 게이트의 면적을 축소시켜 이
의이됨 소자의 접적도를 향상시킬 수 있다.

【발명의 실시를 위한 구체적인 내용】

본 발명은, 컨트롤 게이트가 형성되는 영역의 게이트 산화막의 두께를 기 설
정된 두께만큼 제거하여 터널링 영역의 게이트 산화막보다 상대적으로 얇은 두께를
갖는 이의이됨 소자를 제조함으로써, 컨트롤 게이트의 면적을 축소시켜 이의이됨
소자의 접적도를 향상시킨다는 것이며, 이러한 기술적 수단을 통해 중래 기술에서
의 문제점을 해결할 수 있다.

이하 접부된 도면을 참조하여 본 발명의 실시 예에 대하여 상세하게 설명한
나.

【실시예】

[0016] 도 4는 본 발명의 실시 예에 따른 성글 폴리 이이리품을 나타낸 도면이고, 도 5는 본 발명의 실시 예에 따른 성글 폴리 이이리품의 단면도이며, 도 6은 본 발
명의 실시 예에 따른 성글 폴리 이이리품의 회로도를 간략하게 도시한 도면이다.

[0017] 도 4 내지 도 6을 참조하면, 본 발명의 실시 예에 따른 이이리품 소자는, 반
도체 기판의 표면 아래에 터널링 영역(A'), 리드 트랜지스터(B') 및 컨트롤 갤트
(C')에 각각 대응하는 도전영의 월(Nwell, Pwell, Nwell)과, 활성 영역(Active)과
필드 영역(field area)을 정의하는 필드 산화막과, 상기 필드 산화막으로 구분된
반도체 기판의 상부 표면에 터널링 영역(A')보다 컨트롤 갤트(C')에서 상대적으
로 더 두꺼운 두께(5a>5b)를 갖도록 형성된 갤트 산화막과, 터널링 영역(A')에서
컨트롤 갤트(C')까지의 필드 산화막 및 갤트 산화막(즉, Ox)의 상부에 형성된
폴리 실리콘층(Poly)과, 폴리 실리콘층(Poly)이 형성된 반도체 기판의 상부에 형성
된 충전 절연막(PMD) 등을 포함할 수 있다.

[0018] 이와 같은 이이리품의 접적도를 높이기 위해 제안된 구조와 그 회로도에서
나타낸 본 발명의 성글 폴리 이이리품은 갤트 산화막(0x)의 두께가 동일한 중래
의 성글 폴리 이이리품과 달리 터널링 영역(A')의 갤트 산화막(0x)의 두께(5a)를
컨트롤 갤트(C')의 갤트 산화막(0x)의 두께(5b)보다 상대적으로 두껍게 형성함
으로써, 면적 및 두께에 따라 경전 용량을 조절하도록 할 수 있다. 즉, 컨트롤 게이트(C')에서의 게이트 산화막의 두께가 감소함에 따라 컨트롤 게이트(C')의 면적이 감소시킬 수 있다.

【수학식 1】

\[
\frac{C_1}{C_2} = \frac{A_{11}d_2}{A_{22}d_1} = \frac{V_2}{V_1}
\]

[0019]

상기 수학식 1과 같이 정전 용량이 면적 및 두께에 대한 함수로 바뀌어 게이트 산화막(0x)의 두께 비율만큼 정전 용량 비율이 변하게 되며, 이에 따라 컨트롤 게이트(C')의 게이트 산화막(0x)이 터널링 영역의 게이트 산화막(0x)보다 약간 줄어진 비율에 대응하여 컨트롤 게이트(C')의 면적이 감소할 수 있으며, 두 영역에 사용된 게이트 산화막(0x)의 두께를 조절함으로써, 아이피트 소자의 점적도를 향상시킬 수 있다.

[0021] 한편, 도 7a 내지 도 7d는 본 발명의 실시 예에 따라 반도체 포리 아이피트를 제조하는 과정을 나타낸 공정 순서도이다.

[0022] 도 7a 내지 도7d를 참조하면, 먼저, 반도체 기판(700) 상에 활성 영역 (active area)과 필드 영역(field area)을 정의하는 마스크에 따라 이온 주입 공정, 산화 공정 등을 통해 도 7a에 도시한 바와 같은 필드 산화막(702)을 형성한다. 여기에서, 활성 영역과 필드 영역을 분리하는 필드 산화막(702)이 균일하게 생성될 수 있도록 더미 산화막을 함께 형성할 수 있음은 물론이다.

[0023] 그리고, 도4에 도시한 바와 같은 터널링 영역(A'), 리드 트랜지스터(B') 및
컨트롤 케이트(C')에 대응하는 각각의 도전형 웰(704a, 704b, 704c)을 형성한 후에, 필드 산화막(702)에 따라 정의된 활성 영역의 반도체 기판(700)의 상부 표면에 도 7b에 도시한 바와 같이 케이트 산화막(706)을 형성한다. 여기에서, 터널링 영역(A')과 컨트롤 케이트(C')에 각각 대응하는 도전형 웰(704a, 704c)은 예를 들면, N형 웰을 형성할 수 있고, 리드 트렌지스터(B')에 대응하는 도전형 웰(704b)은 예를 들면, P형 웰을 형성할 수 있다.

다음에, 각각의 도전형 웰(704a, 704b, 704c)이 형성된 반도체 기판(700)의 상부에 컨트롤 케이트(C')에 대응하는 케이트 산화막 양극면을 오른쪽 포토레지스트 패턴(미드시됨)에 따라 예를 들면, 디글레이즈 공정(deglaze process) 등을 통해 도 7c에 도시한 바와 같이 기 설정된 두께만큼 제거한다. 여기에서, 기 설정된 두께는 이에 따른 소자에 대한 원하는 정전 용량 비율을 획득하기 위해 터널링 영역(A')과 대응하여 설정될 수 있다.

이어서, 포토레지스트 패턴을 소정의 에칭 공정에 따라 제거한 후에, 반도체 기판(700)의 상부에 터널링 영역(A')에서 컨트롤 케이트(C')까지 폴리 실리콘층(708)을 형성하고, 그 상부에 도 7d에 도시한 바와 같이 중간 결연막(PMD, 710)을 형성한다. 여기에서, 중간 결연막(710)은 예를 들면, 화학적 기상 증착법(CVD : chemical vapor deposition) 등을 이용하여 예를 들면, TEOS(tetra ethyl ortho silicate), USG(undoped silicate glass), BPSG(boron phosphorus silicate glass), PSG(phosphorus silicate glass) 등의 결연 물질을 증착한 후, 그 상부를 예를 들면, 화학적 기계적 평탄화 공정(CMP : chemical mechanical polishing) 등으로 평
따라서, 컨트롤 게이트가 형성되는 영역의 게이트 산화막의 두께를 기 설정한 두께만큼 제거하여 터널링 영역의 게이트 산화막보다 상대적으로 얇은 두께를 갖는 이어결합 소자를 제조함으로써, 컨트롤 게이트의 면적을 축소시켜 이어결합 소자의 집적도를 향상시킬 수 있다.

이상의 설명에서는 본 발명의 다양한 실시 예들을 제시하여 설명하였으나 본 발명이 반드시 이에 한정되는 것은 아니며, 본 발명이 숭하는 기술분야에서 통상의 지식을 가진 자라면 본 발명의 기술적 사상을 벗어나지 않는 범위 내에서 여러 가지 치환, 변형 및 변경이 가능함을 쉽게 알 수 있을 것이다.
【부록 첨부문구】

【참조항 1】
반도체 기판의 외형 영역과 필드 영역을 정의하는 필드 산화막과,

상기 외형 영역에 대한 상기 반도체 기판의 상부 표면 아래에 터널링 영역, 리드 트랜지스터 및 컨트롤 게이트에 각각 대응하여 형성된 도전형 웨이트.

상기 필드 산화막으로 구분된 상기 반도체 기판의 상부 표면에 상기 터널링 영역보다 상기 컨트롤 게이트에서 상대적으로 더 잡은 두께를 갖도록 형성된 게이트 산화막과,

상기 터널링 영역에서 상기 컨트롤 게이트까지의 상기 필드 산화막 및 게이트 산화막의 상부에 형성된 폴리 실리콘층

을 포함하는 이어폰 소자.

【참조항 2】
제 1 항에 있어서,

상기 게이트 산화막은, 상기 컨트롤 게이트에서의 두께가 감소함에 따라 상기 컨트롤 게이트의 면적을 감소시키는 이어폰 소자.

【참조항 3】
반도체 소자에 형성된 필드 산화막의 사이에 터널링 영역. 리드 트랜지스터.
및 컨트롤 제이트에 각각 대응하여 도전형 웨를 형성하는 단계와,

상기 형성된 도전형 웨의 상부에 제이트 산화막을 형성하는 단계와,

상기 컨트롤 제이트에서의 상기 제이트 산화막을 기 설정된 두께만큼 제거하는 단계와,

상기 웨드 산화막 및 제이트 산화막의 상부에 풍리 실리콘층을 형성하는 단계

를 포함하는 이영률 소자의 제조 방법.

【청구항 4】

제 3 항에 있어서,

상기 제거하는 단계는, 다클레이즈 공정을 통해 수행되는 이영률 소자의 제조 방법.

【청구항 5】

제 3 항 또는 제 4 항에 있어서,

상기 제이트 산화막은, 상기 컨트롤 제이트에서의 두께가 감소함에 따라 상기 컨트롤 제이트의 면적을 감소시키는 이영률 소자의 제조 방법.

【도면의 간단한 설명】

(0028) 도 1은 중래의 싱글 폴리 이영률을 나타낸 도면.
도 2는 종래의 싱글 폴리 이이피돌의 단면도.

도 3은 종래의 싱글 폴리 이이피돌의 회로도를 간략하게 나타낸 도면.

도 4는 본 발명의 실험 예에 따른 싱글 폴리 이이피돌을 나타낸 도면.

도 5는 본 발명의 실험 예에 따른 싱글 폴리 이이피돌의 단면도.

도 6은 본 발명의 실험 예에 따른 싱글 폴리 이이피돌의 회로도를 간략하게 도시한 도면.

도 7a 내지 도 7d는 본 발명의 일 실험 예에 따라 싱글 폴리 이이피돌을 제조하는 과정을 나타낸 공정 순서도.
【도면】

【도 1】

【도 2】

【도 3】
【도 4】

【도 5】

【도 6】
Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections.

Applicant(s)

Hyung-Keun Lee, Mapo-gu, KOREA, REPUBLIC OF;

Power of Attorney: None

Domestic Priority data as claimed by applicant

Foreign Applications

REPUBLIC OF KOREA 10-2008-0137592 12/30/2008

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Projected Publication Date: 07/01/2010

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DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

Attorney Docket Number 801-0310

First Named Inventor Hyung-Ksun Lee

COMPLETE IF KNOWN

Application Number

Filing Date

Art Unit

Examiner Name

I hereby declare that: (1) Each inventor's residence, mailing address, and citizenship are as stated below next to their name; and (2) I believe the inventor(s) named below to be the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought on the invention titled:

EEPROM DEVICE AND METHOD OF MANUFACTURING THE SAME

(Title of the invention)

the application of which

X is attached hereto

OR

□ was filed on (MM/DD/YYYY) ________________ as United States Application Number or PCT International Application Number ________________ and was amended on (MM/DD/YYYY) ________________ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified application, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

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X If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the above-identified patent application is filed access to the above-identified patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the above-identified patent application is filed to have access to the above-identified patent application.

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**DECLARATION — Utility or Design Patent Application**

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☐ Additional foreign application number(s) are listed on a supplemental priority data sheet PTO/SB/028 attached hereeto.

[Page 2 of 3]
DECLARATION — Utility or Design Patent Application

Direct all correspondence to: ☒ The address associated with Customer Number: 80603

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NAME OF SOLE OR FIRST INVENTOR:

A petition has been filed for this unsigned inventor

Hyung-Keun Lee

Inventor's Signature

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□ Additional inventors or a legal representative are being named on the supplemental sheet(s) PTO/ SB/2A or O2/LR, attached hereto
EEPROM DEVICE AND METHOD OF MANUFACTURING THE SAME

The present application claims priority under 35 U.S.C. 119 to Korean Patent Application No. 10-2008-0137592 (filed on December 30, 2008), which is hereby incorporated by reference in its entirety.

BACKGROUND

In general, flash memories have the advantage of not losing stored data even if power is cut, such that they are widely used for storing data for a PC Bios, a set-top box, a printer, and a network server, etc., and recently, also used in digital cameras and mobile phones. In these flash memories, EEPROM type flash memory devices, which have a function of electrically erasing data of memory cells in a package or a sector unit, increases threshold voltage of a cell transistor by generating channel hot electrons at a drain in programming and accumulating the electrons in a floating gate. On the contrary, they decrease the threshold voltage of the cell transistor by generating high voltage between a source/substrate and the floating gate to discharging the electrons accumulated in the floating gate. These EEPROM devices can be categorized as a single poly EEPROM and a double poly EEPROM, in accordance with the manufacturing technology and the number of polysilicon layers utilized.

FIG. 1 is a view showing a related single poly EEPROM and FIG. 2 is a cross-sectional
view of the single poly EEPROM of FIG. 1. A single poly EEPROM is largely composed of a tunneling region A, a read transistor B, and a control gate C, etc. In order not to perform operations of programming and erasing, the EEPROM requires a large amount of capacitance ratio between the tunneling region A and the control gate C, and it is required to apply a relatively large voltage to the tunneling region A and a relatively small voltage to the control gate C to achieve the capacity difference.

The overlap area of a polysilicon layer on the tunneling region A and the control gate C may be made different to achieve the capacity difference. However, this method which can result in making the control gate C, which needs to have a relatively large area, have a relatively large area on semiconductor substrate, and as a result, the integration of the single poly EEPROM is reduced.

FIG. 3 is a simple circuit diagram of a related single poly EEPROM, in which the single poly EEPROM makes the overlap area of a polysilicon layer and an active region in the tunneling region A and the control gate C different so that the capacities are different in the two regions. In two series capacitors C1 and C2, the areas A1 and A2 are different and the capacities C1 and C2 are correspondingly different, and external bias voltage Vc for programming and erasing is divided in an inversely proportional ratio to each capacity and applied to the capacitors C1 and C2. Accordingly, the capacitor C1 having small capacity (e.g.
small area) is applied with a relatively higher voltage than the capacitor C2, thereby generating tunneling. That is, the two capacitors C1 and C2 have relationships of C1=ε(A1/d), C2=ε(A2/d), C1/C2=A1/A2=V2/V1, etc.

In the structure of the single poly EEPROM, since there may be a ratio of the overlap area difference so that tunneling is generated at a side and not generated at the other side, the control gate C that is a region where tunneling should not be generated has to have a relatively large area. For example, there may be several tens of times difference between the areas (i.e., a and c) of the polysilicon overlapping at the tunneling region A and the region of the control gate C; therefore, the area of the control gate C occupies a relatively large portion of the area of the single poly EEPROM, which reduces the integration of the single poly EEPROM.

**SUMMARY**

Embodiments relate to an EEPROM (Electrically Erasable Programmable Read-Only Memory) device. In detail, embodiments relate to an EEPROM device that is suitable for increasing the integration of a device by reducing the area of a control gate of the EEPROM device, and a method of manufacturing a EEPROM device. Embodiments relate to an EEPROM device of which the integrity can be improved by reducing the area of a control gate by adjusting the thickness of a gate oxide layer of a region where the control gate is formed.
An EEPROM device according to embodiments includes: a field oxide layer that defines an active region and a field region of a semiconductor substrate; conductive wells that respectively correspond to a tunneling region, a read transistor, and a control gate, under the active region of the upper surface of the semiconductor substrate; a gate oxide layer that is formed to have a relatively smaller thickness at the control gate than at the tunneling region, on the upper surface of the semiconductor substrate divided by the field oxide layer; and a polysilicon layer that is formed on and/or over the field oxide layer and the gate oxide layer from the tunneling region to the control gate.

A method of manufacturing an EEPROM device according to embodiments, includes: forming conductive wells respectively corresponding to a tunneling region, a read transistor, and a control gate between field oxide layers formed on and/or over a semiconductor device; forming a gate oxide layer on and/or over the conductive wells; removing the gate oxide layer at a predetermined thickness from the control gate; and forming a polysilicon layer on and/or over the field oxide layer and the gate oxide layer.

**DRAWINGS**

FIG. 1 is a view showing a related single poly EEPROM.

FIG. 2 is a cross-sectional view of the single poly EEPROM of FIG. 1.
FIG. 3 is a simple circuit diagram of a single poly EEPROM of FIG. 1.

FIG. 4 is a view showing a single poly EEPROM according to embodiments.

FIG. 5 is a cross-sectional view of a single poly EEPROM according to embodiments.

FIG. 6 is a simple circuit diagram of a poly single EEPROM according to embodiments.

FIGS. 7A to 7D are a sequence of cross-section views illustrating a procedure of manufacturing a single poly EEPROM according to embodiments.

DESCRIPTION

FIG. 4 is a view showing a single poly EEPROM according to embodiments. FIG. 5 is a cross-sectional view of a single poly EEPROM according to embodiments. FIG. 6 is a simple circuit diagram of a poly single EEPROM according to embodiments.

Referring to FIGS. 4 to 6, an EEPROM device according to embodiments may include: conductive wells Nwell, Pwell, and Nwell respectively corresponding to a tunneling region A’, a read transistor B’, and a control gate C’, under the surface of a semiconductor substrate; a field oxide layer defining an active region and a field region, a gate oxide layer formed to have a relatively small thickness (5a>5b) at the control gate C’ than the tunneling region A’ on the upper surface of the semiconductor substrate divided by the field oxide layer; a polysilicon layer Poly formed on and/or over the field oxide layer and the gate oxide layer (i.e. Ox) from the
tunneling region A' and the control gate C'; and interlayer dielectric layer PMD formed on and/or over the semiconductor substrate on which the polysilicon Poly is formed.

Unlike a related single poly EEPROM having the same thickness of a gate oxide Ox, by making the thickness 5a of the gate oxide layer Ox of the tunneling region A' relatively larger than the thickness 5b of the gate oxide layer Ox of the control gate C', capacity can be adjusted in accordance with the area and thickness. That is, as the thickness of the gate oxide layer at the control gate C' decreases, the area of the control gate C' can be decreased.

**Formula 1**

\[
\frac{C_1}{C_2} = \frac{A_1d_2}{A_2d_1} = \frac{V_2}{V_1}
\]

As in Formula 1, the capacity is changed as a function of the area and the thickness, such that the capacity changes as much as the thickness ratio of the gate oxide layer Ox. Accordingly, the area of the control gate C' can be decreased, corresponding to the reduction ratio of thickness of the gate oxide layer Ox of the control gate C' with respect to the gate oxide layer Ox of the tunneling region, and the integrity of the EEPROM device can be maximized by adjusting the thickness of the gate oxide layer Ox used for both regions.

Additionally, FIGS. 7A to 7D are a sequence of cross-section views illustrating a
procedure of manufacturing a single poly EEPROM according to embodiments. Referring to FIGS. 7A and 7B, first, a field oxide layer 702 shown in FIG. 7A is formed on and/or over a semiconductor substrate 700 by an ion implantation process or an oxidization process, in accordance with a mask defining an active region and a field region. It should be understood that a dummy oxide layer can be formed to uniformly form the field oxide layer 702 isolating the active region and the field region.

Subsequently, as shown in FIG. 4 and FIG. 7B, the conductive wells 704a, 704b, 704c corresponding to the tunneling region A', read transistor B', and control gate C' may be formed, and then a gate oxide layer 706 is formed at the active region defined by the field oxide layer 702 on and/or over an upper surface of the semiconductor substrate 700, as shown in FIG. 7B. In this configuration, for example, an N-type well can be formed for the conductive wells 704a and 704c respectively corresponding to the tunneling region A' and the control field C', and a P-type well can be formed for the conductive well 704b corresponding to the read transistor B'.

Next, the oxide layer may be removed at a predetermined thickness as shown in FIG. 7C, for example, by a deglaze process, in accordance with a photoresist pattern opening only the gate oxide region corresponding to the control gate C' on the semiconductor substrate 700 with the conductive wells 704a, 704b, and 704c. The predetermined thickness can be set to correspond to the tunneling region A' to acquire a desired capacity ratio with respect to the EEPROM
device.

Subsequently, the photoresist pattern may be removed by a predetermined ashing process, a polysilicon layer 708 can be formed from the tunneling region A' to the control gate C' on and/or over the semiconductor substrate 700, and then an interlayer dielectric layer 710 may be formed thereon, as shown in FIG. 7D. In this configuration, the interlayer dielectric layer 710 can be formed, for example, by depositing a dielectric substance, such as TEOS (tetra ethyl ortho silicate), USG(undoped silicate glass), BPSG(boron phosphorus silicate glass), and PSG (phosphorus silicate glass), using CVD (chemical vapor deposition), and then planarizing the upper portion, using, for example, CMP (chemical mechanical polishing).

In accordance with embodiments, an EEPROM device may have, at the region where the control gate is formed, a gate oxide layer having a relatively smaller thickness than the gate oxide layer of the tunneling region by removing the gate oxide layer, at a predetermined thickness, at the region where the control gate is formed. Thus, integration of an EEPROM device may be maximized as a result of minimizing the area of the control gate.

It will be obvious and apparent to those skilled in the art that various modifications and variations can be made in the embodiments disclosed. Thus, it is intended that the disclosed embodiments cover the obvious and apparent modifications and variations, provided that they are within the scope of the appended claims and their equivalents.
WHAT IS CLAIMED IS:

1. A device, comprising:

   a field oxide layer that defines an active region and a field region of a semiconductor substrate;

   conductive wells that respectively correspond to a tunneling region, a read transistor, and a control gate, under the active region of an upper surface of the semiconductor substrate;

   a gate oxide layer that is formed to have a relatively smaller thickness at the control gate than at the tunneling region, on the upper surface of the semiconductor substrate divided by the field oxide layer; and

   a polysilicon layer that is formed over the field oxide layer and the gate oxide layer from the tunneling region to the control gate.

2. The device of claim 1, wherein as the thickness of the control gate reduces, the gate oxide layer reduces the area of the control gate.

3. The device of claim 1, wherein the conductive wells respectively corresponding to the tunneling region and the control gate are first conductive types, and the conductive well
corresponding to the read transistor is a second conductive type.

4. The device of claim 1, further comprising an interlayer dielectric layer formed over the polysilicon layer.

5. The device of claim 4, wherein the interlayer dielectric layer comprises tetra ethyl ortho silicate.

6. The device of claim 4, wherein the interlayer dielectric layer comprises undoped silicate glass.

7. The device of claim 4, wherein the interlayer dielectric layer comprises boron phosphorus silicate glass.

8. The device of claim 4, wherein the interlayer dielectric layer comprises phosphorus silicate glass.

9. The device of claim 4, wherein a top surface of the interlayer dielectric layer is
planarized.

10. A method comprising:

forming conductive wells respectively corresponding to a tunneling region, a read
transistor, and a control gate between field oxide layers formed on a semiconductor substrate;

forming a gate oxide layer over the conductive wells;

removing the gate oxide layer at a predetermined thickness from the control gate; and

forming a polysilicon layer over the field oxide layer and the gate oxide layer.

11. The method of claim 10, wherein the removing of gate oxide layer from the control
gate is performed by a deglaze process.

12. The method of claim 11, wherein the deglaze process is performed by using a
photoresist pattern selectively exposing the gate oxide layer corresponding to the control gate.

13. The method of claim 10, wherein as the thickness of the control gate decreases, the
gate oxide layer reduces the area of the control gate.
14. The method of claim 10, comprising:

forming an interlayer dielectric layer over the polysilicon layer.

15. The method of claim 14, wherein the interlayer dielectric layer comprises tetra ethyl ortho silicate.

16. The method of claim 14, wherein the interlayer dielectric layer comprises undoped silicate glass.

17. The method of claim 14, wherein the interlayer dielectric layer comprises boron phosphorus silicate glass.

18. The method of claim 14, wherein the interlayer dielectric layer comprises phosphorus silicate glass.

19. The method of claim 14, wherein forming the interlayer dielectric layer over the polysilicon layer includes chemical vapor deposition.
20. The method of claim 14, comprising:

planarizing an upper portion of the interlayer dielectric layer over the polysilicon layer.
ABSTRACT

An EEPROM device may have, at the region where the control gate is formed, a gate oxide layer having a relatively smaller thickness than the gate oxide layer of the tunneling region by removing the gate oxide layer, at a predetermined thickness, at the region where the control gate is formed. Thus, integration of an EEPROM device may be maximized as a result of minimizing the area of the control gate.
### Electronic Patent Application Fee Transmittal

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**Title of Invention:** EEPROM DEVICE AND METHOD OF MANUFACTURING THE SAME

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**Claims:**

**Miscellaneous-Filing:**

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| Total Files Size (in bytes) | 2001358 |

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**New Applications Under 35 U.S.C. 111**

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/D0/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.
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** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (total or independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.