APPLICATION NO. | ISSUE DATE | PATENT NO. | ATTORNEY DOCKET NO. | CONFIRMATION NO.  
--- | --- | --- | --- | ---  
12/641,410 | 06/05/2012 | 8193052 | SUN.DH.630 | 1570  
23557 | 790 | 05/16/2012 |  
SALIWANCHIK, LLOYD & EISENSCHENK  
A PROFESSIONAL ASSOCIATION  
PO Box 142950  
GAINESVILLE, FL 32614  

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

**Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)**  
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 166 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Sung Kun Park, Chungbuk, KOREA, REPUBLIC OF;
PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

or Fax
(571) 273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

22357 7569
2/02/2012
SAI IWANCHIK, L.LOYD & EISENSCHENK
A PROFESSIONAL ASSOCIATION
PO Box 142950
GAINESVILLE, FL 32614

Phone: (352) 375-8100 Fax: (352) 372-5800

APPLICATION NO: 12/641,140 FILING DATE: 12/18/2009
FIRST NAMED INVENTOR: Sung Kun Park
ATTORNEY DOCKET NO: SUN.DH.630 CONFIRMATION NO: 1570

TITLE OF INVENTION: FLASH MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME

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1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.353)
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication for "Fee Address" Indication form PTO/SB/147 Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
   (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
   (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

   Saliwanchik, Lloyd & Eiseenschienk

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

   PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form if NOT a substitute for filing an assignment.

   (A) NAME OF ASSIGNEE:
   DONGBU HITEK CO., LTD
   SEOUL, KOREA

   (B) RESIDENCE: (CITY and STATE OR COUNTRY)

   Please check the appropriate assignee category or categories (will not be printed on the patent):
   ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fees are submitted:
   ☐ Issue Fee
   ☐ Publication Fee (No small entity discount permitted)
   ☐ Advance Order - # of Copies

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)
   ☐ A check is enclosed.
   ☐ Payment by credit card. Form PTO-2038 is attached.
   ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number: ☐ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)
   ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
   ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature: [Signature]
Typed or printed name: [Name]
Date: May 3, 2012
Registration No: 35,589

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.19. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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PTO/A-85 (Rev. 02/11) Approved for use through 08/31/2013.
OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
# Electronic Patent Application Fee Transmittal

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## Utility under 35 USC 111(a) Filing Fees

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The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)
Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)
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**New Applications Under 35 U.S.C. 111**
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.
NOTICE OF ALLOWANCE AND FEE(S) DUE

23557 7590 02/15/2012
SALIWANCHIK, LLOYD & EISENSCHENK
A PROFESSIONAL ASSOCIATION
PO Box 142950
GAINESVILLE, FL 32614

EXAMINER
PHAM, HOAI V

ART UNIT 2892
PAPER NUMBER

APPLICATION NO. 12/641,410
FILING DATE 12/18/2009
FIRST NAMED INVENTOR Sung Kun Park
ATTORNEY DOCKET NO. SUN.DEH.630
CONFIRMATION NO. 1570

TITLE OF INVENTION: FLASH MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME

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THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

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A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.
**PART B - FEE(S) TRANSMITTAL**

Complete and send this form, together with applicable fee(s), to: **Mail**

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

or **Fax**

(571)-273-2885

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**CURRENT CORRESPONDENCE ADDRESS** (Note: Use Block 1 for any change of address)

| 23557 |
| 7590 |
| 02/15/2012 |

SALIWANCHIK, LLOYD & EISENSCHENK
A PROFESSIONAL ASSOCIATION
PO Box 142950
GAINESVILLE, FL 32614

**Certificate of Mailing or Transmission**

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

| (Deposit's name) |
| (Signature) |
| (Date) |

**APPLICATION NO.**

12/641,410

**FILING DATE**

12/18/2009

**FIRST NAMED INVENTOR**

Sung Kun Park

**ATTORNEY DOCKET NO.**

SUN.DH.630

**CONFIRMATION NO.**

1570

**TITLE OF INVENTION:** FLASH MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME

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3. **ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT** (print or type)

   **PLEASE NOTE:** Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is **NOT** a substitute for filing an assignment.

   **(A) NAME OF ASSIGNEE**

   **(B) RESIDENCE: (CITY and STATE OR COUNTRY)**

Please check the appropriate assignee category or categories (will not be printed on the patent):

- [ ] Individual
- [ ] Corporation or other private group entity
- [ ] Government

4a. The following fee(s) are submitted:

- [ ] Issue Fee
- [ ] Publication Fee (No small entity discount permitted)
- [ ] Advance Order - # of Copies

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PTOL-85 (Rev. 02/11) Approved for use through 08/31/2013.

OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 166 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 166 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

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Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.
Notice of Allowability

Application No. 12/641,410
Applicant(s) PARK, SUNG KUN
Examiner HOAI V. PHAM
Art Unit 2892

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 12/30/2011.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☐ The allowed claim(s) is/are 7.9-12 and 21-27.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All    b) ☐ Some*    c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____.
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE MAILING DATE of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER’S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as “replacement sheets”) must be submitted.
   a) ☐ including changes required by the Notice of Draftsperson’s Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   b) ☐ including changes required by the attached Examiner’s Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner’s comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
3. ☐ Information Disclosure Statements (PTO/SD/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____
7. ☐ Examiner’s Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/HOAI V. PHAM/
Primary Examiner, Art Unit 2892

U.S. Patent and Trademark Office
PTOL-37 (Rev. 03-11) Notice of Allowability Part of Paper No./Mail Date 20120203
DETAILED ACTION

Allowable Subject Matter

1. Claims 7, 9-12, and 21-27 are allowed.

2. The following is an examiner's statement of reasons for allowance: the prior of record fails to disclose the combination of a flash memory device structure recited in the base claims 7, 21 and 22, including the combination of the structure comprising: forming an ONO layer on the semiconductor substrate having the floating gate and the hard mask; and performing an etch back process for the ONO layer (claim 7); forming an insulating layer on the semiconductor substrate; forming a gate spacer at one side of the select gate and one side of the floating gate by performing an etch back process with respect to the insulating layer; and forming a source area in a vicinity of the floating gate and a drain area in a vicinity of the select gate by implanting impurities into the semiconductor substrate, after forming the select gate (claim 21); forming an ONO pattern on a sidewall of the floating gate and the hard mask; forming a polysilicon pattern on the ONO pattern on the sidewall of the floating gate and the hard mask; and forming a select gate by removing a portion of the polysilicon pattern (claim 22).

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HOAI V. PHAM whose telephone number is (571)272-1715. The examiner can normally be reached on M-F.
4. If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Thao Xuan Le can be reached on 571-272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

5. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HOAI V PHAM/
Primary Examiner, Art Unit 2892
**Issue Classification**

**Application/Control No.**
12641410

**Applicant(s)/Patent Under Reexamination**
PARK, SUNG KUN

**Examiner**
HOAI V PHAM

**Art Unit**
2892

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**Total Claims Allowed:**

- **12**

**Assistant Examiner**

/ HOAI V PHAM/
Primary Examiner. Art Unit 2892

**Primary Examiner**

02/03/2012

**O.G. Print Claim(s)**

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**O.G. Print Figure**

- **9**

U.S. Patent and Trademark Office

Part of Paper No. 20120203
### Search Notes

**Application/Control No.**
12641410

**Applicant(s)/Patent Under Reexamination**
PARK, SUNG KUN

** Examiner **
HOAI V PHAM

** Art Unit **
2892

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** APPLICANTS **
Sung Kun Park, Chungbuk, KOREA, REPUBLIC OF;

** CONTINUING DATA ********************

** FOREIGN APPLICATIONS *******************
REPUBLIC OF KOREA 10-2008-0138873 12/31/2008

** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **
01/04/2010

- Foreign Priority claimed: Yes [☑] No [ ]
- 35 USC 119(a-d) conditions met: Yes [☑] No [ ]
- Met after Allowance: [ ]

ADDRESS
SALIWANCHIK, LLOYD & EISENSCHENK
A PROFESSIONAL ASSOCIATION
PO Box 142950
GAINESVILLE, FL 32614
UNITED STATES

TITLE
FLASH MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME

- Authority has been given in Paper No. ________ to charge/credit DEPOSIT ACCOUNT No. ________ for following:

- All Fees
- 1.16 Fees (Filing)
- 1.17 Fees (Processing Ext. of time)
- 1.18 Fees (Issue)
- Other ___________
- Credit

FILING FEE RECEIVED
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I hereby certify that this correspondence is being electronically transmitted via EFS to the United States Patent and Trademark Office on December 30, 2011.

Jeff Lloyd, Patent Attorney, Reg. No. 35,589

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Examiner : Hoai V. Pham
Art Unit : 2892
Applicant : Sung Kun Park
Serial No. : 12/641,410
Filed : December 18, 2009
Confirm. No. : 1570
For : Flash Memory Device and Method of Manufacturing the Same

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT UNDER 37 C.F.R. § 1.111

Sir:

In response to the Office Action dated October 11, 2011, please amend the application identified above as follows:

J:\SUN\DH\630\Amnd\Response1.doc\nr/sjk
In the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

1-6. (Canceled)

7. (Currently Amended) A method of manufacturing a flash memory device, the method comprising:
   forming a floating gate on a semiconductor substrate and a hard mask on the floating gate;
   forming an ONO pattern on a sidewall of the floating gate and the hard mask;
   forming a polysilicon pattern on the ONO pattern on the sidewall of the floating gate and the hard mask; and
   forming a select gate by removing a portion of the polysilicon pattern,
   wherein the forming of the ONO pattern comprises:
   forming an ONO layer on the semiconductor substrate having the floating gate and the hard mask; and
   performing an etch back process for the ONO layer.

8. (Canceled)

9. (Currently Amended) The method of claim 7, wherein forming the floating gate on the semiconductor substrate forms one floating gate in each active region of a cell region of the semiconductor substrate, wherein the floating gates are isolated from each other.

10. (Original) The method of claim 7, wherein the forming of the polysilicon pattern comprises:
    forming a polysilicon layer on an entire surface of the semiconductor substrate; and
    performing an etch back process with respect to the polysilicon layer, thereby exposing the hard mask and remaining the polysilicon layer on the sidewall of the floating gate,
    wherein the floating gate and hard mask are formed in plurality, wherein the polysilicon pattern is connected between closely adjacent floating gates.
11. (Original) The method of claim 10, wherein, when forming the select gate by removing the portion of the polysilicon pattern, the portion of the polysilicon pattern removed corresponds to the connected polysilicon pattern between the closely adjacent floating gates.

12. (Original) The method of claim 7, further comprising:
   forming an insulating layer on the semiconductor substrate;
   forming a gate spacer at one side of the select gate and one side of the floating gate by
   performing an etch back process with respect to the insulating layer; and
   forming a source area in a vicinity of the floating gate and a drain area in a vicinity of the
   select gate by implanting impurities into the semiconductor substrate, after forming the select gate.

13–20. (Canceled)

21. (New) A method of manufacturing a flash memory device, the method comprising:
   forming a floating gate on a semiconductor substrate and a hard mask on the floating gate;
   forming an ONO pattern on a sidewall of the floating gate and the hard mask;
   forming a polysilicon pattern on the ONO pattern on the sidewall of the floating gate and the
   hard mask;
   forming a select gate by removing a portion of the polysilicon pattern;
   forming an insulating layer on the semiconductor substrate;
   forming a gate spacer at one side of the select gate and one side of the floating gate by
   performing an etch back process with respect to the insulating layer; and
   forming a source area in a vicinity of the floating gate and a drain area in a vicinity of the
   select gate by implanting impurities into the semiconductor substrate, after forming the select gate.

22. (New) A method of manufacturing a flash memory device, the method comprising:
   forming a floating gate on a semiconductor substrate and a hard mask directly on a top
   surface of the floating gate;
forming an ONO pattern on a sidewall of the floating gate and the hard mask;
forming a polysilicon pattern on the ONO pattern on the sidewall of the floating gate and the hard mask; and
forming a select gate by removing a portion of the polysilicon pattern.

23. (New) The method of claim 22, wherein the forming of the ONO pattern comprises:
forming an ONO layer on the semiconductor substrate having the floating gate and the hard mask; and
performing an etch back process for the ONO layer.

24. (New) The method of claim 22, wherein forming the floating gate on the semiconductor substrate forms one floating gate in each active region of a cell region of the semiconductor substrate, wherein the floating gates are isolated from each other.

25. (New) The method of claim 22, wherein the forming of the polysilicon pattern comprises:
forming a polysilicon layer on an entire surface of the semiconductor substrate; and
performing an etch back process with respect to the polysilicon layer, thereby exposing the hard mask and remaining the polysilicon layer on the sidewall of the floating gate,
wherein the floating gate and hard mask are formed in plurality, wherein the polysilicon pattern is connected between closely adjacent floating gates.

26. (New) The method of claim 25, wherein, when forming the select gate by removing the portion of the polysilicon pattern, the portion of the polysilicon pattern removed corresponds to the connected polysilicon pattern between the closely adjacent floating gates.

27. (New) The method of claim 26, further comprising:
forming an insulating layer on the semiconductor substrate;
forming a gate spacer at one side of the select gate and one side of the floating gate by performing an etch back process with respect to the insulating layer; and

forming a source area in a vicinity of the floating gate and a drain area in a vicinity of the select gate by implanting impurities into the semiconductor substrate, after forming the select gate.
Remarks

Claims 1-20 are pending in the subject application. Claims 7 and 9 are amended; claims 1-6, 8, and 13-20 are canceled; and claims 21-27 are added. Support for new claims 22-27 can be found, for example, at Figures 1A-1C and original claims 7-12. No new matter is introduced by these amendments. Upon entry of these amendments, claims 7, 9-12, and 21-27 will be before the Examiner. Favorable consideration of the pending claims is respectfully requested.

At the outset, Applicant gratefully acknowledges the Examiner’s indication that claims 8 and 12 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim. Accordingly, claim 7 is amended to incorporate the limitations of allowable claim 8; claim 8 is canceled as duplicative; and new claim 21 is original claim 12 re-written in independent form.

Claims 19-20 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite. This rejection is rendered moot by the cancelation of claims 19-20.

Claims 7, 9-11 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen et al. (U.S. 2005/0207199; herein after “Chen”). This rejection is rendered moot by the above amendments.

With respect to new claims 22-27, Applicant respectfully submits that, at a minimum, the cited reference fails to disclose “forming a floating gate on a semiconductor substrate and a hard mask directly on a top surface of the floating gate,” as specified in claim 22, from which claims 23-27 depend. Instead of forming a hard mask directly on a top surface of a floating gate, Chen teaches forming a hard mask 66 on a control gate 38 on the floating gate 37 (see Chen’s paragraph [0029]).

In view of the foregoing remarks and amendments to the claims, Applicant believes that the claims as currently pending are in condition for allowance, and such action is respectfully requested.

Applicant invites the Examiner to call the undersigned if clarification is needed on any of this response, or if the Examiner believes a telephonic interview would expedite the prosecution of the subject application to completion.
The Commissioner is hereby authorized to charge any fees under 37 C.F.R. §§ 1.16 or 1.17 as required by this paper to Deposit Account 19-0065.

Respectfully submitted,

[Signature]

Jeff Lloyd
Patent Attorney
Registration No. 35,589
Phone No.: 352-375-8100
Fax No.: 352-372-5800
Address: Saliwanchik, Lloyd & Eisenschenk
A Professional Association
P.O. Box 142950
Gainesville, FL 32614-2950

JL/jrr/sjk
# Electronic Acknowledgement Receipt

| **EFS ID:** | 11734503 |
| **Application Number:** | 12641410 |
| **International Application Number:** |  |
| **Confirmation Number:** | 1570 |

**Title of Invention:** FLASH MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME

| **First Named Inventor/Applicant Name:** | Sung Kun Park |
| **Customer Number:** | 23557 |
| **Filer:** | Jeff Lloyd/Wea Sto Domingo |
| **Filer Authorized By:** | Jeff Lloyd |
| **Attorney Docket Number:** | SUN.DH.630 |
| **Receipt Date:** | 30-DEC-2011 |
| **Filing Date:** | 18-DEC-2009 |
| **Time Stamp:** | 11:07:25 |
| **Application Type:** | Utility under 35 USC 111(a) |

## Payment information:
- Submitted with Payment: no

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Warnings:

Information:

| Total Files Size (in bytes) | 245079 |

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.
**PATENT APPLICATION FEE DETERMINATION RECORD**

**APPLICATION AS FILED – PART I**

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**APPLICATION AS AMENDED – PART II**

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**LEGAL INSTRUMENT EXAMINER:**

/MYRTLE LEIGH/

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" in THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" in THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.
Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

euspto@slepatents.com
Office Action Summary

Application No. 12/641,410
Applicant(s) PARK, SUNG KUN

Examiner HOAI V. PHAM
Art Unit 2892

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) □ Responsive to communication(s) filed on 24 August 2011.
2a) □ This action is FINAL.
  2b) □ This action is non-final.
3) □ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
4) □ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5) ☑ Claim(s) 1-20 is/are pending in the application.
  5a) Of the above claim(s) 1-6 and 13-18 is/are withdrawn from consideration.
6) □ Claim(s) _____ is/are allowed.
7) ☑ Claim(s) 7, 9-11, 19 and 20 is/are rejected.
8) □ Claim(s) 8 and 12 is/are objected to.
9) □ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10) □ The specification is objected to by the Examiner.
11) □ The drawing(s) filed on _____ is/are: a)□ accepted or b)☐ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
12) □ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13) ☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a)☐ All b)☐ Some * c)☐ None of:
    1. ☑ Certified copies of the priority documents have been received.
    2. □ Certified copies of the priority documents have been received in Application No. ______.
    3. □ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)
2) □ Notice of Draftsman’s Patent Drawing Review (PTO-948)
3) □ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date ______.
4) □ Interview Summary (PTO-413)
    Paper No(s)/Mail Date ______.
5) □ Notice of Informal Patent Application
6) □ Other: ______.

U.S. Patent and Trademark Office
PTOL-326 (Rev. 03-11) Office Action Summary Part of Paper No./Mail Date 20111001
DETAILED ACTION

Election/Restrictions

1. Applicant’s election without traverse of 7-12 and 19-20 in the reply filed on 08/24/2011 is acknowledged.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

   The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 19-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

   The limitation “forming floating gates spaced apart from each other by a predetermined distance” renders the claim indefinite. It is not clear where the floating gates formed on.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

   A person shall be entitled to a patent unless –

   (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 7, 9-11 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen et al [US 2005/0207199 A1].
With respect to claim 7, Chen et al (fig. 4, cols. 2-3) disclose a method of manufacturing a flash memory device, the method comprising:

forming a floating gate (37) on a semiconductor substrate (41) and a hard mask (66) on the floating gate;

forming an ONO pattern (47) on a sidewall of the floating gate and the hard mask;

forming a polysilicon pattern (59) on the ONO pattern on the sidewall of the floating gate and the hard mask; and

forming a select gate (44) by removing a portion of the polysilicon pattern.

With respect to claim 9, Chen et al (fig. 4, cols. 2-3) disclose that forming the floating gate (37) on the semiconductor substrate forms one floating gate in each active region of a cell region of the semiconductor substrate, wherein the floating gates are isolated from each other.

With respect to claim 10, Chen et al (figs. 3-4, cols. 2-3) disclose that the forming of the polysilicon pattern comprises: forming a polysilicon layer (59) on an entire surface of the semiconductor substrate; and performing an etch back process with respect to the polysilicon layer, thereby exposing the hard mask and remaining the polysilicon layer on the sidewall of the floating gate, wherein the floating gate and hard mask are formed in plurality, wherein the polysilicon pattern is connected between closely
adjacent floating gates.

With respect to claim 11, Chen et al (figs. 3-4, cols. 2-3) disclose that forming the select gate (44) by removing the portion of the polysilicon pattern, the portion of the polysilicon pattern removed corresponds to the connected polysilicon pattern between the closely adjacent floating gates (37).

With respect to claim 19, as best understood, Chen et al (figs. 3-4, cols. 2-3) disclose a method of manufacturing a flash memory device, the method comprising:

forming floating gates (37) spaced apart from each other by a predetermined distance on a semiconductor substrate (41); forming an ONO pattern (47) surrounding lateral sides of the floating gates; forming a word line including select gates (44) aligned in one direction along one sidewall of each of the floating gates while being connected to each other; and

forming a source area (49) at one side of each floating gate, and forming a drain area (50) at a side of the word line in opposition to the source area.

Allowable Subject Matter

6. Claims 8 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HOAI V. PHAM whose telephone number is (571)272-1715. The examiner can normally be reached on M-F.

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Thao Xuan Le can be reached on 571-272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HOAI V PHAM/
Primary Examiner, Art Unit 2892
Notice of References Cited

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NON-PATENT DOCUMENTS

Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)

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| X                       |        |         |               |                |

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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- **✓** Rejected
- **-** Cancelled
- **+** Restricted
- **N** Non-Elected
- **I** Interference
- **A** Appeal
- **O** Obj ected

**Claims renumbered in the same order as presented by applicant**: [ ]
- [ ] CPA
- [ ] T.D.
- [ ] R.1.47

**Application/Control No.**: 12641410
**Examiner**: HOAI V PHAM
**Art Unit**: 2892

**Date of Final**: 07/28/2011
**Date of Original**: 10/02/2011
### Search Notes

**Application/Control No.**
12641410

**Applicant(s)/Patent Under Reexamination**
PARK, SUNG KUN

**Examiner**
HOAI V PHAM

**Art Unit**
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U.S. Patent and Trademark Office  Part of Paper No.: 20111001
I hereby certify that this correspondence is being electronically filed in the United States Patent and Trademark Office on August 24, 2011.

Jeff Lloyd, Patent Attorney, Reg. No. 35,589

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Examiner : Hoai V. Pham
Art Unit : 2892
Applicant : Sung Kun Park
Serial No. : 12/641,410
Filed : December 18, 2009
Conf. No. : 1570
For : Flash Memory Device and Method of Manufacturing the Same

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

ELECTION UNDER 35 U.S.C. § 121

Sir:

In response to the written Restriction Requirement dated August 3, 2011 in the application identified above, Applicant hereby elects to prosecute the invention of Group II (claims 7-12 and 19-20), without traverse.

Respectfully submitted,

[Signature]
Jeff Lloyd
Patent Attorney
Registration No. 35,389
Phone No.: 352-375-8100
Fax No.: 352-372-5800
Address: Saliwanchik, Lloyd & Eisenschenk
A Professional Association
P.O. Box 142950
Gainesville, FL 32614-2950

JL/jld
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- **Submitted with Payment:** no

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**Warnings:**

- Information:
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.
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<td>Sung Kun Park</td>
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23557 7590 08/03/2011  
SALIWANCHEK, LLOYD & EISENSCHENK  
A PROFESSIONAL ASSOCIATION  
PO Box 142950  
GAINESVILLE, FL 32614

EXAMINER
PHAM, HOAI V

ART UNIT  
PAPER NUMBER
2892

NOTIFICATION DATE  
DELIVERY MODE
08/03/2011 ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

euspto@slepatents.com
Office Action Summary

Application No. 12/641,410
Applicant(s) PARK, SUNG KUN
Examiner HOAI V. PHAM
Art Unit 2892

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☑ Responsive to communication(s) filed on 18 December 2009.
2a) ☐ This action is FINAL. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☑ Claim(s) 1-20 is/are pending in the application.
   4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☐ Claim(s) _____ is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☑ Claim(s) 1-20 are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☑ All  b) ☐ Some * c) ☐ None of:
       1. ☐ Certified copies of the priority documents have been received.
       2. ☐ Certified copies of the priority documents have been received in Application No. ______.
       3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413)
2) ☐ Notice of Draftsperson’s Patent Drawing Review (PTO-948) Paper No(s)/Mail Date ______.
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) 5) ☐ Notice of Informal Patent Application
   Paper No(s)/Mail Date ______.
6) ☐ Other: ______.
DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:
   I. Claims 1-6 and 13-18, drawn to a semiconductor device, classified in class 257, subclass 315.
   II. Claims 7-12 and 19-20, drawn to a method of making a semiconductor device, classified in class 438, subclass 201.

2. The inventions are distinct, each from the other because of the following reasons:

   Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the product as claimed can be made by another and materially different process such as forming a select gate using a mask in order to alleviate the need for subsequent removing a portion of the polysilicon pattern.

3. Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and examination burden if restriction were not required because one or more of the following reasons apply:

   (a) the inventions have acquired a separate status in the art in view of their different classification;
(b) the inventions have acquired a separate status in the art due to their recognized divergent subject matter;

(c) the inventions require a different field of search (for example, searching different classes/subclasses or electronic resources, or employing different search queries);

(d) the prior art applicable to one invention would not likely be applicable to another invention;

(e) the inventions are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a invention to be examined even though the requirement may be traversed (37 CFR 1.143) and (ii) identification of the claims encompassing the elected invention.

4. The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected invention.
5. If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

6. Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

7. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

8. The examiner has required restriction between product and process claims. Where applicant elects claims directed to the product, and the product claims are subsequently found allowable, withdrawn process claims that depend from or otherwise require all the limitations of the allowable product claim will be considered for rejoinder. All claims directed to a nonelected process invention must require all the limitations of an allowable product claim for that process invention to be rejoined.

9. In the event of rejoinder, the requirement for restriction between the product claims and the rejoined process claims will be withdrawn, and the rejoined process claims will be fully examined for patentability in accordance with 37 CFR 1.104. Thus, to
be allowable, the rejoined claims must meet all criteria for patentability including the
requirements of 35 U.S.C. 101, 102, 103 and 112. Until all claims to the elected product
are found allowable, an otherwise proper restriction requirement between product
claims and process claims may be maintained. Withdrawn process claims that are not
commensurate in scope with an allowable product claim will not be rejoined. See MPEP
§ 821.04(b). Additionally, in order to retain the right to rejoinder in accordance with the
above policy, applicant is advised that the process claims should be amended during
prosecution to require the limitations of the product claims. **Failure to do so may result
in a loss of the right to rejoinder.** Further, note that the prohibition against double
patenting rejections of 35 U.S.C. 121 does not apply where the restriction requirement
is withdrawn by the examiner before the patent issues. See MPEP § 804.01.

10. Any inquiry concerning this communication or earlier communications from the
examiner should be directed to Hoai v. Pham whose telephone number is 571-272-
1715. The examiner can normally be reached on M-F.

11. If attempts to reach the examiner by telephone are unsuccessful, the examiner’s
supervisor, Thao Xuan Le can be reached on 571-272-1708. The fax phone number for
the organization where this application or proceeding is assigned is 571-273-8300.

12. Information regarding the status of an application may be obtained from the
Patent Application Information Retrieval (PAIR) system. Status information for
published applications may be obtained from either Private PAIR or Public PAIR.
Status information for unpublished applications is available through Private PAIR only.
For more information about the PAIR system, see http://pair-direct.uspto.gov. Should
you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hoai v Pham/
Primary Examiner, Art Unit 2892
### Index of Claims

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U.S. Patent and Trademark Office

Part of Paper No.: 20110728
23557
SALIWANCHIK LLOYD & SALIWANCHIK
A PROFESSIONAL ASSOCIATION
PO Box 142950
GAINESVILLE, FL 32614

Title: FLASH MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME
Publication No: US-2010-0163960-A1
Publication Date: 07/01/2010

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publicly available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101
CONFIRMATION NO. 1570
CORRECTED FILING RECEIPT

23557
SALIWANCHIK LLOYD & SALIWANCHIK
A PROFESSIONAL ASSOCIATION
PO Box 142950
GAINESVILLE, FL 32614

Date Mailed: 02/01/2010

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections.

Applicant(s)
Sung Kun Park, Chungbuk, KOREA, REPUBLIC OF;

Power of Attorney: The patent practitioners associated with Customer Number 23557

Domestic Priority data as claimed by applicant

Foreign Applications
REPUBLIC OF KOREA 10-2008-0138873 12/31/2008

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper Request to Retrieve Electronic Priority Application(s) (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 01/04/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is US 12/641,410

Projected Publication Date: 07/01/2010

Non-Publication Request: No

Early Publication Request: No
PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process simplifies the filing of patent applications on the same invention in member countries, but does not result in a grant of “an international patent” and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application’s filing receipt contains further information and guidance as to the status of applicant’s license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as
set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).
REQUEST FOR CORRECTED FILING RECEIPT

Sir:

Applicant respectfully requests the correction of an error in the Filing Receipt for the above-identified patent application. The application was filed with a typographical error in the applicant's city of residence. Please send a corrected Filing Receipt with the following change:

The Filing Receipt lists the residence as:

aaa Chungbuk

The correct spelling for the residence is:

Chungbuk

A copy of the Filing Receipt containing the error is attached. Also submitted herewith is an Application Data Sheet that reflects the correct spelling of the applicant's residence.
If any further information or documentation is required in order to accede to this request for Corrected Filing Receipt, the Office is respectfully requested to contact the undersigned by telephone at 352-375-8100.

Respectfully submitted,

Jeff Lloyd
Patent Attorney
Registration No. 35,589
Phone No.: 352-375-8100
Fax No.: 352-372-5800
Address: P.O. Box 142950
         Gainesville, FL 32614-2950

JL/jlr

Attachments: Copy of Filing Receipt with error noted
             Application Data Sheet
Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections.

Applicant(s)

Sung Kun Park, 23557
Chungbuk, KOREA, REPUBLIC OF;

Power of Attorney: The patent practitioners associated with Customer Number 23557

Domestic Priority data as claimed by applicant

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Initial 1/26/2010
Applicant Information

Applicant Authority Type: Inventor
Primary Citizenship Country: Republic of Korea
Status: Unknown
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Country of Residence: Republic of Korea
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State or Province of mailing address: Chungbuk
Country of Mailing Address: Republic of Korea
Postal or Zip Code of Mailing Address:
APPLICATION DATA SHEET

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City of Mailing Address: Seoul
State or Province or mailing address: Republic of Korea
Country of Mailing Address: 135-280

3/3
Initial 1/26/2010
# Electronic Acknowledgement Receipt

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.
This is to certify that the following application annexed hereto is a true copy from the records of the Korean Intellectual Property Office.

Application Number: 10-2008-0138873

Filing Date: DEC. 31, 2008

Applicant(s): Dongbu HiTek Co., Ltd.

COMMISSIONER
서지사항

【서류명】 특허출원서
【참조번호】 2302
【출원구분】 특허출원
【출원인】
【영칭】 주식회사 동부하이텍
【출원인코드】 1-1998-000857-5
【대리인】
【성명】 허용록
【대리인코드】 9-1998-000616-9
【포괄위임등록번호】 2007-040671-5
【발명의 국문명칭】 플래시 메모리 소자 및 그 제조 방법
【발명의 영문명칭】 flash memory device and fabricating method thereof
【발명자】
【성명】 박성근
【성명의 영문표기】 PARK, SUNG KUN
【주민등록번호】 691225-1XXXXX
【우편번호】 360-779
【주소】 충북 청주시 상당구 금천동 장자마을 현대아파트 201-1502
【국적】 KR

위와 같이 특허청장에게 제출합니다.

대리인
허용록 (인)

수수료

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제출 일자 : 2008-12-31

[요약]

실시에는 플래시 메모리 소자 및 그 제조 방법에 관한 것이다. 실시예에 따른 플래시 메모리 소자는, 반도체 기판 상에 형성된 플로팅 게이트, 상기 플로팅 게이트의 일 측벽에 차가 형립된(self aligned) 셀렉트 게이트 및 상기 플로팅 게이트와 상기 셀렉트 게이트 사이에 형성된 ONO 채단을 포함한다. 실시에는 스플릿 게이트 구조를 채용하는 ETOX(EEROM tunnel oxide)셀 플래시 메모리 소자에서, 자가 형립된 스플릿 게이트 구조를 형성함으로써 셀 커런트가 일정하고 셀간 소거 특성이 균일하여 신뢰성이 향상되는 효과가 있다.

[대표도]

도 9

[색인어]

플래시, 셀렉트, 자가 형립
[발명의 명칭]

플래시 메모리 소자 및 그 제조 방법 (flash memory device and fabricating method thereof)

[발명의 상세한 설명]

[기술분야]

<1> 실시에는 플래시 메모리 소자 및 그 제조 방법에 관한 것이다.

[배경기술]

<2> 일반적으로 비휘발성(non volatile) 메모리는 전원이 중단되어도 저장된 데이터가 손실되지 않는 장점을 가지고 있어 PC 바이어스(Bios)용, 셋톱박스(SETtopBox), 프린터(printer) 및 네트워크 서버(network server) 등의 데이터 저장용으로 많이 사용되고 있으며 최근에는 디지털 카메라와 휴대폰 등에서도 많이 이용되고 있는 실정이다.

<3> 이러한 비휘발성 메모리 중에서도 전기적으로 메모리 셀의 데이터를 일반적으로 또는 섹터(sector) 단위로 소거하는 기능을 가지고 있는 E2PROM(Electrically Erasable Programmable Read-Only Memory)형 플래시 메모리장치는 프로그램시 드레인 측에 채널 열 전자(channel hot electron)를 형성시켜 전자를 플로팅 게이트(floating gate)에 축적함으로써 셀 트랜지스터의 문턱 전압을 증가시킨다.

<4> 반면에, 플래시 메모리 장치의 소거 동작은 소오스/기판과 플로팅 게이트간
의 고전압을 발생시켜 플로팅 게이트에 촉작된 전자를 방출함으로써 셀 트랜지스터의 분극전압을 낮춘다.

<5> 최근 고퀵직화가 급속히 진행됨에 따라 셀 사이즈의 축소가 매우 절실하게 요구되고 있다. 가장 작은 셀 사이즈는 ETOX 셀로서 2개의 폴리실리콘 패턴을 적층하여 어레이를 구성함으로써 하부 폴리실리콘 패턴을 플로팅 게이트(floating gate)로 사용하고 상부 폴리실리콘 패턴을 셀렉트 게이트(select gate)로 사용할 수 있다.

<6> 이 경우 소거를 진행할 때 과 소거(over erase)문제가 발생할 수 있다.

<7> 이와 같은 과소거 문제를 해결하기 위하여 스플릿 게이트 구조(split gate structure)를 적용한 셀을 사용하였다.

<8> 스플릿 게이트의 적용으로 과 소거 문제를 해결하였으나, 플로팅 게이트와 컨트롤 게이트의 오정렬(misalign)에 의하여 소거 상태에서 발생되는 오정렬만큼 셀렉트 게이트로 작용하는 트랜지스터의 게이트 길이가 달라지게 되고 이로 인한 커런트 분포에 차이가 나게 된다. 즉, 샘플간의 특성이 균일하지 않게 된다.

<9> 셀 사이즈의 감소를 위하여 공통 소스 구조를 사용하게 되면 소스 라인의 양 쪽으로 배치되는 이분 및 오드 워드라인들(even/odd word lines)의 커런트가 달라지게 된다.

<10> 이와 같이 게이트 형성이 공정에서 포토 공정 및 오버레이 변동에 따라서 소거 전류 및 커런트비가 달라져 샘 간 균일한 소거 특성을 보장할 수 없으며 신뢰성이
없어지는 문제가 있다.

【발명의 내용】

【해결하고자 하는 과제】

설시에는 스플릿 게이트 구조를 채용하는 ETOX(EEPROM tunnel oxide)셀 플래시 메모리 소자에서, 자가 정렬된 스플릿 게이트 구조를 형성함으로써 셀간 소거 특성을 균일한 플래시 메모리 소자 및 그 제조 방법을 제공한다.

설시에는 플로팅 게이트를 높게 형성하고, 그 측벽에 셀렉트 게이트를 형성함으로써 커폴링비가 증가되는 플래시 메모리 소자 및 그 제조 방법을 제공한다.

설시에는 플로팅 게이트의 측벽에 게이트를 자가 정렬로 형성시킴으로써 셀 커런트가 일정한 플래시 메모리 소자 및 그 제조 방법을 제공한다.

【과제 해결 수단】

설시에 따른 플래시 메모리 소자는, 반도체 기판 상에 형성된 플로팅 게이트, 상기 플로팅 게이트의 일 측벽에 자가 정렬된 (self aligned) 셀렉트 게이트 및 상기 플로팅 게이트와 상기 셀렉트 게이트 사이에 형성된 ONO 패턴을 포함한다.
실시예에 따른 플래시 메모리 소자의 제조 방법은, 반도체 기판 상에 형성된 플로팅 케이트 및 상기 플로팅 케이트 상면에 하드 마스크를 형성하는 단계, 상기 플로팅 케이트 및 상기 하드 마스크 측벽을 둘러싸는 OMO 패턴을 형성하는 단계, 상기 OMO 패턴 상에 형성되며, 상기 플로팅 케이트 및 상기 하드 마스크의 측벽에 형성되는 폴리실리콘 패턴을 형성하는 단계 및 상기 폴리실리콘 패턴의 일부를 제거하여 셀렉트 케이트를 형성하는 단계를 포함한다.

실시예에 따른 플래시 메모리 소자는, 일 반향으로 형성된 셀렉트 케이트로 이루어진 퍼드 라인들, 상기 퍼드 라인의 일측을 따라 서로 소정 간격 이격되어 배치된 플로팅 케이트들, 상기 플로팅 케이트들 일측에 형성된 소스 영역 및 상기 퍼드 라인의 타측을 따라 상기 소스 영역과 대향하여 형성된 드레인 영역을 포함한다.

실시예에 따른 플래시 메모리 소자의 제조 방법은, 서로 소정 간격 이격되어 배치된 플로팅 케이트들을 형성하는 단계, 상기 플로팅 케이트들의 측면을 둘러싼 OMO 패턴을 형성하는 단계, 상기 플로팅 케이트들의 일측벽을 따라 서로 연결되어 일 반향으로 셀렉트 케이트로 이루어진 퍼드 라인을 형성하는 단계 및 상기 플로팅 케이트들 일측에 형성된 소스 영역 및 상기 퍼드 라인의 타측을 따라 상기 소스 영역과 대향하는 드레인 영역을 형성하는 단계를 포함한다.
【효과】

실시에는 스플릿 게이트 구조를 채용하는 ETOX(EEPROM tunnel oxide)셀 플래시 메모리 소자에서, 자가 정렬된 스플릿 게이트 구조를 형성함으로써 셀 커런트가 일정하고 셀간 소거 특성이 균일하여 신뢰성이 향상되는 효과가 있다.

실시에는 플로팅 게이트를 높게 형성하고, 그 수직축에 셀렉트 게이트를 형성함으로써 커플링비가 증가되므로 효율이 증가하는 효과가 있다.

실시에는 MCS(memory Common Source) 구조뿐 아니라 SAS (self aligned Source) 구조의 적용도 가능한 효과가 있다.

실시에는 플로팅 게이트를 ONO가 완전히 덮고 있으므로 리턴선 특성이 좋고 신뢰성이 우수한 효과가 있다.

실시에는 포토 공정에 의하여 스플릿 게이트를 형성하지 않으므로 셀렉트 트랜지스터의 길이가 포토 공정의 미스 일라인에 의하여 불균일하게 결정되지 않고 셀프 일라인에 의하여 형성하므로 항상 소거 Vt가 일정하고 셀 커런트가 일정하여 공정 안정성이 뛰어난 효과가 있다.

실시에는 셀렉트 게이트의 식각을 위해 플로팅 게이트 위에 하드마스크를 적용하여 ONO막의 상부의 손실을 방지하고 이를 후속으로 셀렉트 게이트를 형성할 때 마스크로 사용하는 등 다양도로 사용될 수 있으므로 공정이 단순하고 간단해지는 효과가 있다.

실시에 따른 플래시 메모리 소자는 커플링비에 의해 Vt가 직접적으로 영향
을 맡는 F-N 방식이 아니라 셀렉트 게이트에 의하여 커런트가 제한되는 구조이며 프로그램은 HCl 방식으로, 소기는 BTBT 방식을 사용하므로 키폴링비에 의한 Vt 영향이 적으로 공정 변동에 대하여 감안하므로 공정이 용이하고 소자 특성이 뛰어난 효과가 있다.

실시에 따른 스플릿 게이트 방식으로 플로팅 게이트의 측벽에 셀렉트 게이트를 형성하므로 ETOX 셽에서 발생하는 과 소거에 의한 문제를 해소할 수 있으며 이로 인하여 칩 오버 헤드(chip over-head)를 작게 할 수 있는 효과가 있다.

또한, 실시에는 플로팅 게이트가 소스 영역 측에 인접하도록 배치하여 프로그램 후 케이블을 끊거나 소거 후 케이블을 연결시키는 데 유리한 효과가 있다.

또한, 실시에는 플로팅 게이트 상에 하드 마스크를 적용하며, 이 하드 마스크를 이용하여 플로팅 게이트 채결, OXO 막 채결, 셀렉트 게이트 채결, 폴리실리콘 전류 페턴 제거 등의 공정을 자가 정밀로 수행함으로써 포토 공정에 의한 CD 변동 및 오경절의 리스크(risk)를 최소화할 수 있는 효과가 있다.

【발명의 실시를 위한 구체적인 내용】

실시에 따른 플라시 메모리 소자 및 제조 방법은 전부된 도면을 참조하여 상세히 설명한다.

실시에의 설명에 있어서, 각 측의 "상/위(on/over)"에 형성되는 것으로 기재되는 경우에 있어, 상/위(on/over)는 직접(directly)와 또는 다른 측을 계져하여
(indirectly) 형성되는 것을 모두 포함한다.

도면에서 각층의 두께나 크기는 설명의 편의 및 명확성을 위하여 파장되거나 생략되거나 또는 개략적으로 도시되었다. 또한 각 구성요소의 크기는 실제크기를 전적으로 반영하는 것은 아니다.

또한, 실시례를 설명함에 있어, 관련된 공지 구성 또는 기능에 대한 구체적인 설명이 본 발명의 요지를 흐릴 수 있다고 판단되는 경우에는 그 상세한 설명은 생략한다.

도 1 내지 도 9는 실시례에 따른 플래시 메모리 소자의 제조 공정을 보여주는 평면도 및 단면도들이다.

실시례는 MCS(memory Common Source) 구조뿐 아니라 SAS (self aligned Source) 구조의 적용도 가능하다.

도 1a 내지 도 8a는 실시례에 따른 플래시 메모리 소자의 제조 공정을 보여주는 평면도이고, 도 1b 내지 도 8b는 도 1a 내지 도 8a에서 1-1 '로 절단하여 보여주는 단면도들이고, 도 1c 내지 도 8c는 도 1a 내지 도 8a에서 1-1 '로 절단하여 보여주는 단면도들이다. 또한, 도 9는 실시례에 따른 플래시 메모리 소자의 일례를 보여주는 단면도이다.

도 1a, 1b 및 도 1c에 따르면, 반도체 기관(10)에 액티브 영역(Active area)을 정의하는 소자 분리막(11)을 형성한다. 상기 소자 분리막(11)은 상기 반도체 기관(10)에 소정 깊이로 트랜지스트를 식각하고, 상기 트랜지스트 내에 접연막을 형성하여 39-10
행성할 수 있다.

<36> 소자 분리막(11)이 형성된 반도체 기판(10) 상에 터널 산화막(21a)을 성장시키고, 커폴링비를 고려하여 결정된 두께만큼 제1폴리실리콘막(22a)을 생성한다.

<37> 상기 제1폴리실리콘은 추후 플로팅 게이트가 형성되며, 실시에 따르면, 플로팅 게이트의 측벽에 설렉트 게이트가 형성되므로, 상기 플로팅 게이트의 두께는 커폴링비에 직접적인 영향을 미칠 수 있다.

<38> 상기 제1폴리실리콘막(22a)은 도프트 폴리실리콘(doped polysilicon)을 사용할 수도 있고, 언-도프트 폴리실리콘(undoped polysilicon)을 중합한 다음, 후속 진행되는 소스 또는 드레인 형성을 위한 이온주입 공정에서 언-도프트 폴리실리콘을 도핑시킬 수도 있다.

<39> 상기 제1폴리실리콘막(22a) 상에 하드마스크막(23a)을 형성한다.

<40> 상기 하드마스크막(23a)은 CVD(chemical vapor deposition)을 이용하여 산화막, 산화화학 및 질화막 중 적어도 하나를 중합하여 형성할 수 있다.

<41> 도 2a, 도 2b 및 도 2c를 참조하면, 상기 하드 마스크막(23a)을 페터밍하여 하드 마스크(23)를 형성하고, 상기 하드 마스크(23)를 사용하여 제1폴리실리콘막(22a)을 페터밍함으로써 플로팅 게이트(22)를 형성한다.

<42> 상기 플로팅 게이트(22)는 각 액티브 영역마다 단독으로 아이솔레이션(isolation)된다(도 2a 참조).

<43> 상기 제1폴리실리콘막(22a)을 식각하여 플로팅 게이트(22)를 형성한 다음에

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상기 하드 마스크(23)는 제거하지 않는 것이 바람직하다.

도 2a에 표시된 붉은 점선은 추후 형성될 셜래트 케이트가 형성될 위치를 표시한 것으로, 소자와 구조 및 동작에 대한 이해를 돕기 위하여 더욱 표시하였다.

도 3a, 도 3b 및 도 3c를 참조하면, 상기 플로팅 케이트(22)가 형성된 반도체 기판(10) 전면에 ONO막(25a)을 형성한다.

상기 ONO막(25a)는 CVD법을 이용하여 산화막, 질화막 및 산화막 순서대로 쌓을 수 있다. 각각의 산화막, 질화막 및 산화막은 50~100Å 두께로 형성할 수 있다.

상기 ONO막(25a)은 셜래트 케이트에 인가되는 바이어스를 통하여 플로팅 케이트(22)에 키폴링 바이어스를 인가할 때 F-N 터널링 현상이 발생하지 않고 충분한 브레이크 다운(break down) 전압을 견딜 수 있도록 하기 위한 것이다.

케다가, 플로팅 케이트(22)에서 셜래트 케이트가 형성되는 일측과 대향하는 타측의 측면도 상기 ONO막이 형성되어 보호하므로 리텐션 측면에서 유리한 장점이 있다.

실시에는 상기 ONO막(25a) 대신, 산화막 및 질화막 중 적어도 어느 한막을 이용하여 결연막을 형성하는 구조도 포함할 수 있다.

도 4a, 도 4b 및 도 4c를 참조하면, 상기 반도체 기판(10) 및 플로팅 케이트(22)의 표면에 형성된 ONO막(25a)을 에치백(etch back)하여 상기 플로팅 케이트(22)의 측벽에 ONO 패턴(25)을 형성한다.
상기 ONO 패턴(25)은 상기 플로팅 게이트(22)의 측면을 따라 스펙터 형태로 형성되며, 플로팅 게이트(22)의 상면의 ONO막(25a), 반도체 기판(10)의 상면에 형성된 ONO막(25a)은 모두 제거된다.

이때, 상기 하드 마스크(23)는 플로팅 게이트(22) 상면에 형성되어 있으므로, 상기 ONO 패턴(25)은 측벽에 형성하기 위한 식각 공정에서 플로팅 게이트(22)를 보호하는 역할을 할 수 있다.

도 5a, 도 5b 및 도 5c를 참조하면, 로직 영역의 소자를 형성하고 선택트 게이트를 형성하기 위하여, 상기 플로팅 게이트(22) 및 ONO 패턴(25)이 형성된 반도체 기판(10) 전면에 제2플리실리콘막(30a)을 형성한다.

상기 제2플리실리콘막(30a)을 형성하기 이전에, 로직 및 선택트 트랜지스터용 게이트 산화막을 형성할 수도 있다.

이 단계에서 HTO(high temperature oxide) 등의 CVD 산화막과 혼용하여 선택트 게이트 및 ONO 패턴을 보강할 수 있는 구조로 형성할 수도 있다.

예를 들면, 플레시 설 인터 폴리 옥사이드(inter poly oxide)와 선택트 게이트의 산화막은 HTO 산화막과 열산화막을 이용하여 형성할 수 있고, 로직영역의 게이트에 대해서는 이중 두께를 갖는 열산화막을 형성할 수 있다.

이때, 플로팅 게이트(22)의 간격을 적절히 조절하여 워드 라인 방향으로는 제2플리실리콘막(30a)이 갭되어 있고, 비트 라인 방향으로는 소스 영역은 갭이 이루어지지 않고 드레인 영역은 갭이 이루어지지 않아야 한다.
즉, 비트 라인 방향에 대해서 드레인 영역 양축으로 배치되는 플로팅 게이트 (22)들은 간격이 넓고, 소스 영역 양축으로 배치되는 플로팅 게이트들은 간격을 폭
게 형성한다.

예를 들면, 제2폴리실리콘막(30a)의 두께를 2000Å으로 증가한다고 하면, 웨드 라인 방향으로 플로팅 게이트(22)의 간격, 비트 라인 방향으로 소스 영역을 사
이에 두는 플로팅 게이트(22)의 간격은 제2폴리실리콘막(30a)의 2배이하인 4000Å
이하로 형성하는 것이 바람직하며, 비트 라인 방향으로 드레인 영역을 사이에 두는
플로팅 게이트의 간격은 제2폴리실리콘막(30a)의 2배 이상인 4000Å 이상의
간격과, 드레인 콘택트 형성될 공간을 포함하여 넓게 형성하는 것이 바람직하다.

도 6a, 도 6b 및 도 6c를 참조하면, 제2폴리실리콘막(30a)을 에치백하여 셀
렉트 게이트를 형성한다.

이 에치백 공정에 의하여 상기 플로팅 게이트(22) 상면의 하드 마스크가 드
러나고, 드레인 영역의 반도체 기판(10)이 드러난다. 이때, 상기 드레인 영역 상의
터널링 산화막이 제거될 수도 있고, 제거되지 않을 수도 있다.

상기 플로팅 게이트(22) 상에 형성된 하드 마스크(23)는 상기 셀렉트 게이트
형성을 위한 제2폴리실리콘막(30a)의 에치백 공정에서 플로팅 게이트(22)를 보호하
는 역할을 수행할 수 있다.

이때, 웨드 라인 방향으로 플로팅 게이트(22) 사이의 영역, 비트 라인 방향
으로 소스 영역을 사이에 두는 플로팅 게이트(22) 사이의 영역에는 제2폴리실리콘
막(30a)이 겹쳐되어 있으므로 에치백을 하더라도 완전히 제거되지 않고 제2폴리실리콘막 잔류 패턴(30b)이 남게 된다.

반면에, 드레인 영역 상에 형성된 제2폴리실리콘막(30a)은 완전히 갭되어 있지 않으므로 완전히 제거될 수 있다.

이로써, 드레인 영역의 양측에 형성된 폴리실리콘 스페이서는 셀렉트 게이트(30)로 사용될 수 있다. 따라서, 폴딩 게이트(22)가 완전히 양각하므로 채워지더라도 셀렉트 게이트(30)에서 커런트를 조절할 수 있는 것이다.

상기 셀렉트 게이트(30)는 제2폴리실리콘막(30a)을 에치백으로 형성하여 셀렉트 게이트(30)의 갭이를 전 셀에서 공유하게 형성할 수 있으므로 포토 공정에 의한 오버레이 및 CD 변동에 따른 셀 특성의 분명한 문제를 해소할 수 있다.

도 7a, 도 7b 및 도 7c를 참조하면, 폴딩 게이트(22) 상에 포토레저스트 패턴(91)을 형성하고 폴딩 게이트(22) 상면의 하드 마스크(23)를 이용하여 비트 라인 방향으로 소스 영역을 사이에 두고 형성된 제2폴리실리콘 잔류 패턴을 제거한다. 이로써, 상기 셀렉트 게이트(30)가 스프링 게이트로 형성될 수 있다.

이때, 상기 포토레저스트 패턴(91)은 상기 제2폴리실리콘 잔류 패턴(30b)을 제거하기 위한 보조 패턴으로 설계적으로 하드 마스크를 식각보호막으로 사용하여 제2폴리실리콘 잔류 패턴(30b)은 자가 경열에 의하여 제거될 수 있다.

상기 제2폴리실리콘 잔류 패턴(30b)은 제거함으로써 위드 방향으로 드레인 영역을 사이에 두고 셀렉트 게이트(30)가 형성된다. 상기 셀렉트 게이트(30)는 위
드 방향으로 배치된 플로팅 게이트(22)들의 일측의 측벽들을 따라 형성된다.

여기서, 평면도에는 포토레지스트 패턴(91)을 도시하지 않았다.

이후, 도시하지는 않았으나, p+ 임플란트를 이용하여 LDD를 형성한다.

도 8a, 도 8b 및 도 8c를 참조하면, 기판 전면에 접연막을 형성하고 에지백 하여 상기 셀렉트 게이트(30)의 측벽 및 플로팅 게이트(22)의 측벽 상에 게이트 스페이서(40)를 형성할 수 있다.

상기 게이트 스페이서(40)는 소스 영역을 사이에 두고 배치된 플로팅 게이트(22)의 측벽 상에 형성된 ONO 패턴(25) 상에 형성될 수 있다. 상기 게이트 스페이서(40)는 드레인 영역을 사이에 두고 배치된 플로팅 게이트(22)의 측벽 상에 형성된 셀렉트 게이트(30)의 측벽 상에 형성될 수 있다.

또한, 상기 소스 영역 및 드레인 영역의 엑티브 영역에 p+ 임플란트 공정을 이용하여 소스 영역(16) 및 드레인 영역(15)을 형성할 수 있다.

즉, 인접한 플로팅 게이트(22) 사이의 엑티브 영역에 소스 영역(16)을 형성할 수 있다. 인접한 셀렉트 게이트(30) 사이의 엑티브 영역에 드레인 영역(15)을 형성할 수 있다.

상기와 같은 제조 방법에 따라 제조된 플래시 메모리 소자는 도 9에 도시된 바와 같다.

도 9를 참조하면, 플로팅 게이트(22)와 셀렉트 게이트(30)가 반도체 기판(10) 상에 수평하게 배치되며, 상기 플로팅 게이트(22)와 셀렉트 게이트(30) 사이
에는 ONO 패턴(25)이 채워져 있으며, 상기 플로팅 게이트(22)의 상면에는 하드 마스크(23)가 형성되어 있으며, 상기 플로팅 게이트(22)의 일측의 반도체 기판(10)에는 소스 영역(16)이 형성되어 있고, 상기 셀렉트 게이트(30)의 일측의 반도체 기판(10)에는 드레인 영역(15)이 형성되어 있다. 상기 플로팅 게이트(22)와 상기 반도체 기판(10) 사이에는 터널링 산화막(21a)이 형성되어 있다. 상기 플로팅 게이트(22) 및 상기 셀렉트 게이트(30)가 형성된 반도체 기판(10) 전면에 PMD(premetal dielectric)막(50)이 형성되고, 콘택을 위한 콘택홀이 형성되고, 상기 콘택홀 내에 텔스텐 등이 갈려되어 콘텍전극(60)이 형성된다. 상기 PMD막(50) 상에 금층이 바가진 후 패턴화하여 콘텍 전극(60)과 접속하는 금속배선(70)을 형성할 수 있다. 상기 금속배선(70)은 비트 라인이 될 수 있다.

상기 셀렉트 게이트(30)는 상기 플로팅 게이트(22) 및 상기 플로팅 게이트(22)상의 하드 마스크(23)의 측벽에 자가 정렬되어 형성되어, 상기 셀렉트 게이트(30)의 높이는 상기 플로팅 게이트(22) 및 상기 하드 마스크(23)의 높이에 따라 결정될 수 있고, 이 높이를 높일수록 커플링비가 높아지게 된다.

상기와 같이 자가 정렬 방법으로 형성된 셀렉트 게이트(30)는 플로팅 게이트(22)의 측벽에 존재하며 상면에는 형성되지 않으므로 빛을 방지할 수 있으며, 셀렉트 게이트(30)의 길이가 전 설에서 균일하게 형성되기 때문에 소거 전류도 항상 일정하여 신뢰성이 뛰어나다.

도 10 내지 도 12는 실시에 따른 플레시 메모리 소자의 동작을 보여주기 위한 단면도들이다.
실시에 따른 플래시 메모리 소자는 다양한 방법으로 프로그램 및 소거가 가능하며, 아래 프로그램, 소기 및 리드(read)를 설명한다.

프로그램 동작은 도 10을 참조한다.

셀렉트 게이트(30) 측, 워드 라인에 프로그램 동작시에 5V를 인가하고 소스 영역(16)에 6V를 인가하고 드레인 영역(15)에 0.5V를 인가하고, 범크(bulk)는 접지와 연결된다.

이때, 상기 드레인 영역(15)에서 소스 영역(16)으로 채널리 형성되면서 황산유학이 터널링 산화막(21a)을 통해서 풀로팅 게이트(22)로 주입되어 프로그램이 이루어지게 된다. 이를 HCI(hot carrier injection)법이라고 한다.

소기 동작은 도 11을 참조한다.

셀렉트 게이트(30) 측, 워드 라인에 소기 동작시에 -5V를 인가하고, 소스 영역(16)에 6V를 인가하고 범크(bulk)는 접지와 연결된다. 이때, 상기 드레인은 풀로팅된다.

이로써, 소스 영역(16)과 풀로팅 게이트(22) 영역 간에 BIBT(band to band tunneling)에 의하여 소거가 이루어진다.

리드 동작은 도12을 참조한다.

셀렉트 게이트(30) 측, 워드 라인에 3V를 인가하고, 소스 영역(16)에 0V를 인가하고 범크 영역은 접지와 연결된다.

리드 방법은 일반적인 드레인 리드 방법으로 소스 측에 풀로팅 게이트(22)가
비치되어 있으므로 플로팅 게이트(22)에 존재하는 전자의 유무에 따라 세널을 끝거나 연결시키는 데 유리하다. 따라서, 도 10에서 0.5V를 프로그램하였으므로, 도 12에서 드레인 영역(15)을 통해 0.5V를 리드할 수 있다.

실시에는 스플릿 게이트 구조를 재용하는 ETOX (EEPROM tunnel oxide) 셀 플래시 메모리 소자에서, 자기 정렬된 스플릿 게이트 구조를 형성함으로써 셀 커런트가 일정하고 샘간 소거 특성이 균일하여 신뢰성이 향상되는 효과가 있다.

실시에는 플로팅 게이트(22)를 높게 형성하고, 그 측벽에 셀렉트 게이트(30)를 형성함으로써 커플링비가 증가되므로 효율이 증가하는 효과가 있다.

실시에는 MCS (memory Common Source) 구조뿐만 아니라 SAS (self aligned Source) 구조의 적용도 가능한 효과가 있다.

실시에는 플로팅 게이트를 ONO가 완전히 덮고 있으므로 리텔션 특성이 좋고 신뢰성이 우수한 효과가 있다.

실시에는 포트 공정에 의하여 스플릿 게이트를 형성하지 않으므로 설명트 트랜지스터의 길이가 포트 공정의 미스 올라인에 의하여 불균일하게 결정되지 않고 설명 올라인에 의하여 형성하므로 항상 소거 VT가 일정하고 설명 커런트가 일정하여 공정 안정성이 뛰어난 효과가 있다.

실시에는 설명트 게이트의 식각을 위해 플로팅 게이트 위에 하드마스크를 적용하여 ONO 막의 상부의 녹실을 방지하고 이를 후속으로 설명트 게이트를 형성할 때 마스크로 사용하는 등 다양한으로 사용될 수 있으므로 공정이 단순하고 간단해지
는 효과가 있다.

실시에 따른 편리 베모리 소자는 커플링비에 의해 VT가 직접적으로 영향을 받는 F-N 방식이 아니라 셀렉트 게이트에 의하여 커턴트가 제한되는 구조이며 프로그램은 HCI 방식으로, 소거는 BTBT 방식을 사용하면 커플링비에 의한 VT 영향이 적으므로 공정 변동에 대하여 강건하므로 공정이 용이하고 소자 특성이 뛰어난 효과가 있다.

실시에 따른 스플릿 게이트 방식으로 플로팅 게이트의 측벽에 셀렉트 게이트를 형성하므로 ETOX 설에서 발생하는 과 소거에 의한 문제를 해소할 수 있으며, 이로 인하여 칩 오버 헤드(chip over-head)를 적게 할 수 있는 효과가 있다.

또한, 실시에는 플로팅 게이트가 소스 영역 측에 인접하도록 배치하여 프로그램 후 채널을 끝거나 소거 후 채널을 연결시키는 데 유리한 효과가 있다.

또한, 실시에는 플로팅 게이트 상에 하드 마스크를 적용하며, 이 하드 마스크를 이용하여 플로팅 게이트 식각 없음, OXO 막 식각, 셀렉트 게이트 식각, 폴리실리콘 관류 패턴 제어 등의 공정을 자가 정립으로 수행함으로써 포토 공정에 의한 CD 변동 및 오정렬의 리스크(risk)를 최소화할 수 있는 효과가 있다.

이상에서 실시에를 중심으로 설명하였으나 이는 단지 예시일 뿐 본 발명을 한정하는 것이 아니며, 본 발명이 속하는 분야의 통상의 지식을 가진 자라면 본 실시에의 본질적인 특성을 벗어나지 않는 범위에서 이상에 예시되지 않은 여러 가지의 변형과 응용이 가능함을 알 수 있을 것이다. 예를 들어, 실시에 구체적으로
나라난 각 구성 요소는 변형하여 실시할 수 있는 것이다. 그리고 이러한 변형과 응용에 관계된 차이점들은 첨부된 정부 법리에서 규정하는 본 법령의 범위에 포함되는 것으로 해석되어야 할 것이다.
【청구항 1】
반도체 기판 상에 형성된 플로팅 게이트;
상기 플로팅 게이트의 일 측벽에 자기 정렬된(self aligned) 셀렉트 게이트;
및
상기 플로팅 게이트와 상기 셀렉트 게이트 사이에 형성된 ONO 패턴을 포함하는 플래시 메모리 소자.

【청구항 2】
제 1항에 있어서.
상기 플로팅 및 상기 셀렉트 게이트들과 상기 반도체 기판 사이에 형성된 터널링 산화막을 더 포함하는 플래시 메모리 소자.

【청구항 3】
제 1항에 있어서.
상기 플로팅 게이트 상면에 형성된 하드 마스크를 더 포함하는 플래시 메모리 소자.

【청구항 4】
제 1항에 있어서.
상기 플로팅 게이트의 타 측벽 및 상기 셀렉트 게이트의 일 측벽 상부에 형성된 게이트 스페이서를 더 포함하는 플래시 메모리 소자.
【정구항 5】

제 1항에 있어서.

상기 플로팅 게이트 인근의 상기 반도체 기판에 소스 영역이 형성되고, 상기 섹레트 게이트의 인근의 상기 반도체 기판에 드레인 영역이 형성되는 것을 특징으로 하는 플레시 메모리 소자.

【정구항 6】

제 1항에 있어서.

상기 ONO 페턴은 상기 플로팅 게이트의 측벽을 둘러싸며 형성된 것을 특징으로 하는 플레시 메모리 소자.

【정구항 7】

반도체 기판 상에 형성된 플로팅 게이트 및 상기 플로팅 게이트 상면에 하드 마스크를 형성하는 단계;

상기 플로팅 게이트 및 상기 하드 마스크 측벽을 둘러싸는 ONO 페턴을 형성하는 단계;

상기 ONO 페턴 상에 형성되며, 상기 플로팅 게이트 및 상기 하드 마스크의 측벽에 형성되는 폴리실리콘 페턴을 형성하는 단계; 및

상기 폴리실리콘 페턴의 일부를 제거하여 섹레트 게이트를 형성하는 단계를 포함하는 플레시 메모리 소자의 제조 방법.
제출 연차 : 2008-12-31

【징구항 8】

제 7항에 있어서,

상기ONO 패턴을 형성하는 단계에 있어서,

상기 폴로팅 게이트 및 상기 하드 마스크가 형성된 상기 반도체 기판 상에
ONO막을 형성하는 단계; 및

상기 ONO막을 에치백하여 상기 폴로팅 게이트 및 상기 하드 마스크의 측벽에
ONO패턴을 남기는 단계를 포함하는 플래시 메모리 소자의 제조 방법.

【징구항 9】

제 7항에 있어서,

상기 폴로팅 게이트는 각 액티브 영역에 대하여 하나가 형성되며, 서로 교집
된 패턴으로 형성되는 것을 특징으로 하는 플래시 메모리 소자의 제조 방법.

【징구항 10】

제 7항에 있어서,

상기 폴리실리콘 패턴을 형성하는 단계에 있어서,

상기 반도체 기판 전면에 폴리실리콘막을 형성하는 단계;

상기 폴리실리콘막은 상기 하드 마스크가 드러나도록 에치백하여 상기 폴로
딩 게이트의 측벽에 상기 폴리실리콘 패턴을 형성하며, 인근에 배치된 폴로팅 게이
트들 사이에서 상기 폴리실리콘 패턴들이 연결된 것을 특징으로 하는 플래시 메모
리 소자의 제조 방법.
【정구항 11】

제 10항에 있어서,

상기 폴리실리콘 패턴의 일부를 제거하여 상기 셀렉트 게이트를 형성하는 단계에 있어서,

상기 제거된 폴리실리콘 패턴은 상기 인근에 배치된 플로팅 게이트들 사이에서 연결된 폴리실리콘 패턴들인 것을 특정으로 하는 플래시 메모리 소자의 제조 방법.

【정구항 12】

제 7항에 있어서,

상기 셀렉트 게이트를 형성하는 단계 이후에,

상기 반도체 기판에 절연막을 형성하고 에치백하여 상기 셀렉트 게이트의 일측 및 상기 플로팅 게이트의 일측에 게이트 스페이서를 형성하는 단계; 및

상기 반도체 기판에 불순물을 주입하여 상기 플로팅 게이트의 인근에 소스 영역 및 상기 셀렉트 게이트의 인근에 드레인 영역을 형성하는 단계를 포함하는 플래시 메모리 소자의 제조 방법.

【정구항 13】

일 반향으로 형성된 셀렉트 게이트로 이루어진 웨드 라인들;

상기 웨드 라인의 일측을 따라 서로 소정 간격 이격되어 배치된 플로팅 게이트들;
상기 플로팅 게이트들 일측에 형성된 소스 영역; 및

상기 와드 라인의 타측을 따라 상기 소스 영역과 대향하여 형성된 드레인 영역을 포함하는 플래시 메모리 소자.

【청구항 14】

제 13항에 있어서.

상기 셀렉트 게이트와 상기 플로팅 게이트 사이에 상기 플로팅 게이트의 측벽을 둘러싸도록 형성된 CMOS 패턴을 더 포함하는 플래시 메모리 소자.

【청구항 15】

제 13항에 있어서.

상기 플로팅 게이트 하부에 형성된 터널링 산화막을 더 포함하는 플래시 메모리 소자.

【청구항 16】

제 13항에 있어서.

상기 소스 영역을 사이에 두고 배치되는 상기 와드 라인들의 간격이 상기 드레인 영역을 사이에 두고 배치되는 상기 와드 라인들의 간격보다 좁은 것을 특징으로 하는 플래시 메모리 소자.

【청구항 17】

제 13항에 있어서.

상기 플로팅 게이트 상면에 산화막 및 절화막 중 적어도 하나를 포함하는 하
드 마스크가 형성된 것을 특정으로 하는 플래시 메모리 소자.

【청구항 18】

제 13항에 있어서,

상기 드레인 영역과 연결되며 상기 워드 라인과 교차하는 비트 라인을 더 포함하는 플래시 메모리 소자.

【청구항 19】

서로 소정 간격 이격되어 배치된 플로팅 게이트들을 형성하는 단계;

상기 플로팅 게이트들의 측면을 푸른색은 OXO 패턴을 형성하는 단계;

상기 플로팅 게이트들의 일측벽을 따라 서로 연결되어 일 방향으로 셀렉트 게이트로 이루어진 워드 라인을 형성하는 단계; 및

상기 플로팅 게이트들 일측에 형성된 소스 영역 및 상기 워드 라인의 타측을 따라 상기 소스 영역과 대향하는 드레인 영역을 형성하는 단계를 포함하는 플래시 메모리 소자의 제조 방법.

【청구항 20】

제 19항에 있어서,

상기 워드 라인을 형성하는 단계 이후에,

상기 플로팅 게이트 및 상기 셀렉트 게이트의 측벽에 게이트 스페이서를 형성하는 단계를 포함하는 플래시 메모리 소자의 제조 방법.
【정구항 21】

제 19항에 있어서.

상기 소스 영역을 사이에 두고 배치되는 상기 워드 라인들의 간격이 상기 드레인 영역을 사이에 두고 배치되는 상기 워드 라인들의 간격보다 좁은 것을 특정적으로 하여 플래시 메모리 소자의 제조 방법.

【정구항 22】

제 19항에 있어서.

상기 플로팅 게이트 상면에 하드 마스크가 형성된 것을 특정으로 하는 플래시 메모리 소자의 제조 방법.

【정구항 23】

제 19항에 있어서.

상기 드레인 영역과 연결되며 상기 워드 라인과 교차하는 비트 라인을 더 포함하는 플래시 메모리 소자의 제조 방법.

【도면의 간단한 설명】

<102> 도 1 내지 도 9는 실시예에 따른 플래시 메모리 소자의 제조 공정을 보여주는 평면도 및 단면도들이다.

<103> 도 10 내지 도 12는 실시예에 따른 플래시 메모리 소자의 동작을 보여주기 위한 단면도들이다.
제출 일자 : 2008-12-31
【도면】

【도 1a】

【도 1b】

【도 1c】
CONFIRMATION NO. 1570

FILING RECEIPT

23557
SALIWANCHIK LLOYD & SALIWANCHIK
A PROFESSIONAL ASSOCIATION
PO Box 142950
GAINESVILLE, FL 32614

Date Mailed: 01/06/2010

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections.

Applicant(s) 
Sung Kun Park, a aa Chungbuk, KOREA, REPUBLIC OF;

Power of Attorney: The patent practitioners associated with Customer Number 23557

Domestic Priority data as claimed by applicant

Foreign Applications
REPUBLIC OF KOREA 10-2008-0138873 12/31/2008

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper Request to Retrieve Electronic Priority Application(s) (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 01/04/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is US 12/641,410

Projected Publication Date: 07/01/2010

Non-Publication Request: No

Early Publication Request: No
PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process simplifies the filing of patent applications on the same invention in member countries, but does not result in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

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The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

- Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)
- Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)
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**Total Files Size (in bytes):** 1671397
The undersigned hereby requests the USPTO retrieve an electronic copy of each of the following foreign applications for which benefit has been claimed under 35 U.S.C. 119(a)-(d) from a foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement:

Please retrieve (check all that apply)

- [ ] The following applications originally filed in participating offices (only list the Participating Office and the Participating Office Application Number (columns 1 and 2 below)):
- [ ] The following applications originally filed in non-participating offices (must list the information for all three columns below):

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This Request to Retrieve Electronic Priority Application(s) (Request) should be filed within the later of four months from the date of filing the above-identified application claiming foreign priority, or sixteen months from the filing date of the foreign application to which priority is claimed.

This Request should be submitted concurrently with the claim for priority, or thereafter. The USPTO will not attempt to retrieve the identified priority application(s) until applicant identifies the indicated priority application(s) on the oath or declaration or an application data sheet in compliance with 37 CFR 1.63(c).

Applicants are advised to consult Private PAIR (accessed through www.uspto.gov) to assure that the retrieval has been successful. The applicant remains ultimately responsible for the submission of the certified copy of the foreign application(s) within the period set forth in 37 CFR 1.55(a) (before the U.S. application issues as a patent) if the USPTO does not timely retrieve the identified priority application(s).

I hereby declare that I have the authority to grant access to the above-identified applications.

Signature: Jeff Lloyd

Printed or Typed Name: Jeff Lloyd

Patent Attorney

Telephone Number: 352-375-8100

Date: December 18, 2009

Registration Number, if applicable: 35,589

This collection of information is required by 37 CFR 1.55(d). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process an application). Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 8 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing this form, call 1-800-PTO-9199 and select option 2.
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**Title of Invention:** FLASH MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME

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FLASH MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION


BACKGROUND

Generally, a non-volatile memory retains data even if power is switched off. Accordingly, the non-volatile memory is mainly used for data storage of a PC bias, a set-top box, a printer, and a network server. Recently, the non-volatile memory is used in a digital camera and a portable phone.

Among the non-volatile memories, an electrically erasable programmable read-only memory (EEPROM)-type flash memory device erases data of a memory cell all at once or according to a sector unit. In programming, the flash memory device generates channel hot electrons from a drain and charges the electrons in a floating gate, thereby increasing a threshold voltage of a cell transistor.

In erasing, the flash memory device generates a high voltage between a source/substrate and the floating gate to emit electrons from the floating gate such that the threshold voltage of the cell transistor can be lowered.

Recently, as high integration is rapidly performed, the reduction of a cell size is required. An EEPROM tunnel oxide cell (ETOX) currently has the smallest cell size and has an array structure in which two polysilicon patterns are stacked. A lower polysilicon pattern of the two polysilicon patterns may serve as a floating gate, and an upper polysilicon pattern may serve as a select gate.

In this structure, over-erase may occur.

In order to solve the over-erase, a cell having a split gate structure is used.

Although the over-erase has been solved by employing the split gate structure, the length of a gate of a transistor serving as the select gate may be varied by a misalignment degree, effecting an erase state due to the misalignment between the floating gate and the control gate.
Accordingly, a difference is made in current distribution. In other words, uniform characteristics are not represented between cells.

If a common source structure is used to reduce a cell size, the current of even/odd word lines arranged at each side of a source line may be varied.

As described above, when forming a gate, an erase current and a coupling ratio have variations due to a photo process and overlay variation, so that uniform erase characteristics cannot be ensured between cells, and reliability of the flash memory device is degraded.

**BRIEF SUMMARY**

An embodiment provides a flash memory device and a method of manufacturing the same, capable of representing uniform erase characteristics between cells by forming a self-aligned split gate structure in an EEPROM tunnel oxide cell (ETOX)-type flash memory device employing a split gate structure.

An embodiment provides a flash memory device and a method of manufacturing the same, capable of increasing a coupling ratio by forming a tall floating gate, and forming a select gate on a sidewall of the floating gate.

An embodiment provides a flash memory device and a method of manufacturing the same, capable of representing a constant cell current by self-aligning a select gate on a sidewall of a floating gate.

According to an embodiment, a flash memory device includes a floating gate formed on a semiconductor substrate, a select gate self-aligned on one sidewall of the floating gate, and an ONO pattern interposed between the floating gate and the select gate.

According to an embodiment, a method of manufacturing a flash memory device includes forming a floating gate on a semiconductor substrate and a hard mask on the floating gate; forming an ONO pattern on a sidewall of the floating gate and the hard mask; forming a polysilicon pattern on the ONO pattern on the sidewall of the floating gate and the hard mask; and forming a select gate by removing a portion of the polysilicon pattern.

According to an embodiment, a flash memory device includes word lines including select gates aligned in one direction; floating gates spaced apart from each other by a predetermined distance along one side of each of the word lines; a source area formed at one side of each of the
floating gates; and a drain area formed in opposition to the source area along a side of each of the
word lines.

According to an embodiment, a method of manufacturing a flash memory device includes
forming floating gates spaced apart from each other by a predetermined distance; forming an
ONO pattern on a lateral side of each of the floating gates, forming a word line including select
gates aligned in one direction along one sidewall of the floating gates while being connected to
each other; forming a source area at one side of each floating gate; and forming a drain area at
one side of the word line in opposition to the source area.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A to 9 show plan and cross-sectional views illustrating a method of
manufacturing a flash memory device according to an embodiment; and

FIGS. 10 to 12 are cross-sectional views showing the operational procedure of the flash
memory device according to an embodiment.

DETAILED DESCRIPTION

Hereinafter, embodiments a flash memory and a method of manufacturing the same will
be described in detail with reference to accompanying drawings.

In the description of embodiments, it will be understood that when a layer (or film) is
referred to as being ‘on/over’ another layer or substrate, it can be directly on another layer or
substrate, or intervening layers may also be present. Further, it will be understood that when a
layer is referred to as being ‘under/below’ another layer, it can be directly under another layer, or
one or more intervening layers may also be present. In addition, it will also be understood that
when a layer is referred to as being ‘between’ two layers, it can be the only layer between the
two layers, or one or more intervening layers may also be present.

The thickness and size of each layer shown in the drawings may be simplified or
exaggerated for the purpose of convenience or clarity. The real size of the elements may be
different from the size of elements shown in drawings.
Detailed description about well-known functions or configurations may make the subject matter of the disclosure unclear. Accordingly, hereinafter, description will be made regarding components directly related to the technical scope of the disclosure.

Embodiments are applicable to a self aligned source (SAS) structure in addition to a memory common source (MCS) structure.

FIGS. 1A, 2A, 3A, 4A, 5A, 6A, 7A, and 8A are plan views of a manufacturing process of the flash memory device according to an embodiment. FIGS. 1B, 2B, 3B, 4B, 5B, 6B, 7B, and 8B are cross-sectional views taken along line I-I’ of FIGS. (1-8)A. FIGS. 1C, 2C, 3C, 4C, 5C, 6C, 7C, and 8C are cross-sectional views taken along line II-II’ of FIGS. (1-8)A. FIG. 9 is a cross-sectional view showing the flash memory device according to an embodiment.

Referring to FIGS. 1A to 1C, an isolation layer 11 is formed in a semiconductor substrate 10 to define an active area. The isolation layer 11 may be formed by filling an insulating layer in a trench after the trench has been formed to a predetermined depth in the semiconductor substrate 10 through an etch process.

A tunnel oxide layer 21a is grown from the semiconductor substrate 10 having the isolation layer 11, and a first polysilicon layer 22a is deposited by a thickness based on a coupling ratio.

The first polysilicon layer 22a is formed as a floating gate, and a select gate is formed at a sidewall of the floating gate in accordance with an embodiment. Therefore, the thickness of the floating gate may exert a direct influence on the coupling ratio.

The first polysilicon layer 22a may include doped polysilicon. In addition, the first polysilicon layer 22a may be formed by doping undoped polysilicon through a subsequent ion implantation process of forming a source/drain after undoped polysilicon has been deposited.

A hard mask layer 23a is formed on the first polysilicon layer 22a.

The hard mask layer 23a may be formed by depositing at least one of an oxide layer, an oxynitride layer, and a nitride layer, through a chemical vapor deposition (CVD) scheme.

Referring to FIGS. 2A to 2C, a hard mask 23 is formed by patterning the hard mask layer 23a, and a floating gate 22 is formed by patterning the first polysilicon layer 22a using the hard mask 23 as an etch mask.

Floating gates 22 are isolated from each other in each active region (see FIG. 2A).
Preferably, after forming the floating gate 22 by etching the first polysilicon layer 22a, the hard mask 23 is not removed.

The dotted lines of FIG. 2A represent a position wherein a select gate is formed in a subsequent process, and is marked in FIG. 2A for the purpose of comprehension about the structure and the operation of a device.

Referring to FIGS. 3A to 3C, an ONO layer 25a is formed on the entire surface of the semiconductor substrate 10 having the floating gate 22.

The ONO layer 25a may be formed by sequentially depositing an oxide layer, a nitride layer, and an oxide layer through a CVD scheme. Each of the oxide layer, the nitride layer, and the oxide layer may be formed at a thickness of 50 Å to 100 Å.

The ONO layer 25a allows the floating gate 22 to sufficiently endure a break-down voltage without F-N tunneling when a coupling bias is applied to the floating gate 22 due to a bias that has been applied to the select gate.

The ONO layer 25a is formed at a lateral side of the floating gate 22 opposite to the select gate to protect the floating gate 22, so that advantageous effects can be obtained in terms of retention.

Instead of the ONO layer 25a, in an alternate embodiment, an insulating layer can be employed by using at least one of an oxide layer and a nitride layer.

Referring to FIGS. 4A to 4C, an etch-back process is performed with respect to the ONO layer 25a formed on the surface of the semiconductor substrate 10 and the floating gate 22, thereby forming an ONO pattern 25 at the sidewalls of the floating gate 22.

The ONO pattern 25 is formed as a spacer along the lateral sides of the floating gate 22. The ONO layer 25a is removed from the top surface of the floating gate 22 (by being removed from the top surface of the hard mask 23) and the semiconductor substrate 10.

Since the hard mask 23 remains on the top surface of the floating gate 22, the hard mask 23 protects the floating gate 22 in an etch process to form the ONO pattern 25 on the sidewalls of the floating gate 22.

Referring to FIGS. 5A to 5C, in order to form a device of a logic area and a select gate of the cell area, a second polysilicon layer 30a is formed on the entire surface of the semiconductor substrate 10 having the floating gate 22 and the ONO pattern 25.
A gate oxide layer for logic and select transistors may be formed before the second polysilicon layer 30a has been formed.

In the step of forming the gate oxide layer, a structure capable of enhancing the select gate and the ONO pattern can be formed with a CVD oxide layer such as a high temperature oxide (HTO).

For example, a flash cell inter-poly-oxide layer and an oxide layer of the select gate may be formed by using an HTO oxide layer and a thermal oxide layer. A gate of a logic area can be formed by using a thermal oxide layer having a double thickness.

The second polysilicon layer 30a is gap-filled in a word line direction while adjusting the interval between floating gates 22. In a bit line direction, the second polysilicon layer 30a is gap-filled in a source area, but not gap-filled in a drain area.

In other words, in the bit line direction, the floating gates 22 are narrowly arranged at both sides of the drain area, and widely arranged at both sides of the source area. Therefore, the second polysilicon layer 30a gap fills the narrowly arranged floating gates, but not the regions between widely arranged floating gates.

For example, when the second polysilicon layer 30a is deposited at a thickness of 2000 Å, the interval between the floating gates 22 in the word line direction and the interval between the floating gates 22 arranged at both sides of the source area in the bit-line direction preferably correspond to two times or less (4000 Å or less) the thickness of the polysilicon layer 30a. In addition, the floating gates 22 arranged at both sides of the drain area in the bit line direction preferably have the interval enough to cover two times or more (4000 Å or more) the thickness of the polysilicon layer 30a and the space for a drain contact.

Referring to FIGS. 6A to 6C, the second polysilicon layer 30a is subject to an etch-back process to form the select gate.

Through the etch-back process, the hard mask 23 on the top surface of the floating gate 22 and the semiconductor substrate 10 of the drain area are exposed. In this case, a tunneling oxide layer may be removed from the drain area, but in certain embodiments the tunneling oxide layer remains.

The hard mask 23 formed on the floating gate 22 protects the floating gate 22 from the etch-back process for the second polysilicon layer 30a performed to form the select gate.
The second polysilicon layer 30a is gap-filled between the floating gates 22 in the word line direction and between the floating gates 22 arranged at both sides of the source area in the bit line direction. For this reason, even though the etch-back process is performed, the second polysilicon layer 30a is not completely removed from the substrate (shown as remaining pattern 30b).

In addition, since the second polysilicon layer 30a is not completely gap-filled in the drain area, the second polysilicon layer 30a can be completely removed from the drain area.

Accordingly, polysilicon spacers formed at both sides of the drain area by the etch-back process can be used as the select gates 30. Therefore, even if the floating gate 22 is fully charged with positive charges, a current can be adjusted in the select gate 30.

Since the select gates 30 are formed through an etch-back process for the second polysilicon layer 30a, the select gates 30 have uniform lengths over the whole cell. Accordingly, irregular cell characteristics caused by overlay and CD variation in a photo process can be solved.

Referring to FIGS. 7A to 7C, a photoresist pattern 91 is formed on the substrate to cover word line regions, and the second polysilicon remaining patterns 30b from both sides of the source area in the bit line direction are removed using the photoresist pattern 91 as an etch mask. Accordingly, the select gate 30 may serve as a split gate.

The photoresist pattern 91 is an auxiliary pattern to remove the second polysilicon remaining pattern 30b. Substantially, the second polysilicon remaining pattern 30b may be removed through self-alignment by using the hard mask 23 as an etch passivation layer.

The select gates 30 are formed at both sides of the drain area in the word line direction by removing the second polysilicon remaining patterns 30b. Accordingly, the select gate 30 is formed on one sidewall of each of the floating gates 22 arranged in the word line direction.

The photoresist pattern 91 is not shown in the plan view of FIG. 7A.

Thereafter, although not shown, a lightly doped drain (LDD) is formed through an n-implant process.

Referring to FIGS. 8A to 8C, an insulating layer is formed on the entire surface of the semiconductor substrate 10, and gate spacers 40 are formed on sidewalls of the select gates 30 and the floating gates 22 through an etch-back process of the insulating layer.
The gate spacers 40 may be formed on the ONO pattern 25 on the sidewall of the floating gates 22 arranged at both sides of the source area. The gate spacers 40 may also be formed on the sidewall of the select gate 30 at the sidewall of the floating gates 22 arranged at both sides of the drain area.

Referring to FIG. 9, source and drain areas 16 and 15 may be formed in the active areas for the source and drain areas through an n+ implant process.

The source area 16 may be formed in the active area between the adjacent floating gates 22, and the drain area 15 may be formed in the active area between the adjacent select gates 30.

The flash memory device manufactured in the above method is shown in FIG. 9.

According to an embodiment, the floating gate 22 and the select gate 30 are horizontally arranged on the semiconductor substrate 10, and the ONO pattern 25 is interposed between the floating gate 22 and the select gate 30. The hard mask 23 is formed on the floating gate 22. The source area 16 is formed on the semiconductor substrate 10 at one side of the floating gate 30, and the drain area 15 is formed on the semiconductor substrate 10 at one side of the select gate 30 in opposition to the source area 16. The tunneling oxide layer 21a is formed between the floating gate 22 and the semiconductor substrate 10. A pre-metal dielectric (PMD) layer 50 is formed on the entire surface of the semiconductor substrate 10 having the floating gate 22 and the select gate 30. A contact hole for contact is formed, and a metal such as tungsten is gap-filled in the contact hole to form a contact electrode 60. After depositing a metal layer on the PMD layer 50, the metal layer is patterned to form a metal line 70 connected to the contact electrode 60. The metal line 70 may be for a bit line.

The select gate 30 is formed on a sidewall of the floating gate 22 and the hard mask 23 through self-alignment. The height of the select gate 30 may be determined according to the combined height of the floating gate 22 and the hard mask 23. As the height of the floating gate 22 and the hard mask 23 is increased, a coupling ratio is increased.

Since the select gate 30 formed through the self-alignment method exits on the sidewall of the floating gate 22 and does not exist on the top surface of the floating gate 22, excessive erasure can be inhibited. Since the select gates 30 have uniform lengths over the whole cell, an erasing current is also uniform, so that superior reliability can be ensured.
FIGS. 10 to 12 are cross-sectional views showing the operation of the flash memory device according to an embodiment.

The flash memory device according to an embodiment can be variously programmed an erased. Hereinafter, programming, erasing, and reading operations will be described.

A programming operation of a device according to an embodiment will be described below with reference to FIG. 10.

In the programming operation, a voltage of 5V is applied to the select gate 30 (the word line), a voltage of 6V is applied to the source area 16, a voltage of 0.5V is applied to the drain area 15, and a bulk (substrate body) is grounded.

In this case, a channel is formed from the drain area 15 to the source area 16, so that hot carriers are injected into the floating gate 22 through the tunneling oxide layer 21a, thereby achieving the programming. This is called a hot carrier injection (HCI) scheme.

The erasing operation of the device will be described below with reference to FIG. 11.

In the erasing operation, a voltage of -5V is applied to the select gate 30, that is, the word line, and a voltage of 6V is applied to the source area 16. The bulk is grounded. In this case, the drain 15 is floated.

Accordingly, the erasing operation is performed through band to band tunneling (BTBT) between the source area 16 and the floating gate 22.

The reading operation for the device will be described below with reference to FIG. 12.

A voltage of 3V is applied to the select gate 30, that is, the word line, and a voltage of 0V is applied to the source area 16. The bulk is grounded.

The reading scheme is generally known to those skilled in the art. Since the floating gate 22 is provided at the side of the source area, the channel may be advantageously connected or disconnected according to the existence of electrons of the floating gate 22. Accordingly, as shown in FIG. 10, since a voltage of 0.5V has been programmed, the voltage of 0.5V can be read through the drain area 15 as shown in FIG. 12.

According to an embodiment, a self-aligned split gate structure is formed for an EEPROM tunnel oxide cell flash memory device employing a split gate structure, so that a cell current is constant and the erasing characteristic between cells is uniform. Accordingly, the reliability can be improved.
According to an embodiment, the height of the floating gate 22 is increased, and the select gate 30 is formed at the sidewall of the floating gate 22, thereby increasing a coupling ratio. Accordingly, efficiency of the device can be improved.

Embodyments are applicable to the SAS structure in addition to the MCS structure.

According to an embodiment, an ONO layer covers sides of a floating gate, so that a superior retention characteristic and superior reliability can be ensured.

According to an embodiment, since a split gate is not formed through a photo process, the lengths of the select transistors are not irregularly formed by the misalignment of the photo process. Rather, the lengths of the select transistors are determined due to self-alignment. Accordingly, an erasing voltage (the erase threshold voltage Vt) and a cell current are constant, and superior stability can be ensured in the manufacturing process.

According to an embodiment, a hard mask is formed on a floating gate in order to perform an etch process for a select gate, thereby inhibiting an upper portion of the ONO layer between the floating gate and the select gate from being damaged. When the select gate is formed in the subsequent process, the hard mask is used as an etch mask. Accordingly, the same hard mask may be used in multiple steps, so that the manufacturing process can be simplified.

The flash memory device according to an embodiment has a structure in which a current is restricted by the select gate instead of employing an F-N scheme to exert an influence on the Vt due to a coupling ratio. Since the flash memory device according to an embodiment is programmed through an HCI scheme and erased through a BTBT scheme, the flash memory device is rarely affected by the Vt due to the coupling ratio. Accordingly, since the flash memory device has minimal variation in the manufacturing process, the manufacturing process can be easily performed, and superior characteristics of the flash memory device can be obtained.

According to the embodiment, since a select gate is formed on a sidewall of a floating gate through a split gate scheme, over-erase occurring in an ETOX cell can be solved. Accordingly, a chip over-head cost can be reduced.

In addition, according to an embodiment, since a floating gate is adjacent to a source area, a channel can be easily disconnected after programming and easily connected after erasing.

According to an embodiment, a hard mask is used on a floating gate. Etch processes for a floating gate, an ONO layer, and a select gate, and a removal process for a polysilicon remaining
pattern are performed through self-alignment using the hard mask. Accordingly, CD variation caused in a photo process and the risk of misalignment can be minimized.

Although an embodiment has been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the spirit and scope of the principles of this disclosure.
CLAIMS

What is claimed is:

1. A flash memory device comprising:
   a floating gate on a semiconductor substrate;
   a select gate self-aligned on one sidewall of the floating gate; and
   an ONO pattern interposed between the floating gate and the select gate.

2. The flash memory device of claim 1, further comprising a tunneling oxide layer
   interposed between the bottom surfaces of floating and select gates and the semiconductor
   substrate.

3. The flash memory device of claim 1, further comprising a hard mask on a top
   surface of the floating gate.

4. The floating gate of claim 1, further comprising gate spacers formed on an
   opposite sidewall to the one sidewall of the floating gate and on one sidewall of the select gate.

5. The flash memory device of claim 1, further comprising:
   a source area in the semiconductor substrate in a vicinity of a side of the floating gate
   opposite to the one sidewall of the floating gate, and
   a drain area in the semiconductor substrate in a vicinity of the select gate at a side
   opposite to the floating gate.

6. The flash memory device of claim 1, wherein the ONO pattern surrounds
   sidewalls of the floating gate.

7. A method of manufacturing a flash memory device, the method comprising:
   forming a floating gate on a semiconductor substrate and a hard mask on the floating
   gate;
forming an ONO pattern on a sidewall of the floating gate and the hard mask;
forming a polysilicon pattern on the ONO pattern on the sidewall of the floating gate and
the hard mask; and
forming a select gate by removing a portion of the polysilicon pattern.

8. The method of claim 7, wherein the forming of the ONO pattern comprises:
forming an ONO layer on the semiconductor substrate having the floating gate and the
hard mask; and
performing an etch back process for the ONO layer.

9. The method of 7, wherein forming the floating gate on the semiconductor substrate
forms one floating gate in each active region of a cell region of the semiconductor substrate,
wherein the floating gates are isolated from each other.

10. The method of claim 7, wherein the forming of the polysilicon pattern
comprises:
forming a polysilicon layer on an entire surface of the semiconductor substrate; and
performing an etch back process with respect to the polysilicon layer, thereby exposing
the hard mask and remaining the polysilicon layer on the sidewall of the floating gate,
wherein the floating gate and hard mask are formed in plurality, wherein the polysilicon
pattern is connected between closely adjacent floating gates.

11. The method of claim 10, wherein, when forming the select gate by removing the
portion of the polysilicon pattern, the portion of the polysilicon pattern removed corresponds to
the connected polysilicon pattern between the closely adjacent floating gates.

12. The method of claim 7, further comprising:
forming an insulating layer on the semiconductor substrate;
forming a gate spacer at one side of the select gate and one side of the floating gate by
performing an etch back process with respect to the insulating layer; and
forming a source area in a vicinity of the floating gate and a drain area in a vicinity of the select gate by implanting impurities into the semiconductor substrate, after forming the select gate.

13. A flash memory device comprising:
word lines including select gates aligned in one direction;
floating gates spaced apart from each other by a predetermined distance along one side of each word line;
a source area formed at one side of the floating gates disposed along each word line; and
a drain area formed in opposition to the source area along each word line at a side opposite the one side along which the floating gates are disposed.

14. The flash memory device of claim 13, further comprising an ONO pattern surrounding a sidewall of the floating gate and formed between each select gate and floating gate.

15. The flash memory device of claim 13, further comprising a tunneling oxide layer formed at a lower portion of the floating gate.

16. The flash memory device of claim 13, wherein word lines are arranged at both sides of the source area and at both sides of the drain area, wherein the word lines at both sides of the source area are spaced to have an interval narrower than an interval between the word lines at both sides of the drain area.

17. The flash memory device of claim 13, further comprising a hard mask formed on a top surface of the floating gates and including at least one of an oxide layer and a nitride layer.

18. The flash memory device of claim 13, further comprising bit lines connected to the drain area while crossing the word lines.
19. A method of manufacturing a flash memory device, the method comprising:
forming floating gates spaced apart from each other by a predetermined distance;
forming an ONO pattern surrounding lateral sides of the floating gates;
forming a word line including select gates aligned in one direction along one sidewall of
each of the floating gates while being connected to each other; and
forming a source area at one side of each floating gate, and forming a drain area at a side
of the word line in opposition to the source area.

20. The method of claim 19, further comprising a gate spacer formed at sidewalls of
the floating gates and the select gates.
ABSTRACT

Disclosed is a flash memory device and a method of manufacturing the same. The flash memory device includes a floating gate formed on a semiconductor substrate, a select gate self-aligned on one sidewall of the floating gate, and an ONO pattern interposed between the floating gate and the select gate. A self-aligned split gate structure is formed for an EEPROM tunnel oxide cell flash memory device employing a split gate structure, so that a cell current is constant and the erasing characteristic between cells is uniform, thereby improving the reliability.
DECLARATION (37 C.F.R. § 1.63) AND POWER OF ATTORNEY

As a below-named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name; and

I believe that I am the original, first, and sole inventor (if only one name is listed below), or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled FLASH MEMORY DEVICE AND METHOD FOR MANUFACTURING THE SAME, specification for which

☒ is attached hereto.
☐ was filed ________________, Serial No. ________________.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code §119 and/or §365 of any foreign application(s) for patent or inventor’s certificate listed below and have also identified any foreign application for patent or inventor’s certificate having a filing date before that of the application on which priority is claimed:

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I hereby claim priority benefits under Title 35, United States Code §119 of any provisional application(s) for patent listed below:

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I hereby claim the benefit under Title 35, United States Code, §120 and/or §365 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application(s) in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint all persons registered to practice before the Patent and Trademark Office associated with **Customer Number 23557** as my attorneys with full power of substitution and revocation to prosecute this application and all divisions and continuations thereof and to transact all business in the Patent and Trademark Office connected therewith.
## PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

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## APPLICATION AS AMENDED – PART II

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* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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