The projected patent number and issue date are specified above.

**Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)**
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 1299 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Tae-Gyu KIM, Seongnam-si, KOREA, REPUBLIC OF;
PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

or Fax
(571)-273-885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where applicable. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

34610 7590 02/02/2012
KED & ASSOCIATES, LLP
P.O. Box 8638
Reston, VA 20195

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE, address above, or being facsimile transmitted to the USPTO (571) 273-885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO. 11/835,816
FILING DATE 08/08/2007
FIRST NAMED INVENTOR Taek-Gyu KIM
ATTORNEY DOCKET NO. EZ-0001
CONFIRMATION NO. 2115

TITLE OF INVENTION: DIGITAL VIDEO RECORDER HAVING HIERARCHICAL MEMORIES AND METHOD FOR IMPLEMENTING HIERARCHICAL MEMORIES

APPL. TYPE nonprovisional
SMALL ENTITY NO
ISSUE FEE DUE $1740
PUBLICATION FEE DUE $300
PREV. PAID ISSUE FEE $0
TOTAL FEE(S) DUE $2040
DATE DUE 05/02/2012

EXAMINER HASAN, SYED Y
ART UNIT 2484
CLASS-SUBCLASS 386-046000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.253).
   □ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
   □ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Box 03-02 or more recent attached). Use of a Customer Number is required.

2. For printing on the patent front page, list
   (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
   (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

KED & Associates, LLP

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recording as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE
Humax Co., Ltd.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)
Gyeonggido, Korea

Please check the appropriate assignee category or categories (will not be printed on the patent):
□ Individual  □ Corporation or other private group entity  □ Government

4a. The following fee(s) are submitted:
   □ Issue Fee
   □ Publication Fee (No small entity discount permitted)
   □ Advance Order - # of Copies

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)
   □ A check is enclosed.
   □ Payment by credit card. (Firm ID# needs to be attached)
   □ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 16-0607. (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)
   □ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
   □ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature __________________ Date 05/01/2012

Typed or printed name David C. Oren Registration No. 38,694

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
<table>
<thead>
<tr>
<th>Application Number:</th>
<th>11835816</th>
</tr>
</thead>
<tbody>
<tr>
<td>Filing Date:</td>
<td>08-Aug-2007</td>
</tr>
<tr>
<td>Title of Invention:</td>
<td>DIGITAL VIDEO RECORDER HAVING HIERARCHICAL MEMORIES AND METHOD FOR IMPLEMENTING HIERARCHICAL MEMORIES</td>
</tr>
<tr>
<td>First Named Inventor/Applicant Name:</td>
<td>Tae-Gyu KIM</td>
</tr>
<tr>
<td>Filer:</td>
<td>David Carlton Oren/Kathy Humphries</td>
</tr>
<tr>
<td>Attorney Docket Number:</td>
<td>EZ-0001</td>
</tr>
<tr>
<td>Filed as Large Entity:</td>
<td></td>
</tr>
</tbody>
</table>

**Utility under 35 USC 111(a) Filing Fees**

<table>
<thead>
<tr>
<th>Description</th>
<th>Fee Code</th>
<th>Quantity</th>
<th>Amount</th>
<th>Sub-Total in USD($)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Basic Filing:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pages:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Claims:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Miscellaneous-Filing:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Petition:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Patent-Appeals-and-Interference:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Post-Allowance-and-Post-Issuance:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<p>| Utility Appl issue fee       | 1501     | 1        | 1740   | 1740               |
| Publ. Fee- early, voluntary, or normal | 1504     | 1        | 300    | 300                |</p>
<table>
<thead>
<tr>
<th>Description</th>
<th>Fee Code</th>
<th>Quantity</th>
<th>Amount</th>
<th>Sub-Total in USD($)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Extension-of-Time:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Miscellaneous:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Total in USD ($)</strong></td>
<td></td>
<td></td>
<td></td>
<td><strong>2040</strong></td>
</tr>
</tbody>
</table>
# Electronic Acknowledgement Receipt

<table>
<thead>
<tr>
<th>EFS ID:</th>
<th>12671380</th>
</tr>
</thead>
<tbody>
<tr>
<td>Application Number:</td>
<td>11835816</td>
</tr>
<tr>
<td>International Application Number:</td>
<td></td>
</tr>
<tr>
<td>Confirmation Number:</td>
<td>2115</td>
</tr>
<tr>
<td>Title of Invention:</td>
<td>DIGITAL VIDEO RECORDER HAVING HIERARCHICAL MEMORIES AND METHOD FOR IMPLEMENTING HIERARCHICAL MEMORIES</td>
</tr>
<tr>
<td>First Named Inventor/Applicant Name:</td>
<td>Tae-Gyu KIM</td>
</tr>
<tr>
<td>Customer Number:</td>
<td>34610</td>
</tr>
<tr>
<td>Filer:</td>
<td>David Carlton Oren/Kathy Humphries</td>
</tr>
<tr>
<td>Filer Authorized By:</td>
<td>David Carlton Oren</td>
</tr>
<tr>
<td>Attorney Docket Number:</td>
<td>EZ-0001</td>
</tr>
<tr>
<td>Receipt Date:</td>
<td>01-MAY-2012</td>
</tr>
<tr>
<td>Filing Date:</td>
<td>08-AUG-2007</td>
</tr>
<tr>
<td>Time Stamp:</td>
<td>10:59:43</td>
</tr>
<tr>
<td>Application Type:</td>
<td>Utility under 35 USC 111(a)</td>
</tr>
</tbody>
</table>

**Payment information:**

- Submitted with Payment: yes
- Payment Type: Credit Card
- Payment was successfully received in RAM: $2040
- RAM confirmation Number: 10851
- Deposit Account:          
- Authorized User:          

**File Listing:**

<table>
<thead>
<tr>
<th>Document Number</th>
<th>Document Description</th>
<th>File Name</th>
<th>File Size(Bytes)/Message Digest</th>
<th>Multi Part/.zip</th>
<th>Pages (if appl.)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Description</td>
<td>File Name</td>
<td>ID</td>
<td>Status</td>
<td>Count</td>
</tr>
<tr>
<td>---</td>
<td>------------------------------------</td>
<td>-------------</td>
<td>-------------</td>
<td>--------</td>
<td>-------</td>
</tr>
<tr>
<td>1</td>
<td>Issue Fee Payment (PTO-85B)</td>
<td>ez-1-if.pdf</td>
<td>96359</td>
<td>no</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>Fee Worksheet (S806)</td>
<td>fee-info.pdf</td>
<td>31913</td>
<td>no</td>
<td>2</td>
</tr>
</tbody>
</table>

Warnings:

Information:

Total Files Size (in bytes): 128272

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.
NOTICE OF ALLOWANCE AND FEE(S) DUE

34610 7590 02/02/2012
KED & ASSOCIATES, LLP
P.O. Box 8638
Reston, VA 20195

EXAMINER
HASAN, SYED Y

ART UNIT 2484
PAPER NUMBER

DATE MAILED: 02/02/2012

APPLICATION NO. FILING DATE FIRST NAMED INVENTOR ATTORNEY DOCKET NO. CONFIRMATION NO.
11/835,816 08/08/2007 Tae-Gyu KIM EZ-0001 2115

TITLE OF INVENTION: DIGITAL VIDEO RECORDER HAVING HIERARCHICAL MEMORIES AND METHOD FOR IMPLEMENTING HIERARCHICAL MEMORIES

APPLN. TYPE SMALL ENTITY ISSUE FEE DUE PUBLICATION FEE DUE PREV. PAID ISSUE FEE TOTAL FEE(S) DUE DATE DUE
nonprovisional NO $1740 $300 $0 $2040 05/02/2012

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.
If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:
A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.
B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or
If the SMALL ENTITY is shown as NO:
A. Pay TOTAL FEE(S) DUE shown above, or
B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee’s responsibility to ensure timely payment of maintenance fees when due.

Page 1 of 3
**PART B - FEE(S) TRANSMITTAL**

Complete and send this form, together with applicable fee(s), to: **Mail**

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

or Fax
(571)-273-2885

**KED & ASSOCIATES, LLP**
P.O. Box 8638
Reston, VA 20195

**APPLICATION NO.** 11/835,816

**FILING DATE** 08/08/2007

**FIRST NAMED INVENTOR** Tae-Gyu KIM

**ATTORNEY DOCKET NO.** EZ-0001

**CONFIRMATION NO.** 2115

**APPLICATION**

**TITLE OF INVENTION:** DIGITAL VIDEO RECORDER HAVING HIERARCHICAL MEMORIES AND METHOD FOR IMPLEMENTING HIERARCHICAL MEMORIES

<table>
<thead>
<tr>
<th>APPLN. TYPE</th>
<th>SMALL ENTITY</th>
<th>ISSUE FEE DUE</th>
<th>PUBLICATION FEE DUE</th>
<th>PREV. PAID ISSUE FEE</th>
<th>TOTAL FEE(S) DUE</th>
<th>DATE DUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>nonprovisional</td>
<td>NO</td>
<td>$1740</td>
<td>$300</td>
<td>$0</td>
<td>$2040</td>
<td>05/02/2012</td>
</tr>
</tbody>
</table>

**EXAMINER** HASAN, SYED Y

**ART UNIT** 2484

**CLASS-SUBCLASS** 386-046000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.306).
   - Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
   - "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list:
   1. the names of up to 3 registered patent attorneys or agents OR, alternatively,
   2. the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

3. **ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)**

   PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

   (A) **NAME OF ASSIGNEE**

   (B) **RESIDENCE:** (CITY and STATE OR COUNTRY)

   Please check the appropriate assignee category or categories (will not be printed on the patent):
   - [ ] Individual
   - [ ] Corporation or other private group entity
   - [ ] Government

4a. The following fee(s) are submitted:
   - Issue Fee
   - Publication Fee (No small entity discount permitted)
   - Advance Order - # of Copies

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
   - A check is enclosed.
   - Payment by credit card. Form PTO-2038 is attached.
   - The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number __________ (enclose an extra copy of this form).

5. **Change in entity status** (from status indicated above)
   - a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
   - b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

**NOTE:** The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature ________________________________

Date ________________________________

Typed or printed name ________________________________

Registration No. __________

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PTOL-85 (Rev. 02/11) Approved for use through 08/31/2013.

OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 938 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 938 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.
Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.
Notice of Allowability

Application No. 11/835,816
Applicant(s) KIM, TAE-GYU
Examiner SYED HASAN
Art Unit 2484

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 9 September 2011.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ______; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1 - 7 and 9 - 18 (renumbered 1 - 17).

4. ☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☑ All  b) ☐ Some*  c) ☐ None  of the:
      1. ☑ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. ______.
      3. ☑ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: ______.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date ______.
   b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ______.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☑ Notice of References Cited (PTO-892)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date ______
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

6. ☐ Interview Summary (PTO-413), Paper No./Mail Date ______.
7. ☐ Examiner's Amendment/Comment
8. ☑ Examiner's Statement of Reasons for Allowance
9. ☐ Other ______.

/Thai Tran/
Supervisory Patent Examiner, Art Unit 2484

U.S. Patent and Trademark Office
PTOL-37 (Rev. 03-11)
DETAILED ACTION

Allowable Subject Matter

1. Claims 1 – 7 and 9 - 18 (renumbered 1 – 17) are allowed.

2. The following is a statement of reasons for the indication of allowable subject matter:

   The present invention of claims 1 – 7 and 9 - 18 is directed to a method for playing back stream data from a digital video recorder having and implementing hierarchical memories.

   Independent claim 1 identifies the unique distinct feature “wherein the memory controller controls the audio and video streams to be moved to and stored in the non-volatile memory, when a first predetermined size of stream data in the audio and video streams are accumulated in the volatile memory, and the memory controller controls the audio and video streams to be moved to and stored in the hard disk drive when a second predetermined size of stream data in the audio and video streams are accumulated in the non-volatile memory, or an accumulation of stream data of a corresponding broadcast program is completed.”

   The closet prior art, Dorovanessian et al (US 2006/0051060) discloses a digital video recorder (para 0032) comprising: a storage unit, that includes a volatile memory (fig 3, 228, para 0032); a non-volatile memory (para 0025) and a hard disk drive (fig 3, 203, para 0032); and a memory controller (fig 3, 221, para 0032, memory controller) to control audio (para 0004) and video (para 0022) streams successively outputted from a demultiplexer (fig 3, 220, para 0031 demux) to be moved to and stored in the volatile memory(para 0031). However Dorovanessian et al fails to anticipate or render the above mentioned underlined limitations obvious.

   Hence claim 1 is allowed.
Since claims 2 - 6 are dependent on claim 1, therefore they are allowed.
Independent claim 7 identifies the unique distinct feature “wherein the memory
controller controls stream data following the stream data, stored in the volatile memory, to be
moved or copied to the non-volatile memory, and a size of the stream data stored in the
volatile memory, is large enough to be played back while the succeeding stream data are
stored in the non-volatile memory.”
Hence claim 7 is allowed.

Since claims 9 - 11 are dependent on claim 7, therefore they are allowed.
Independent claim 12 identifies the unique distinct feature “(a) moving and storing audio
and video streams, which are successively outputted from a demultiplexer, in a non-volatile
memory when a predetermined size of stream data in the audio and video streams are
accumulated in a volatile memory; and (b) when a predetermined size of stream data in the
audio and video streams are accumulated in the non-volatile memory by repeating the moving
and storing of the audio and video streams in the non-volatile memory and accumulation of
stream data of a corresponding broadcast program is completed, moving and storing the
stream data in a hard disk drive.”
Hence claim 12 is allowed.

Since claims 13 - 15 are dependent on claim 12, therefore they are allowed.
Independent claim 16 identifies the unique distinct feature “having a certain size
of stream data with an earlier playback order stored in a volatile memory, the stream
data with an earlier playback order being among stream data stored in a hard disk;
and having stream data following the stream data, which are stored in the volatile
memory, stored in a non-volatile memory; whereas the size of the stream data stored in
the volatile memory is large enough to be played back while the succeeding stream
data are stored in the non-volatile memory"

Hence claim 16 is allowed.

Since claims 17 and 18 are dependent on claim 16, therefore they are allowed.

Therefore claims 1 – 7 and 9 - 18 are allowed over prior art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Syed Y. Hasan whose telephone number is 571-270-1082. The examiner can normally be reached on 9/8/5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Thai Tran can be reached on 571-272-7382. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. Y. H./
12/14/2011

/Thai Tran/
Supervisory Patent Examiner, Art Unit 2484
<table>
<thead>
<tr>
<th>*</th>
<th>Document Number</th>
<th>Date</th>
<th>Name</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>US-2006/0051060</td>
<td>03-2006</td>
<td>Dorovanessian et al.</td>
<td>386/094</td>
</tr>
</tbody>
</table>

**FOREIGN PATENT DOCUMENTS**

<table>
<thead>
<tr>
<th>*</th>
<th>Document Number</th>
<th>Date</th>
<th>Country</th>
<th>Name</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>O</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Q</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NON-PATENT DOCUMENTS**

Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages.

* | U | V | W | X |
## Index of Claims

<table>
<thead>
<tr>
<th>Application/Control No.</th>
<th>Applicant(s)/Patent Under Reexamination</th>
</tr>
</thead>
<tbody>
<tr>
<td>11835816</td>
<td>KIM, TAE-GYU</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Examiner</th>
<th>Art Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>SYED HASAN</td>
<td>2484</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>✓</th>
<th>Rejected</th>
<th>-</th>
<th>Cancelled</th>
<th>N</th>
<th>Non-Elected</th>
<th>A</th>
<th>Appeal</th>
<th>☑</th>
<th>Claims renumbered in the same order as presented by applicant</th>
<th>CPA</th>
<th>T.D.</th>
<th>R.1.47</th>
</tr>
</thead>
<tbody>
<tr>
<td>=</td>
<td>Allowed</td>
<td>✗</td>
<td>Restricted</td>
<td>I</td>
<td>Interference</td>
<td>O</td>
<td>Objection</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CLAIM</th>
<th>DATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Final</td>
<td>Original</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>7</td>
<td>7</td>
</tr>
<tr>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>9</td>
<td>9</td>
</tr>
<tr>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>11</td>
<td>11</td>
</tr>
<tr>
<td>12</td>
<td>12</td>
</tr>
<tr>
<td>13</td>
<td>13</td>
</tr>
<tr>
<td>14</td>
<td>14</td>
</tr>
<tr>
<td>15</td>
<td>15</td>
</tr>
<tr>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>17</td>
<td>17</td>
</tr>
<tr>
<td>18</td>
<td>18</td>
</tr>
<tr>
<td>19</td>
<td>19</td>
</tr>
<tr>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>21</td>
<td>21</td>
</tr>
<tr>
<td>22</td>
<td>22</td>
</tr>
</tbody>
</table>
**Search Notes**

<table>
<thead>
<tr>
<th>Application/Control No.</th>
<th>Applicant(s)/Patent Under Reexamination</th>
</tr>
</thead>
<tbody>
<tr>
<td>11835816</td>
<td>KIM, TAE-GYU</td>
</tr>
</tbody>
</table>

**Examiner**

<table>
<thead>
<tr>
<th>Art Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>SYED Y HASAN</td>
</tr>
<tr>
<td>2484</td>
</tr>
</tbody>
</table>

---

**SEARCHED**

<table>
<thead>
<tr>
<th>Class</th>
<th>Subclass</th>
<th>Date</th>
<th>Examiner</th>
</tr>
</thead>
<tbody>
<tr>
<td>G9B</td>
<td>20.009, 27.012, 27.05</td>
<td>5/6/2011</td>
<td>Syed Y. Hasan</td>
</tr>
</tbody>
</table>

---

**SEARCH NOTES**

<table>
<thead>
<tr>
<th>Search Notes</th>
<th>Date</th>
<th>Examiner</th>
</tr>
</thead>
<tbody>
<tr>
<td>Approve Allowability: Thai Tran</td>
<td>12/13/2011</td>
<td>Syed Y. Hasan</td>
</tr>
<tr>
<td>Inventor and Interference search</td>
<td>12/14/2011</td>
<td>Syed Y. Hasan</td>
</tr>
</tbody>
</table>

---

**INTERFERENCE SEARCH**

<table>
<thead>
<tr>
<th>Class</th>
<th>Subclass</th>
<th>Date</th>
<th>Examiner</th>
</tr>
</thead>
<tbody>
<tr>
<td>386</td>
<td>213, 241, 279, 326, 334, 344</td>
<td>12/14/2011</td>
<td>Syed Y. Hasan</td>
</tr>
<tr>
<td>711</td>
<td>112, 117</td>
<td>12/14/2011</td>
<td>Syed Y. Hasan</td>
</tr>
</tbody>
</table>
**Issue Classification**

<table>
<thead>
<tr>
<th>Application/Control No.</th>
<th>Applicant(s)/Patent Under Reexamination</th>
</tr>
</thead>
<tbody>
<tr>
<td>11835816</td>
<td>KIM, TAE-GYU</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Examiner</th>
<th>Art Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>SYED HASAN</td>
<td>2484</td>
</tr>
</tbody>
</table>

**ORIGIONAL**

<table>
<thead>
<tr>
<th>CLASS</th>
<th>SUBCLASS</th>
</tr>
</thead>
<tbody>
<tr>
<td>395</td>
<td>213</td>
</tr>
</tbody>
</table>

**INTERNATIONAL CLASSIFICATION**

<table>
<thead>
<tr>
<th>CLAIMED</th>
<th>NON-CLAIMED</th>
</tr>
</thead>
<tbody>
<tr>
<td>H 0 4 N</td>
<td>H 0 4 N</td>
</tr>
</tbody>
</table>

**CROSS REFERENCE(S)**

<table>
<thead>
<tr>
<th>CLASS</th>
<th>SUBCLASS (ONE SUBCLASS PER BLOCK)</th>
</tr>
</thead>
<tbody>
<tr>
<td>386</td>
<td>241 279 326 334 344</td>
</tr>
<tr>
<td>711</td>
<td>112 117</td>
</tr>
</tbody>
</table>

**Claims renumbered in the same order as presented by applicant**

<table>
<thead>
<tr>
<th>Final</th>
<th>Original Final</th>
<th>Original Final</th>
<th>Final</th>
<th>Original Final</th>
<th>Final</th>
<th>Original Final</th>
<th>Final</th>
<th>Original Final</th>
<th>Final</th>
<th>Original Final</th>
<th>Final</th>
<th>Original Final</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>16</td>
<td>17</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>17</td>
<td>18</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>19</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td></td>
<td>20</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>5</td>
<td></td>
<td>21</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>6</td>
<td></td>
<td>22</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**(Assistant Examiner)**

**(Primary Examiner)**

**Total Claims Allowed:**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>O.G. Print Claim(s)</td>
<td>O.G. Print Figure</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
</tr>
</tbody>
</table>
In reply to the Office Action dated May 10, 2011, please amend the above-identified application as follows:

Amendments to the Specification are reflected in this paper.

Amendments to the Claims are reflected in the listing of claims.

Remarks begin after the listing of the claims.
AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph on page 14, lines 11-17 with the following amended paragraph:

The demultiplexer 220 demultiplexes various kinds of information, such as audio, video, and other data that are multiplexed in broadcast signals supplied by the tuner 210. The demultiplexer 220 also demultiplexes a broadcast program, selected in accordance with the user's selection input, among broadcast signals received through the tuner 210 and extracts the selected broadcast program to video and audio streams. The broadcast signal extracted and outputted by the demultiplexer 220 can be an MPEG data format, for example, program stream (PS) and/or partial transport stream (TS).

Please replace the paragraph on page 15, line 19-page 16, line 3 with the following amended paragraph:

The non-volatile memory [[270]]280 is slower than the memory although it is possible to read/write in block units. The non-volatile memory [[270]]280 can be, for example, a flash memory. As shown in FIG. 3, the non-volatile memory [[270]]280 can be logically partitioned into a plurality of areas. For example, the non-volatile memory can be partitioned into a buffering area 330 and an NV (non-volatile) storage area 340.
Please replace the paragraphs on page 17, line 4-page 18, line 11 with the following amended paragraphs:

In step 415, the memory controller 250 determines whether the storage space of the first VM area 310 is used up while storing the audio and video streams, successively outputted from the demultiplexer 220, in the first VM area 310 of the volatile memory 270.

If there still is storage space in the first VM area 310, step 410 is repeated to continuously store the audio and video streams, outputted from the demultiplexer 220, in the first VM area 310 of the volatile memory 270.

If the storage space of the first VM area 310 is used up, however, step 420 is performed to have the memory controller 250 store following audio and video streams in the second VM area 320. The memory controller 250 also controls the data stored in the first VM area 310 to be written in the NV storage area 340 of the non-volatile memory [[270]]280, in steps represented by 420 and 435.

As described above, the storage space of the volatile memory 270 is divided into two or more partitioned areas, and if the audio and video streams fill up the storage space of one of the partitioned areas, succeeding audio and video streams will continue to be stored in another partitioned area. While the audio and video streams are stored in another partitioned area, the data written in the partitioned area, in which the preceding audio and video streams are stored, are stored in the NV storage area 340 of the non-volatile memory [[270]]280, and once the storing is completed, the data written in the pertinent partitioned area is deleted. For example, if the volatile memory 270 consists of and sequentially use the first VM area 310 and the second
VM area 320, as shown in FIG. 3, the data written in the first VM area 310 is written in the NV storage area 340 of the non-volatile memory 280 while the audio and video streams are stored in the second VM area 320. However, all of the data written in the first VM area 310 will have to move to or be copied to the NV storage area 340 of the non-volatile memory 280 before completing the writing of the audio and video streams in the second VM area 320. If the writing of the audio and video streams is completed before the storage space of the first VM area 310 is used up, the second VM area 320 will no longer be used, and the audio and video streams written in the first VM area 310 will move to or be copied to the NV storage area 340 by the control of the memory controller 250.
AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A digital video recorder, comprising:
   
a storage unit, including that includes a volatile memory, a non-volatile memory, and a hard disk drive; and

   a memory controller, controlling to control audio and video streams successively outputted from a demultiplexer to be moved to and stored in the volatile memory, the non-volatile memory, and the hard disk drive in the order of the volatile memory, non-volatile memory, and hard disk drive

   wherein the memory controller controls the audio and video streams to be moved to and stored in the non-volatile memory when a first predetermined size of stream data in the audio and video streams are accumulated in the volatile memory, and

   the memory controller controls the audio and video streams to be moved to and stored in the hard disk drive when a second predetermined size of stream data in the audio and video streams are accumulated in the non-volatile memory, or an accumulation of stream data of a corresponding broadcast program is completed.
2. (Currently Amended) The digital video recorder of Claim 1, wherein a storage area of the volatile memory is partitioned into a plurality of volatile memory (VM) areas; each VM area successively stores audio and video streams by a designated size; and
audio and video streams stored in a VM area, the storage space of which is completely used up, are moved or copied to the non-volatile memory by the memory controller.

3. (Currently Amended) The digital video recorder of Claim 2, wherein a storage area of the non-volatile memory is allotted into a plurality of partitioned areas including a buffering area and [an] a non-volatile (NV) storage area; audio and video streams stored in the VM area are stored in the NV storage area; and
audio and video streams stored in an NV storage area, the storage space of which is completely used up, are moved or copied to the hard disk drive by the memory controller.

4. (Currently Amended) The digital video recorder of Claim 3, wherein[ , if] when the storage space of the NV storage area is completely used up, the memory controller controls the audio and video streams stored in the VM area to be stored in the buffering area while the audio and video streams are moved or copied to the hard disk drive.
5. (Currently Amended) The digital video recorder of Claim 4, wherein [[if] when the moving or copying of the audio and video streams written in the NV storage area is completed, [the]]a size of the buffering area is expanded by [[the]]a size of the NV storage area[[;]], the expanded buffering area is re-designated as a new NV storage area[[;]], and a reduced NV storage area is re-designated as a new buffering area.

6. (Original) The digital video recorder of Claim 1, wherein stream data stored in the storage unit is a PS (program stream) or a partial TS (transport stream).

7. (Currently Amended) A digital video recorder, comprising:

   a storage unit, including that includes a volatile memory, a non-volatile memory, and a hard disk drive; and

   a memory controller, controlling to control stream data with an earlier playback order being among stream data stored in the hard disk drive to be moved or copied to the volatile memory or the non-volatile memory,

   whereas a decoder decodes and outputs stream data stored in the volatile memory or the non-volatile memory

   wherein the memory controller controls stream data following the stream data, stored in the volatile memory, to be moved or copied to the non-volatile memory, and

   a size of the stream data stored in the volatile memory is large enough to be played back while the succeeding stream data are stored in the non-volatile memory.
8. (Canceled)

9. (Currently Amended) The digital video recorder of Claim [[8]]7, wherein the stream data, following the stream data written in the volatile memory, are written in the non-volatile memory.

10. (Currently Amended) The digital video recorder of Claim [8]9, wherein[[, if]] when decoding the stream data written in the volatile memory is completed, [[the]]a decoder successively decodes and outputs stream data stored in the non-volatile memory.

11. (Original) The digital video recorder of Claim 7, wherein the stream data is a PS (program stream) or a partial TS (transport stream).

12. (Currently Amended) A method for storing stream data of a digital video recorder, comprising:

   (a) moving and storing audio and video streams, which are successively outputted from a demultiplexer, in a non-volatile memory [[if]] when a predetermined size of stream data in the audio and video streams are accumulated in a volatile memory as stream data in a predetermined size; and

   (b) [[if]]when a predetermined size of stream data in a predetermined size the audio and video streams are accumulated in the non-volatile memory by repeating the above step
(a) moving and storing of the audio and video streams in the non-volatile memory, or an accumulation of stream data of a corresponding broadcast program is completed, moving and storing the stream data in a hard disk drive.

13. (Currently Amended) The method of Claim 12, wherein when a storage area of the volatile memory is divided into a first partitioned area and a second partitioned area, the step (a) moving and storing audio and video streams in the non-volatile memory comprises:

starting an accumulation of stream data in the first partitioned area;

when the storage space of the first partitioned area is completely used up, controlling the accumulated stream data to be moved to and stored in the non-volatile memory and controlling stream data for succeeding audio and video streams to be accumulated in the second partitioned area; and

when the storage space of the second partitioned area is completed used up, controlling the accumulated stream data to be moved to and stored in the non-volatile memory and controlling stream data for succeeding audio and video streams to be accumulated in the first partitioned area.

14. (Currently Amended) The method of Claim 12, wherein when a storage area of the non-volatile memory is divided into a buffering area and a non-volatile (NV) storage area, the step (b) moving and the storing the stream data in the hard disk drive comprises:

starting an accumulation of the stream data in the NV storage area; and
when the storage space of the NV storage area is completely used up, controlling the accumulated stream data to be moved to and stored in the hard disk drive and controlling succeeding stream data to be accumulated in the buffering area,

whereas, once the moving of the stream data accumulated in the NV storage area is completed, the buffering area is expanded by the storage space of the NV storage area and is re-designated as a new NV storage area, and the remaining storage space is re-designated as a new buffering area.

15. (Currently Amended) The method of Claim 14, wherein the buffering area has storage space that is sufficient to accumulate succeeding stream data while the stream data accumulated in the NV storage area are being moved and stored in the hard disk drive.

16. (Currently Amended) A method for playing back stream data of a digital video recorder, comprising:

having a certain size of stream data with an earlier playback order stored in a volatile memory, the stream data with an earlier playback order being among stream data stored in a hard disk; and

having stream data following the stream data, which are stored in the volatile memory, stored in a non-volatile memory;
whereas [the]]a size of the stream data stored in the volatile memory is large enough to be played back while the succeeding stream data are stored in the non-volatile memory.

17. (Original) The method of Claim 16, wherein a decoder controls the succeeding stream data stored in the non-volatile memory to be decoded, once decoding of the stream data stored in the volatile memory is completed.

18. (Original) The method of Claim 16, wherein the stream data is a PS (program stream) or a partial TS (transport stream).

19-22. (Canceled)
REMARKS

Claims 1-7 and 9-18 are pending in this application. By this Amendment, the specification and claims 1-5, 7, 9, 10 and 12-16 are amended and claims 8 and 19-22 are canceled without prejudice or disclaimer. Various amendments may be made for clarity and are unrelated to issues of patentability.

Applicant gratefully acknowledges the Office Action’s indication that claims 16-18 are allowed, and that claims 13, 20 and 22 contain allowable subject matter. However, as will be described below, all claims are believed to be allowable.

The Office Action rejects claims 19-22 under 35 U.S.C. §101. Claims 19-22 have been canceled. Thus, the rejection under 35 U.S.C. §101 is moot.

The Office Action rejects claims 1, 6-12 and 19 under 35 U.S.C. §102(a) by U.S. Patent Publication 2006/0051060 to Dorovanessian et al. (hereafter Dorovanessian). The Office Action also rejects claims 2-5, 14, 15 and 21 under 35 U.S.C. §103(a) over Dorovanessian in view of U.S. Patent Publication 2007/0223875 to Chung et al. (hereafter Chung). The rejections are respectfully traversed with respect to the pending claims.

Independent claim 1 recites a storage unit that includes a volatile memory, a non-volatile memory, and a hard disk drive, and a memory controller to control audio and video streams successively outputted from a demultiplexer to be moved to and stored in the volatile memory. Independent claim 1 also recites that the memory controller controls the audio and video streams to be moved to and stored in the non-volatile memory when a first predetermined size
of stream data in the audio and video streams are accumulated in the volatile memory. Independent claim 1 also recites that the memory controller controls the audio and video streams to be moved to and stored in the hard disk drive when a second predetermined size of stream data in the audio and video streams are accumulated in the non-volatile memory, or an accumulation of stream data of a corresponding broadcast program is completed.

Dorovanessian does not teach or suggest all the features of independent claim 1. More specifically, Dorovanessian does not disclose a non-volatile memory. Dorovanessian’s FIG. 3 discloses a memory 228, a hard-disk drive 203 and a DVD/RW Drive 204. The DVD/RW drive 204 does not teach or suggest a non-volatile memory and/or the features of a non-volatile memory as recited in independent claim 1.

Dorovanessian discloses that data stored in memory is unconditionally stored in a hard disk drive. This differs from features of the present specification that describe reducing the use of a hard disk. Dorovanessian does not have a configuration to reduce use of a hard disk by storing data in a non-volatile memory before data is stored in a hard disk.

For at least these reasons, Dorovanessian does not teach or suggest that the memory controller controls the audio and video streams to be moved to and stored in the non-volatile memory when a first predetermined size of stream data in the audio and video streams are accumulated in the volatile memory, and the memory controller controls the audio and video streams to be moved to and stored in the hard disk drive when a second predetermined size of stream data in the audio and video streams are accumulated in the non-volatile memory, or an accumulation of stream data of a corresponding broadcast program is completed, as recited in
independent claim 1. Chung does not teach or suggest the missing features of independent claim 1. Independent claim 1 therefore defines patentable subject matter.

Independent claim 7 recites a storage unit that includes a volatile memory, a non-volatile memory, and a hard disk drive, and a memory controller to control stream data with an earlier playback order being among stream data stored in the hard disk drive to be moved or copied to the volatile memory. Independent claim 7 also recites that the memory controller controls stream data following the stream data, stored in the volatile memory, to be moved or copied to the non-volatile memory, and a size of the stream data stored in the volatile memory is large enough to be played back while the succeeding stream data are stored in the non-volatile memory.

For at least similar reasons as set forth above, Dorovanessian does not teach or suggest all the features of independent claim 7. More specifically, Dorovanessian does not teach or suggest the features of independent claim 7 relating to a non-volatile memory. Dorovanessian does not teach or suggest that the memory controller controls stream data following the stream data, stored in the volatile memory, to be moved or copied to the non-volatile memory, and a size of the stream data stored in the volatile memory is large enough to be played back while the succeeding stream data are stored in the non-volatile memory, as recited in independent claim 7. Chung does not teach or suggest the missing features of independent claim 7. Accordingly, independent claim 7 defines patentable subject matter.

Independent claim 12 recites (a) moving and storing audio and video streams, which are successively outputted from a demultiplexer, in a non-volatile memory when a predetermined
size of stream data in the audio and video streams are accumulated in a volatile memory. Independent claim 12 also recites that (b) when a predetermined size of stream data in the audio and video streams are accumulated in the non-volatile memory by repeating the moving and storing of the audio and video streams in the non-volatile memory, or an accumulation of stream data of a corresponding broadcast program is completed, moving and storing the stream data in a hard disk drive.

For at least similar reasons as set forth above, Dorovanessian and Chung do not teach or suggest all the features of independent claim 12. More specifically, Dorovanessian does not teach or suggest the features of independent claim 12 relating to non-volatile memory. Dorovanessian also does not teach or suggest moving and storing audio and video streams in a non-volatile memory when a predetermined size of stream data in the audio and video streams are accumulated in a volatile memory. Dorovanessian also does not teach or suggest that when a predetermined size of stream data in the audio and video streams are accumulated in the non-volatile memory (by repeating the moving and storing of the audio and video streams in the non-volatile memory), or an accumulation of stream data of a corresponding broadcast program is completed, moving and storing the stream data in a hard disk drive. Chung does not teach or suggest the missing features of independent claim 12. Accordingly, independent claim 12 defines patentable subject matter.

For at least the reasons set forth above, each of independent claims 1, 7, 12 and 16 defines patentable subject matter. Each of the dependent claims depends from one of the independent claims and therefore defines patentable subject matter at least for this reason. In
addition, the dependent claims recite features that further and independently distinguish over the applied references.

**CONCLUSION**

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Favorable consideration and prompt allowance of claims 1-7 and 9-18 are earnestly solicited. If the Examiner believes that any additional changes would place the application in better condition for allowance, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,
KED & ASSOCIATES, LLP

David C. Oren
Registration No. 38,694

Correspondence Address:
P.O. Box 8638
Reston, VA 20195
703 766-3777 DCO/ah
**Date:** September 9, 2011
**Please direct all correspondence to Customer Number 34610**
**Electronic Patent Application Fee Transmittal**

<table>
<thead>
<tr>
<th>Application Number:</th>
<th>11835816</th>
</tr>
</thead>
<tbody>
<tr>
<td>Filing Date:</td>
<td>08-Aug-2007</td>
</tr>
</tbody>
</table>

**Title of Invention:** DIGITAL VIDEO RECORDER HAVING HIERARCHICAL MEMORIES AND METHOD FOR IMPLEMENTING HIERARCHICAL MEMORIES

<table>
<thead>
<tr>
<th>First Named Inventor/Applicant Name:</th>
<th>Tae-Gyu KIM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Filer:</td>
<td>David Carlton Oren/Kathy Humphries</td>
</tr>
<tr>
<td>Attorney Docket Number:</td>
<td>EZ-0001</td>
</tr>
</tbody>
</table>

Filed as Large Entity

**Utility under 35 USC 111(a) Filing Fees**

<table>
<thead>
<tr>
<th>Description</th>
<th>Fee Code</th>
<th>Quantity</th>
<th>Amount</th>
<th>Sub-Total in USD($)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Basic Filing:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pages:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Claims:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Miscellaneous-Filing:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Petition:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Patent-Appeals-and-Interference:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Post-Allowance-and-Post-Issuance:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Extension-of-Time:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Extension - 1 month with $0 paid | 1251 | 1 | 130 | 130 |
<table>
<thead>
<tr>
<th>Description</th>
<th>Fee Code</th>
<th>Quantity</th>
<th>Amount</th>
<th>Sub-Total in USD($)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Miscellaneous:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Total in USD ($)</th>
<th>130</th>
</tr>
</thead>
</table>
### Electronic Acknowledgement Receipt

<table>
<thead>
<tr>
<th>EFS ID:</th>
<th>10916927</th>
</tr>
</thead>
<tbody>
<tr>
<td>Application Number:</td>
<td>11835816</td>
</tr>
<tr>
<td>International Application Number:</td>
<td></td>
</tr>
<tr>
<td>Confirmation Number:</td>
<td>2115</td>
</tr>
<tr>
<td>Title of Invention:</td>
<td>DIGITAL VIDEO RECORDER HAVING HIERARCHICAL MEMORIES AND METHOD FOR IMPLEMENTING HIERARCHICAL MEMORIES</td>
</tr>
<tr>
<td>First Named Inventor/Applicant Name:</td>
<td>Tae-Gyu KIM</td>
</tr>
<tr>
<td>Customer Number:</td>
<td>34610</td>
</tr>
<tr>
<td>Filer:</td>
<td>David Carlton Oren/Kathy Humphries</td>
</tr>
<tr>
<td>Filer Authorized By:</td>
<td>David Carlton Oren</td>
</tr>
<tr>
<td>Attorney Docket Number:</td>
<td>EZ-0001</td>
</tr>
<tr>
<td>Receipt Date:</td>
<td>09-SEP-2011</td>
</tr>
<tr>
<td>Filing Date:</td>
<td>08-AUG-2007</td>
</tr>
<tr>
<td>Time Stamp:</td>
<td>16:29:43</td>
</tr>
<tr>
<td>Application Type:</td>
<td>Utility under 35 USC 111(a)</td>
</tr>
</tbody>
</table>

### Payment information:

- Submitted with Payment: yes
- Payment Type: Credit Card
- Payment was successfully received in RAM: $130
- RAM confirmation Number: 3522
- Deposit Account: 
- Authorized User: 

### File Listing:

<table>
<thead>
<tr>
<th>Document Number</th>
<th>Document Description</th>
<th>File Name</th>
<th>File Size(Bytes)/Message Digest</th>
<th>Multi Part/.zip</th>
<th>Pages (if appl.)</th>
</tr>
</thead>
</table>
### Document Description/PDF files in .zip description

<table>
<thead>
<tr>
<th>Document Description</th>
<th>Start</th>
<th>End</th>
</tr>
</thead>
<tbody>
<tr>
<td>Miscellaneous Incoming Letter</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Extension of Time</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Amendment/Req. Reconsideration-After Non-Final Reject</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Specification</td>
<td>4</td>
<td>6</td>
</tr>
<tr>
<td>Claims</td>
<td>7</td>
<td>13</td>
</tr>
<tr>
<td>Applicant Arguments/Remarks Made in an Amendment</td>
<td>14</td>
<td>18</td>
</tr>
</tbody>
</table>

### Warnings:

### Information:

| 2 | Fee Worksheet (S806)                                                     | fee-info.pdf | 30255     | no | 2 |

### Warnings:

### Information:

Total Files Size (in bytes): 663368

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Docket No.: EZ-0001

In re Application of

Tae-Gyu KIM

Serial No: 11/835,816

Filed: August 8, 2007

For: DIGITAL VIDEO RECORDER HAVING HIERARCHICAL MEMORIES AND METHOD FOR IMPLEMENTING HIERARCHICAL MEMORIES

Confirmation No.: 2115
Group Art Unit: 2484
Examiner: Syed Y. HASAN
Customer No.: 34610

Dear Sir:

Transmitted herewith is an Amendment and/or Reply in the above identified application.

☐ No additional fee is required.
☒ Also attached: Petition for Extension of Time

The fee has been calculated as shown below:

<table>
<thead>
<tr>
<th>NO. OF CLAIMS</th>
<th>HIGHEST PREVIOUSLY PAID FOR</th>
<th>EXTRA CLAIMS</th>
<th>RATE</th>
<th>FEE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Claims</td>
<td>17</td>
<td>22</td>
<td>0</td>
<td>x $52.00 =</td>
</tr>
<tr>
<td>Independent Claims</td>
<td>4</td>
<td>6</td>
<td>0</td>
<td>x 220.00=</td>
</tr>
</tbody>
</table>

If multiple claims newly presented, add $390.00
Fee for extension of time $130.00

TOTAL FEE DUE $130.00

☒ Please charge my Credit Card.

☒ The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 16-0607, including any filing fees under 37 C.F.R. 1.16 for presentation of extra claims and any patent application processing fees under 37 C.F.R. 1.17.

Respectfully submitted,
KEND & ASSOCIATES, LLP

David C. Oren
Registration No. 38,694

Correspondence Address:
P.O. Box 8638
Reston, VA 20195
(703) 766-3777 DCO/kah
Date: September 9, 2011

Please direct all correspondence to Customer Number 34610
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Tae-Gyu KIM

Confirmation No.: 2115

Group Art Unit: 2484

Serial No.: 11/835,816

Examiner: Syed Y. HASAN

Filed: August 8, 2007

Customer No.: 34610

For: DIGITAL VIDEO RECORDER HAVING HIERARCHICAL MEMORIES AND METHOD FOR IMPLEMENTING HIERARCHICAL MEMORIES

PETITION FOR EXTENSION OF TIME UNDER 37 C.F.R. §1.136(a)(1)

U.S. Patent and Trademark Office
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, Virginia 22314

Sir:

Applicant petitions the Commissioner of Patents and Trademarks to extend the time for response to the Office Action dated May 10, 2011 for one month.

Please charge our credit card including the amount of $130.00 for the extension of time under 37 C.F.R. §1.17(a). Any deficiency or overpayment should be charged or credited to Deposit Account No. 16-0607.

Respectfully submitted,
KED & ASSOCIATES, LLP

David C. Oren
Registration No. 38,694

Correspondence Address:
P.O. Box 8638
Reston, VA 20195
703 766-3777 DCO/iah

Date: September 9, 2011
Please direct all correspondence to Customer Number 34610
PATENT APPLICATION FEE DETERMINATION RECORD
Substitute for Form PTO-875
Application No. 11/835,816
Filing Date 08/08/2007
To be Mailed

APPLICATION AS FILED – PART I
(Column 1) (Column 2) SMALL ENTITY OR OTHER THAN SMALL ENTITY

- BASIC FEE (37 CFR 1.16(a), (b), or (c))
  - NUMBER FILED
  - NUMBER EXTRA
  - RATE ($) FEE ($)
  - RATE ($) FEE ($)
- SEARCH FEE (37 CFR 1.16(b), (i), or (m))
  - N/A
  - N/A
  - N/A
  - N/A
- EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))
  - N/A
  - N/A
  - N/A
  - N/A
TOTAL CLAIMS (37 CFR 1.16(i))
  - minus 20 = 
  - X $ = OR
  - X $ =
INDEPENDENT CLAIMS (37 CFR 1.16(h))
  - minus 3 = 
  - X $ = OR
  - X $ =

APPLICATION SIZE FEE (37 CFR 1.16(e))
If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))

TOTAL

APPLICATION AS AMENDED – PART II
(Column 1) (Column 2) (Column 3) SMALL ENTITY OR OTHER THAN SMALL ENTITY

09/09/2011 CLAIMS REMAINING AFTER AMENDMENT HIGHEST NUMBER PREVIOUSLY PAID FOR PRESENT EXTRA
Total (37 CFR 1.16(i))
  - 17 Minus ** 22 = 0
  - X $ = OR
  - X $ =
Independent (37 CFR 1.16(h))
  - 4 Minus *** 6 = 0
  - X $ = OR
  - X $ =

Application Size Fee (37 CFR 1.16(e))
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))

TOTAL ADD'L FEE OR TOTAL ADD'L FEE

CLAIMS REMAINING AFTER AMENDMENT HIGHEST NUMBER PREVIOUSLY PAID FOR PRESENT EXTRA
Total (37 CFR 1.16(i))
  - Minus **
  - X $ = OR
  - X $ =
Independent (37 CFR 1.16(h))
  - Minus ***
  - X $ = OR
  - X $ =

Application Size Fee (37 CFR 1.16(e))
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))

TOTAL ADD'L FEE OR TOTAL ADD'L FEE

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the “Highest Number Previously Paid For” in this space is less than 20, enter "20".
*** If the “Highest Number Previously Paid For” in this space is less than 3, enter "3".

The “Highest Number Previously Paid For” (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner: KATRINA HARLING

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.
<table>
<thead>
<tr>
<th>APPLICATION NO.</th>
<th>FILING DATE</th>
<th>FIRST NAMED INVENTOR</th>
<th>ATTORNEY DOCKET NO.</th>
<th>CONFIRMATION NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>11/835,816</td>
<td>08/08/2007</td>
<td>Tae-Gyu KIM</td>
<td>EZ-0001</td>
<td>2115</td>
</tr>
</tbody>
</table>

34610 7890 05/10/2011
KED & ASSOCIATES, LLP
P.O. Box 8638
Reston, VA 20195

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.
Office Action Summary

Application No. 11/835,816
Applicant(s) KIM, TAE-GYU
Examiner SYED Y. HASAN
Art Unit 2484

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) □ Responsive to communication(s) filed on ___.
   2a) □ This action is FINAL.
   2b) □ This action is non-final.
   3) □ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) □ Claim(s) 1 - 22 is/are pending in the application.
   4a) Of the above claim(s) _____ is/are withdrawn from consideration.
   5) □ Claim(s) 16 - 18 is/are allowed.
   6) □ Claim(s) 1 - 12, 14, 15 and 19 - 22 is/are rejected.
   7) □ Claim(s) 13 is/are objected to.
   8) □ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) □ The specification is objected to by the Examiner.
10) □ The drawing(s) filed on _____ is/are: a) □ accepted or b) □ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) □ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) □ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) □ All   b) □ Some *   c) □ None of:
   1. □ Certified copies of the priority documents have been received.
   2. □ Certified copies of the priority documents have been received in Application No. _____.
   3. □ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) □ Notice of References Cited (PTO-892)
2) □ Notice of Draftsman’s Patent Drawing Review (PTO-948)
3) □ Information Disclosure Statement(s) (PTO/SB/08)
   Paper No(s)/Mail Date 9/1/2009.
4) □ Interview Summary (PTO-413)
   Paper No(s)/Mail Date _____.
5) □ Notice of Informal Patent Application
6) □ Other: ____.
DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

   Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent thereof, subject to the conditions and requirements of this title.

   The USPTO “Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility ”(Official Gazette notice of 22 November 2005), Annex IV reads as follows:

   Claims that recite nothing but the physical characteristics of a form of energy, such as a frequency, voltage, or the strength of a magnetic field, define energy or magnetism, per se, and as such are nonstatutory natural phenomena. O’Reilly, 56 U.S. (15 How.) at 112-14. Moreover, it does not appear that a claim reciting a signal encoded with functional descriptive material falls within any of the categories of patentable subject matter set forth in Sec. 101.

   … a signal does not fall within one of the four statutory classes of Sec. 101
   … signal claims are ineligible for patent protection because they do not fall within any of the four statutory classes of Sec. 101.

   Claim 19 - 22 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter as follows.

   Claims 19 - 22 define “recorded medium” with descriptive material. While “functional descriptive material” may be claimed as a statutory product (i.e., a “manufacture”) while embodied on a tangible computer readable medium, recording
medium embodying that same functional descriptive material is neither a process nor a product (i.e., a tangible “thing”) and therefore does not fall within one of the four statutory class of §101. Rather, “medium” is a form of energy, in the absence of any physical structure or tangible material.

When nonfunctional descriptive material is recorded on some computer-readable medium, in a computer or on an electromagnetic carrier signal, it is not statutory since no requisite functionality is present to satisfy the practical application requirement. Merely claiming nonfunctional descriptive material, i.e., abstract ideas, stored on a computer-readable medium, in a computer, or on an electromagnetic carrier signal.

Examiner recommends either cancelling the claim or adding language to the claim that makes this claim statutory, e.g. “non-transitory recorded medium”

This claim language needs to be supported by the specification.

**Claim Rejections - 35 USC § 102**

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

   A person shall be entitled to a patent unless –

   (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1, 6 – 12 and 19 are rejected under 35 U.S.C. 102 (a) as being anticipated by Dorovanessian et al (US 2006/0051060).

   Regarding claim 1, Dorovanessian et al discloses a digital video recorder (para 0032, DVR) comprising:
a storage unit, including

a volatile memory, (fig 3, 228, para 0032, memory)

a non-volatile memory (para 0025, DVD-R/W) and

a hard disk drive (fig 3, 203, para 0032, hard disk drive); and

a memory controller (fig 3, 221, para 0032, memory controller) controlling audio (para 0004) and video (para 0022) streams successively outputted from a demultiplexer (fig 3, 220, para 0031 demux) to be moved to and stored in the volatile memory, the non-volatile memory, and the hard disk drive in the order of the volatile memory, non-volatile memory, and hard disk drive (para 0031, Processor 224 of MPEG decoder 202 controls demux 220 to send recording data to memory 228 via memory controller 221) while stream data are moved or copied to the non-volatile memory (para 0031, The packetized data is then sent via coupling 253 to hard disk drive 203 wherein a first digital copy of the encoded MPEG data is stored.)

Regarding claim 6, Dorovanessian et al discloses the digital video recorder, wherein the stream data is a PS (program stream) or a partial TS (transport stream) (para 0040 transport stream)

Regarding claim 7, Dorovanessian et al discloses a digital video recorder (para 0032, DVR) comprising:

a storage unit, including a volatile memory (fig 3, 228, para 0032, memory) a non-volatile memory (para 0025, DVD-R/W) and a hard disk drive (fig 3, 203, para 0032, hard disk drive); and

a memory controller (fig 3, 221, para 0032, memory controller) controlling stream
data stored in the hard disk drive to be moved or copied to the volatile memory or the non-volatile memory, whereas a decoder (fig 3, 202, para 0031, decoder) decodes and outputs stream data stored in the volatile memory or the non-volatile memory (para 0032).

Regarding **claim 8**, Dorovanessian et al discloses the digital video recorder, wherein the memory controller moves or copies stream data in the size that can be decoded and played back by the decoder to the volatile memory (para 0031, Processor 224 of MPEG decoder 202 controls demux 220 to send recording data to memory 228 via memory controller 221) while stream data are moved or copied to the non-volatile memory (para 0031, The packetized data is then sent via coupling 253 to hard disk drive 203 wherein a first digital copy of the encoded MPEG data is stored.)

Regarding **claim 9**, Dorovanessian et al discloses the digital video recorder, wherein stream data, following the stream data written in the volatile memory, are written in the non-volatile memory (para 0031, Processor 224 of MPEG decoder 202 controls demux 220 to send recording data to memory 228 via memory controller 221. For clarity, the connections between memory controller 221 and other components of MPEG decoder 202 have been omitted. Processor 224 also controls memory controller to send the packetized data to an IDE interface 227 via bus 262. The packetized data is then sent via coupling 253 to hard disk drive 203 wherein a first digital copy of the encoded MPEG data is stored.)

Regarding **claim 10**, Dorovanessian et al discloses the digital video recorder, wherein, if decoding the stream data written in the volatile memory is completed, the
decoder successively decodes and outputs stream data stored in the non-volatile memory (para 0031, Processor 224 of MPEG decoder 202 controls demux 220 to send recording data to memory 228 via memory controller 221. For clarity, the connections between memory controller 221 and other components of MPEG decoder 202 have been omitted. Processor 224 also controls memory controller to send the packetized data to an IDE interface 227 via bus 262. The packetized data is then sent via coupling 253 to hard disk drive 203 wherein a first digital copy of the encoded MPEG data is stored.)

Regarding **claim 11**, Dorovanessian et al discloses the digital video recorder, wherein the stream data is a PS (program stream) or a partial TS (transport stream) (para 0040 transport stream)

**Claims 12 and 19** are rejected based on claim 1 above.

**Claim Rejections - 35 USC § 103**

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Regarding **claim 2**, Dorovanessian et al discloses the digital video recorder wherein video streams are moved or copied to the non-volatile memory by the memory controller (see claim 1 above) except for wherein a storage area of the volatile memory is partitioned into a plurality of VM areas; each VM area successively stores audio and video streams by a designated size; and audio and video streams stored in a VM area, the storage space of which is completely used up

However Chung et al teaches wherein a storage area of the volatile memory is partitioned into a plurality of VM areas; each VM area successively stores audio and video streams by a designated size; and audio and video streams stored in a VM area, the storage space of which is completely used up (para 0019)

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate wherein a storage area of the volatile memory is partitioned into a plurality of VM areas; each VM area successively stores audio and video streams by a designated size; and audio and video streams stored in a VM area, the storage space of which is completely used up as taught by Chung et al in the system of Dorovanessian et al in order to provide less effort and time for I/O accessing and improve I/O performance.

Regarding **claim 3**, Dorovanessian et al discloses the digital video recorder wherein moved or copied to the hard disk drive by the memory controller (see claim 2
above) except for wherein a storage area of the non-volatile memory is allotted into a plurality of partitioned areas including a buffering area and an NV storage area; audio and video streams stored in the VM area are stored in the NV storage area; and audio and video streams stored in an NV storage area, the storage space of which is completely used up.

However Chung et al teaches wherein a storage area of the non-volatile memory is allotted into a plurality of partitioned areas including a buffering area and an NV storage area; audio and video streams stored in the VM area are stored in the NV storage area; and audio and video streams stored in an NV storage area, the storage space of which is completely used up (para 0019).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate wherein a storage area of the non-volatile memory is allotted into a plurality of partitioned areas including a buffering area and an NV storage area; audio and video streams stored in the VM area are stored in the NV storage area; and audio and video streams stored in an NV storage area, the storage space of which is completely used up as taught by Chung et al in the system of Dorovanessian et al in order to provide less effort and time for I/O accessing and improve I/O performance.

Regarding claim 4, Dorovanessian et al discloses the digital video recorder while the audio and video streams are moved or copied to the hard disk drive (see claim 3 above) except for wherein, if the storage space of the NV storage area is completely used up, the memory controller controls the audio and video streams stored in the VM area to be stored in the buffering area.
However Chung et al teaches wherein, if the storage space of the NV storage area is completely used up, the memory controller controls the audio and video streams stored in the VM area to be stored in the buffering area (para 0019).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate wherein, if the storage space of the NV storage area is completely used up, the memory controller controls the audio and video streams stored in the VM area to be stored in the buffering area as taught by Chung et al in the system of Dorovanessian et al in order to provide less effort and time for I/O accessing and improve I/O performance.

Regarding claim 5, Dorovanessian et al discloses the digital video recorder wherein, if the moving or copying of the audio and video streams written in the NV storage area is completed (see claim 4 above) except for wherein, the size of the buffering area is expanded by the size of the NV storage area; the expanded buffering area is re-designated as a new NV storage area; and a reduced NV storage area is re-designated as a new buffering area.

However Chung et al teaches wherein, the size of the buffering area is expanded by the size of the NV storage area; the expanded buffering area is re-designated as a new NV storage area; and a reduced NV storage area is re-designated as a new buffering area (para 0019).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate wherein, the size of the buffering area is expanded by the size of the NV storage area; the expanded buffering area is re-designated as a new NV
storage area; and a reduced NV storage area is re-designated as a new buffering area as taught by Chung et al in the system of Dorovanessian et al in order to provide less effort and time for I/O accessing and improve I/O performance.

Regarding claim 15, Dorovanessian et al discloses the method (see claims 12 and 14 above) except for wherein the buffering area has storage space that is sufficient to accumulate succeeding stream data while the stream data accumulated in the NV storage area are being moved and stored in the hard disk drive.

However Chung et al teaches wherein the buffering area has storage space that is sufficient to accumulate succeeding stream data while the stream data accumulated in the NV storage area are being moved and stored in the hard disk drive (para 0019)

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate wherein the buffering area has storage space that is sufficient to accumulate succeeding stream data while the stream data accumulated in the NV storage area are being moved and stored in the hard disk drive as taught by Chung et al in the system of Dorovanessian et al in order to provide less effort and time for I/O accessing and improve I/O performance.

Claims 14 and 21 are rejected based on claims 3 and 5 above.

Allowable Subject Matter

6. Claims 16 – 18 are allowed

The present invention of claims 16 - 18 is directed to a method for playing back stream data of a digital video recorder

Independent claim 16 identifies the unique distinct feature “having a certain size
of stream data with an earlier playback order stored in a volatile memory, the stream
data with an earlier playback order being among stream data stored in a hard disk;
and having stream data following the stream data, which are stored in the volatile
memory, stored in a non-volatile memory whereas the size of the stream data stored in
the volatile memory is large enough to be played back while the succeeding stream
data are stored in the non-volatile memory”

The closest prior art Dorovanessian et al (US 2006/0051060) and Chung et al
(U.S 2007/0223875) disclose the digital video recorder (see claims 1 and 2 above) but
fails to anticipate or render the above mentioned underlined limitations obvious.

Hence claim 16 is allowed.

Since claims 17 and 18 are dependent on claim 16, therefore they are also
allowed.

7. Claim 13 is objected as being dependent on a rejected base claim, but would be
allowable if rewritten in independent form including all of the limitations of the base
claim and any intervening claims.

Regarding claim 13, the prior art of record fails to teach, disclose or fairly
suggest as recited in claim 13, the prior art fails to disclose the digital video recorder,
“wherein, if a storage area of the volatile memory is divided into a first partitioned area
and a second partitioned area, the step (a) comprises: starting an accumulation of
stream data in the first partitioned area; if the storage space of the first partitioned area
is completely used up, controlling the accumulated stream data to be moved to and
stored in the non-volatile memory and controlling stream data for succeeding audio and
video streams to be accumulated in the second partitioned area; and if the storage space of the second partitioned area is completed used up, controlling the accumulated stream data to be moved to and stored in the non-volatile memory and controlling stream data for succeeding audio and video streams to be accumulated in the first partitioned area.”

8. Claim 20 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and amended to overcome the rejection(s) under 35 U.S.C. 101.

Regarding claim 20, the prior art of record fails to teach, disclose or fairly suggest as recited in claim 20, the prior art fails to disclose the digital video recorder, “wherein, if a storage area of the volatile memory is divided into a first partitioned area and a second partitioned area, the step (a) comprises: starting an accumulation of stream data in the first partitioned area; if the storage space of the first partitioned area is completely used up, controlling the accumulated stream data to be moved to and stored in the non-volatile memory and controlling stream data for succeeding audio and video streams to be accumulated in the second partitioned area; and if the storage space of the second partitioned area is completed used up, controlling the accumulated stream data to be moved to and stored in the non-volatile memory and controlling stream data for succeeding audio and video streams to be accumulated in the first partitioned area”

9. Claims 22 would be allowable if amended to overcome the rejection(s) under 35 U.S.C. 101 rejection set forth in this Office action.
Regarding claim 22, the prior art of record fails to teach, disclose or fairly suggest as recited in claim 22, the prior art fails to disclose the digital video recorder
“having a certain size of stream data with an earlier playback order stored in a volatile memory, the stream data with an earlier playback order being among stream data stored in a hard disk; and having stream data following the stream data, which are stored in the volatile memory, stored in a non-volatile memory, whereas the size of the stream data stored in the volatile memory is large enough to be played back while the succeeding stream data are stored in the non-volatile memory.”

**Conclusion**

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Syed Y. Hasan whose telephone number is 571-270-1082. The examiner can normally be reached on 9/8/5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Thai Tran can be reached on 571-272-7382. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. Y. H./
05/06/2011

/Thai Tran/
Supervisory Patent Examiner, Art Unit 2484
### U.S. PATENT DOCUMENTS

<table>
<thead>
<tr>
<th>*</th>
<th>Document Number</th>
<th>Date</th>
<th>Name</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>US-2006/0051060</td>
<td>03-2006</td>
<td>Dorovanessian et al.</td>
<td>386/094</td>
</tr>
<tr>
<td>C</td>
<td>US-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>US-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>US-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F</td>
<td>US-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>G</td>
<td>US-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>US-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I</td>
<td>US-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>J</td>
<td>US-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>K</td>
<td>US-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>US-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M</td>
<td>US-</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### FOREIGN PATENT DOCUMENTS

<table>
<thead>
<tr>
<th>*</th>
<th>Document Number</th>
<th>Date</th>
<th>Country</th>
<th>Name</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>O</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Q</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### NON-PATENT DOCUMENTS

<table>
<thead>
<tr>
<th>*</th>
<th>Document Number</th>
<th>Date</th>
<th>Country</th>
<th>Name</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>U</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>W</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)*

Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.
** BIB DATA SHEET **

** CONFIRMATION NO. 2115 **

<table>
<thead>
<tr>
<th>SERIAL NUMBER</th>
<th>FILING or 371(c) DATE</th>
<th>CLASS</th>
<th>GROUP ART UNIT</th>
<th>ATTORNEY DOCKET NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>11/835,816</td>
<td>08/08/2007</td>
<td>386</td>
<td>2484</td>
<td>EZ-0001</td>
</tr>
</tbody>
</table>

**APPLICANTS**
Tae-Gyu KIM, Seongnam-si, KOREA, REPUBLIC OF;

** CONTINUING DATA ***********************

** FOREIGN APPLICATIONS **********************
REPUBLIC OF KOREA 10-2006-0075348 08/09/2006

** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **
08/24/2007

<table>
<thead>
<tr>
<th>Foreign Priority claimed</th>
<th>Yes</th>
<th>No</th>
<th>Met after Allowance</th>
<th>STATE OR COUNTRY</th>
<th>SHEETS DRAWINGS</th>
<th>TOTAL CLAIMS</th>
<th>INDEPENDENT CLAIMS</th>
</tr>
</thead>
<tbody>
<tr>
<td>35 USC 119(a-d) conditions met</td>
<td>Yes</td>
<td>No</td>
<td></td>
<td>KOREA, REPUBLIC OF</td>
<td>5</td>
<td>22</td>
<td>6</td>
</tr>
</tbody>
</table>

** ADDRESS **
KED & ASSOCIATES, LLP
P.O. Box 8638
Reston, VA 20195
UNITED STATES

** TITLE **
DIGITAL VIDEO RECORDER HAVING HIERARCHICAL MEMORIES AND METHOD FOR IMPLEMENTING HIERARCHICAL MEMORIES

** FILING FEE RECEIVED **
1700

FEES: Authority has been given in Paper No. _______ to charge/credit DEPOSIT ACCOUNT No. _______ for following:

☐ All Fees
☐ 1.16 Fees (Filing)
☐ 1.17 Fees (Processing Ext. of time)
☐ 1.18 Fees (Issue)
☐ Other __________________
☐ Credit
**Search Notes**

**Application/Control No.**
11835816

**Applicant(s)/Patent Under Reexamination**
KIM, TAE-GYU

**Examiner**
SYED Y HASAN

**Art Unit**
2484

---

**SEARCHED**

<table>
<thead>
<tr>
<th>Class</th>
<th>Subclass</th>
<th>Date</th>
<th>Examiner</th>
</tr>
</thead>
<tbody>
<tr>
<td>G9B</td>
<td>20.009, 27.012, 27.05</td>
<td>5/6/2011</td>
<td>Syed Y. Hasan</td>
</tr>
</tbody>
</table>

---

**SEARCH NOTES**

<table>
<thead>
<tr>
<th>Search Notes</th>
<th>Date</th>
<th>Examiner</th>
</tr>
</thead>
</table>

---

**INTERFERENCE SEARCH**

<table>
<thead>
<tr>
<th>Class</th>
<th>Subclass</th>
<th>Date</th>
<th>Examiner</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLAIM</td>
<td>DATE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>-------</td>
<td>------</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Final</td>
<td>Original</td>
<td>05/06/2011</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>O</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>=</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>=</td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>=</td>
<td></td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
# List of Art Cited by Applicant

## PTO-1449

### U.S. Patent Documents

<table>
<thead>
<tr>
<th>EXAMINER'S INITIALS</th>
<th>*PATENT NO.</th>
<th>*ISSUE DATE</th>
<th>*INVENTOR NAME</th>
<th>CLASS</th>
<th>SUBCLASS</th>
<th>FILING DATE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### U.S. Patent Application Publications

<table>
<thead>
<tr>
<th>*PATENT APPLN. PUB. NO.</th>
<th>*PUB. DATE</th>
<th>*APPLICANT</th>
<th>CLASS</th>
<th>SUBCLASS</th>
<th>FILING DATE</th>
</tr>
</thead>
</table>

### U.S. Patent Applications

<table>
<thead>
<tr>
<th>*APPLN. NO.</th>
<th>*FILING DATE</th>
<th>*INVENTOR</th>
<th>CLASS</th>
<th>SUBCLASS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Foreign Patent Documents

<table>
<thead>
<tr>
<th>EXAMINER'S INITIALS</th>
<th>PATENT NO.</th>
<th>DATE</th>
<th>COUNTRY</th>
<th>CLASS</th>
<th>SUBCLASS</th>
<th>Translation</th>
</tr>
</thead>
<tbody>
<tr>
<td>/SH/</td>
<td>EP 1 605 453 A2</td>
<td>12/14/2005</td>
<td>Europe</td>
<td></td>
<td></td>
<td>X</td>
</tr>
</tbody>
</table>

### Other Art


### Examiner

/ Syed Hasan /  

**DATE CONSIDERED** 05/07/2011

---

**EXAMINER:** Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.
## EAST Search History

### EAST Search History (Prior Art)

<table>
<thead>
<tr>
<th>Ref #</th>
<th>Hits</th>
<th>Search Query</th>
<th>DBs</th>
<th>Default Operator</th>
<th>Plurals</th>
<th>Time Stamp</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1</td>
<td>1</td>
<td>11/835816</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>OR</td>
<td>OFF</td>
<td>2011/05/07 13:30</td>
</tr>
<tr>
<td>L2</td>
<td>117</td>
<td>hierarchical memories</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 13:31</td>
</tr>
<tr>
<td>L3</td>
<td>0</td>
<td>dvr with (hierarchical memories)</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 13:31</td>
</tr>
<tr>
<td>L4</td>
<td>0</td>
<td>dvr same (hierarchical memories)</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 13:31</td>
</tr>
<tr>
<td>L5</td>
<td>0</td>
<td>dvr and (hierarchical memories)</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 13:31</td>
</tr>
<tr>
<td>L6</td>
<td>2</td>
<td>recorder and (hierarchical memories)</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 13:31</td>
</tr>
<tr>
<td>L7</td>
<td>2</td>
<td>(video recorder) and (hierarchical memories)</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 13:32</td>
</tr>
<tr>
<td>L8</td>
<td>2</td>
<td>(digital video recorder) and (hierarchical memories)</td>
<td>US-PG/PUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 13:33</td>
</tr>
<tr>
<td>L9</td>
<td>3724</td>
<td>(digital video recorder) and (memory and (hard disk))</td>
<td>US-PG/PUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 13:33</td>
</tr>
<tr>
<td>L10</td>
<td>183</td>
<td>(digital video recorder) with (memory and (hard disk))</td>
<td>US-PG/PUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 13:34</td>
</tr>
<tr>
<td>L11</td>
<td>2</td>
<td>(digital video recorder) with (memory and (hard disk)) with (memory controller)</td>
<td>US-PG/PUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 13:34</td>
</tr>
<tr>
<td>L12</td>
<td>28</td>
<td>(digital video recorder) with (memory and (hard disk)) and (memory controller)</td>
<td>US-PG/PUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 13:35</td>
</tr>
<tr>
<td>L13</td>
<td>28</td>
<td>(digital video recorder) and memory and (hard disk) and (memory controller) and (audio and video) and (demultiplexer)</td>
<td>US-PG/PUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 13:39</td>
</tr>
<tr>
<td>L14</td>
<td>13</td>
<td>(digital video recorder) and memory and (hard disk) and (memory controller) and (audio and video) and (demultiplexer) and (volatile and nonvolatile)</td>
<td>US-PG/PUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 13:47</td>
</tr>
<tr>
<td>L15</td>
<td>0</td>
<td>(hierarchical memories) and (volatile memory) and (non-volatile memory) and (hard disk)</td>
<td>US-PG/PUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 13:52</td>
</tr>
<tr>
<td>Line</td>
<td>Score</td>
<td>Term</td>
<td>Indexes</td>
<td>Adj</td>
<td>Date</td>
<td>Time</td>
</tr>
<tr>
<td>------</td>
<td>-------</td>
<td>------</td>
<td>---------</td>
<td>-----</td>
<td>------</td>
<td>------</td>
</tr>
<tr>
<td>L16</td>
<td>0</td>
<td>(volatile memory) and (non-volatile memory) and (hard disk)</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>2011/05/07 13:52</td>
<td></td>
</tr>
<tr>
<td>L17</td>
<td>2</td>
<td>(hierarchical memories) and (volatile memory) and (non-volatile memory) and (hard disk)</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>2011/05/07 13:52</td>
<td></td>
</tr>
<tr>
<td>L18</td>
<td>56133</td>
<td>(volatile memory) and (non-volatile memory) and (hard disk)</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>2011/05/07 13:53</td>
<td></td>
</tr>
<tr>
<td>L19</td>
<td>16696</td>
<td>(volatile memory) with (non-volatile memory) with (hard disk)</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>2011/05/07 13:53</td>
<td></td>
</tr>
<tr>
<td>L20</td>
<td>2038</td>
<td>(volatile memory) near (non-volatile memory) near (hard disk)</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>2011/05/07 13:53</td>
<td></td>
</tr>
<tr>
<td>L21</td>
<td>11</td>
<td>(volatile memory) (non-volatile memory) (hard disk)</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>2011/05/07 13:54</td>
<td></td>
</tr>
<tr>
<td>L22</td>
<td>0</td>
<td>(stored) near (order) near (volatile memory) near (non-volatile memory) near (hard disk)</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>2011/05/07 13:56</td>
<td></td>
</tr>
<tr>
<td>L23</td>
<td>17</td>
<td>(stored) with (order) with (volatile memory) with (non-volatile memory) with (hard disk)</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>2011/05/07 13:56</td>
<td></td>
</tr>
<tr>
<td>L24</td>
<td>12</td>
<td>(hierarchical memories) and (memory) and (hard dis$1)</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 14:14</td>
</tr>
<tr>
<td>L25</td>
<td>1</td>
<td>(personal video recorder) with (volatile memory) with (non-volatile memory) with (hard dis $1)</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 14:24</td>
</tr>
<tr>
<td>L26</td>
<td>96</td>
<td>(personal video recorder) and (volatile memory) with (non-volatile memory) with (hard dis $1)</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 14:24</td>
</tr>
<tr>
<td>L27</td>
<td>96</td>
<td>(personal video recorder) and ((volatile memory) with (non-volatile memory) with (hard dis $1))</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 14:25</td>
</tr>
<tr>
<td>L28</td>
<td>3</td>
<td>(personal video recorder) same ((volatile memory) with (non-volatile memory) with (hard dis $1))</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 14:25</td>
</tr>
<tr>
<td>L29</td>
<td>28</td>
<td>partition$2 (volatile memory)</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 14:28</td>
</tr>
<tr>
<td>L30</td>
<td>0</td>
<td>(non-volatile memory) (overflow) (volatile memory)</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 14:49</td>
</tr>
<tr>
<td>L31</td>
<td>39</td>
<td>(non-volatile memory) with (overflow) with (volatile memory)</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 14:49</td>
</tr>
<tr>
<td>L32</td>
<td>1</td>
<td>(&quot;20040202073&quot;), PN</td>
<td>US-PGPUB; USPAT; USOCR</td>
<td>OR</td>
<td>OFF</td>
<td>2011/05/07 14:59</td>
</tr>
<tr>
<td>L33</td>
<td>176</td>
<td>((digital video recorder) or (dvr)) and (volatile memory) and (hard dis $1) and (memory controller) and (decoder)</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 15:10</td>
</tr>
<tr>
<td>L34</td>
<td>9</td>
<td>((digital video recorder) or (dvr)) and (volatile memory) and (hard dis $1) and (memory controller) and (decoder) and (stream data)</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 15:10</td>
</tr>
<tr>
<td>L35</td>
<td>1</td>
<td>((digital video recorder) or (dvr)) and ((volatile memory) with (hard dis $1) with (memory controller) with (decoder))</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 15:13</td>
</tr>
<tr>
<td>L36</td>
<td>1</td>
<td>((volatile memory) with (hard dis$1) with (memory controller) with (decoder))</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 15:13</td>
</tr>
<tr>
<td>L37</td>
<td>2</td>
<td>((volatile memory) same (hard dis$1) same (memory controller) same (decoder))</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 15:14</td>
</tr>
<tr>
<td>L38</td>
<td>1993</td>
<td>((volatile memory) and (hard dis$1) and (memory controller) and (decoder))</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 15:16</td>
</tr>
<tr>
<td>L39</td>
<td>11</td>
<td>((volatile memory) with (hard dis$1) with (memory controller) and (decoder))</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 15:16</td>
</tr>
<tr>
<td>L40</td>
<td>50</td>
<td>(volatile memory) with (hard dis$1) with (memory controller)</td>
<td>US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB</td>
<td>ADJ</td>
<td>OFF</td>
<td>2011/05/07 15:40</td>
</tr>
</tbody>
</table>
### EAST Search History (Interference)

EAST Search History (Interference)

**<This search history is empty>**

---

**5/7/2011 6:01:26 PM**

C:\Documents and Settings\shasan\My Documents\EAST\Workspaces\11835816\11835816 050611b.wsp
SPE RESPONSE FOR CERTIFICATE OF CORRECTION

DATE: February 17, 2011
TO SPE OF: ART UNIT 2822
SUBJECT: Request for Certificate of Correction for Appl. No.: 11/835816 patent no 783590

CofC mailroom date: 2-09-11

Please respond to this request for a certificate of correction within 7 days.

FOR IFW FILES:

Please review the requested changes/corrections as shown in the COCIN document(s) in the IFW application image. No new matter should be introduced, nor should the scope or meaning of the claims be changed.

Please complete the response (see below) and forward the completed response to scanning using document code COCX.

FOR PAPER FILES:

Please review the requested changes/corrections as shown in the attached certificate of correction. Please complete this form (see below) and forward it with the file to:

Certificates of Correction Branch (CofC)
Randolph Square – 9D10-A
Palm Location 7580

Magdalene Talley
Certificates of Correction Branch
571-272-0423

Thank You For Your Assistance

The request for issuing the above-identified correction(s) is hereby:

Note your decision on the appropriate box.

☐ Approved
☐ Approved in Part
☐ Denied

All changes apply.
Specify below which changes do not apply.
State the reasons for denial below.

Comments: ____________________________________________

______________________________________________________

______________________________________________________

______________________________________________________

______________________________________________________

PTOL-306 (REV. 7/03) U.S. DEPARTMENT OF COMMERCE Patent and Trademark Office
# LIST OF ART CITED BY APPLICANT

(PTO-1449)

<table>
<thead>
<tr>
<th>EXAMINER’S INITIALS</th>
<th>*PATENT NO.</th>
<th>*ISSUE DATE</th>
<th>*INVENTOR NAME</th>
<th>CLASS</th>
<th>SUBCLASS</th>
<th>FILING DATE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## U.S. PATENT DOCUMENTS

<table>
<thead>
<tr>
<th>*PATENT APPLN. PUB. NO.</th>
<th>*PUB. DATE</th>
<th>*APPLICANT</th>
<th>CLASS</th>
<th>SUBCLASS</th>
<th>FILING DATE</th>
</tr>
</thead>
</table>

## U.S. PATENT APPLICATION PUBLICATIONS

<table>
<thead>
<tr>
<th>*APPLN. NO.</th>
<th>*FILING DATE</th>
<th>*INVENTOR</th>
<th>CLASS</th>
<th>SUBCLASS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## U.S. PATENT APPLICATIONS

<table>
<thead>
<tr>
<th>EXAMINER’S INITIALS</th>
<th>PATENT NO.</th>
<th>DATE</th>
<th>COUNTRY</th>
<th>CLASS</th>
<th>SUBCLASS</th>
<th>Translation</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>EP 1 605 453 A2</td>
<td>12/14/2005</td>
<td>Europe</td>
<td></td>
<td>X</td>
<td></td>
</tr>
</tbody>
</table>

## FOREIGN PATENT DOCUMENTS

<table>
<thead>
<tr>
<th>OTHER ART (Including Author, Title, Date, Pertinent Pages, Publisher, Place of Publication, Etc.)</th>
</tr>
</thead>
</table>

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR
HU IE IS IT LI LT LU MC NL PL PT RO SE SI SK TR
Designated Extension States:
AL BA HR LV MK YU

(30) Priority: 10.06.2004 US 865368

(71) Applicant: Marvell World Trade Ltd.
St. Michael (BB)

(72) Inventor: Sutardja, Sehat
Los Altos Hills California 94022 (US)

(74) Representative: Grünecker, Kinkeldey,
Stockmair & Schwanhäusser Anwältssozietät
Maximilianstrasse 58
80538 München (DE)

(54) Adaptive storage system

(57) A disk drive system for a computer with high power and low power modes, comprising a low power disk drive (LPDD); a high power disk drive (HPDD); and a control module that includes a least used block (LUB) module that identifies a LUB in said LPDD, wherein said control module selectively transfers said LUB to said HPDD during said low power mode when at least one of a data storing request and a data retrieving request is received.
Description

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is related to U.S. Patent Application No. 10/779,544, which was filed on February 13, 2004 and related to U.S. Patent Application No. [which was filed on _____________________], (Marvell Docket No. MP0484) and which are hereby incorporated by reference in their entirety.

FIELD OF THE INVENTION

[0002] The present invention relates to data storage systems, and more particularly to low power data storage systems.

BACKGROUND OF THE INVENTION

[0003] Laptop computers are powered using both line power and battery power. The processor, graphics processor, memory and display of the laptop computer consume a significant amount of power during operation. One significant limitation of laptop computers relates to the amount of time that the laptop can be operated using batteries without recharging. The relatively high power dissipation of the laptop computer usually corresponds to a relatively short battery life.

[0004] Referring now to FIG. 1A, an exemplary computer architecture 4 is shown to include a processor 6 with memory 7 such as cache. The processor 6 communicates with an input/output (I/O) interface 8. Volatile memory 9 such as random access memory (RAM) 10 and/or other suitable electronic data storage also communicates with the interface 8. A graphics processor 11 and memory 12 such as cache increase the speed of graphics processing and performance.

[0005] One or more I/O devices such as a keyboard 13 and a pointing device 14 (such as a mouse and/or other suitable device) communicate with the interface 8. A high power disk drive (HPDD) 15 such as a hard disk drive having one or more platters with a diameter greater than 1.8" provides nonvolatile memory, stores data and communicates with the interface 8. The HPDD 15 typically consumes a relatively high amount of power during operation. When operating on batteries, frequent use of the HPDD 15 will significantly decrease battery life. The computer architecture 4 also includes a display 16, an audio output device 17 such as audio speakers and/or other input/output devices that are generally identified at 18.

[0006] Referring now to FIG. 1B, an exemplary computer architecture 20 includes a processing chipset 22 and an I/O chipset 24. For example, the computer architecture may be a Northbridge/Southbridge architecture (with the processing chipset corresponding to the Northbridge chipset and the I/O chipset corresponding to the Southbridge chipset) or other similar architecture. The processing chipset 22 communicates with a processor 25 and a graphics processor 26 via a system bus 27. The processing chipset 22 controls interaction with volatile memory 28 (such as external DRAM or other memory), a Peripheral Component Interconnect (PCI) bus 30, and/or Level 2 cache 32. Level 1 cache 33 and 34 may be associated with the processor 25 and/or the graphics processor 26, respectively. In an alternate embodiment, an Accelerated Graphics Port (AGP) (not shown) communicates with the processing chipset 22 instead of and/or in addition to the graphics processor 26. The processing chipset 22 is typically but not necessarily implemented using multiple chips. PCI slots 36 interface with the PCI bus 30.

[0007] The I/O chipset 24 manages the basic forms of input/output (I/O). The I/O chipset 24 communicates with an Universal Serial Bus (USB) 40, an audio device 41, a keyboard (KBD) and/or pointing device 42, and a Basic Input/Output System (BIOS) 43 via an Industry Standard Architecture (ISA) bus 44. Unlike the processing chip 22, the I/O chip 24 is typically (but not necessarily) implemented using a single chip, which is connected to the PCI bus 30. A HPDD 50 such as a hard disk drive also communicates with the I/O chipset 24. The HPDD 50 stores a full-featured operating system (OS) such as Windows XP®/Windows 2000®, Linux and MAC®-based OS that is executed by the processor 25.

SUMMARY OF THE INVENTION

[0008] A disk drive system according to the present invention for a computer with high power and low power modes comprises a low power disk drive (LPDD) and a high power disk drive (HPDD). A control module includes a least used block (LUB) module that identifies a LUB in the LPDD. The control module selectively transfers the LUB to the HPDD during the low power mode when at least one of a data storing request and a data retrieving request is received.

[0009] In other features, during the storing request for write data, the control module transfers the write data to the LPDD if sufficient space is available on the LPDD for the write data. If there is insufficient space available for the write data on the LPDD, the control module powers the HPDD and transfers the LUB from the LPDD to the HPDD and the write data to the LPDD.

[0010] In yet other features, the control module includes an adaptive storage module that determines whether the write data is likely to be used before the LUB when there is insufficient space available for the write data on the LPDD. If the write data is likely to be used, the control module stores the write data on the HPDD. If the write data is likely to be used before the LUB, the control module powers the HPDD and transfers the LUB from the LPDD to the HPDD and the write data to the LPDD.

[0011] In still other features, during the data retrieving
request for read data, the control module retrieves the read data from the LPDD if the read data is stored in the LPDD. The control module includes an adaptive storage module that determines whether the read data is likely to be used once when the read data is not located on the LPDD. The control module retrieves the read data from the HPDD if the read data is likely to be used once. If the adaptive storage module determines that the read data is likely to be used more than once, the control module transfers the read data from the HPDD to the LPDD if sufficient space is available on the LPDD for the read data. If the adaptive storage module determines that the read data is likely to be used more than once, the control module transfers the LUB from the LPDD to the HPDD and the read data from the HPDD to the LPDD if sufficient space is not available on the LPDD for the read data.

[0012] In still other features, the control module transfers the read data from the HPDD to the LPDD if sufficient space is available on the LPDD for the read data. The control module transfers the LUB from the LPDD to the HPDD and the read data from the HPDD to the LPDD if sufficient space is not available on the LPDD for the read data. If the read data is not located on the LPDD, the control module retrieves the read data from the HPDD.

[0013] In still other features, the HPDD includes one or more platters, wherein the one or more platters have a diameter that is greater than 1.8". The LPDD includes one or more platters, wherein the one or more platters have a diameter that is less than or equal to 1.8".

[0014] A disk drive system according to the present invention for a computer including low power and high power modes comprises a low power disk drive (LPDD) and a high power disk drive (HPDD). A control module communicates with the LPDD and the HPDD. During a storing request for write data in the low power mode, the control module determines whether there is sufficient space available on the LPDD for the write data and transfers the write data to the LPDD if sufficient space is available.

[0015] In other features, the control module stores the write data on the LPDD if insufficient space is available. The control module further includes a LPDD maintenance module that transfers data files from the LPDD to the HPDD during the high power mode to increase available disk space on the LPDD. The LPDD maintenance module transfers the data files based on at least one of age, size and likelihood of future use in the low power mode. The HPDD includes one or more platters having a diameter that is greater than 1.8". The LPDD includes one or more platters having a diameter that is less than or equal to 1.8".

[0016] A data storage system according to the present invention for a computer including low power and high power modes comprises low power (LP) nonvolatile memory and high power (HP) nonvolatile memory. A cache control module communicates with the LP and HP nonvolatile memory and includes an adaptive storage module. When write data is to be written to one of the LP and HP nonvolatile memory, the adaptive storage module generates an adaptive storage decision that selects one of the LP and HP nonvolatile memory.

[0017] In other features, the adaptive decision is based on at least one of power modes associated with prior uses of the write data, a size of the write data, a date of last use of the write data and a manual override status of the write data. The LP nonvolatile memory includes at least one of flash memory and a low power disk drive (LPDD). The LPDD includes one or more platters, wherein the one or more platters have a diameter that is less than or equal to 1.8". The HP nonvolatile memory comprises a hard disk drive including one or more platters, wherein the one or more platters have a diameter that is greater than 1.8".

[0018] A data storage system according to the present invention for a computer including low power and high power modes comprises low power (LP) nonvolatile memory and high power (HP) nonvolatile memory. A cache control module communicates with the LP and HP nonvolatile memory and includes a drive power reduction module. When read data is read from the HP nonvolatile memory during the low power mode and the read data includes a sequential access data file, the drive power reduction module calculates a burst period for transfers of segments of the read data from the HP nonvolatile memory to LP nonvolatile memory.

[0019] In other features, the drive power reduction module selects the burst period to reduce power consumption during playback of the read data during the low power mode. The LP nonvolatile memory includes at least one of flash memory and a low power disk drive (LPDD). The LPDD includes one or more platters, wherein the one or more platters have a diameter that is less than or equal to 1.8". The HP nonvolatile memory comprises a high power disk drive (HPDD). The HPDD includes one or more platters, wherein the one or more platters have a diameter that is greater than 1.8". The burst period is based on at least one of spin-up time of the LPDD, spin-up time of the HPDD, power consumption of the LPDD, playback length of the read data, and capacity of the LPDD.

[0020] A multi-disk drive system according to the present invention comprises a high power disk drive (HPDD) including one or more platters, wherein the one or more platters have a diameter that is greater than 1.8" and a low power disk drive (LPDD) including one or more platters, wherein the one or more platters have a diameter that is less than or equal to 1.8". A drive control module collectively controls data access to the LPDD and the HPDD.

[0021] A redundant array of independent disks (RAID) system according to the present invention comprises a first disk array that includes X high power disk drives (HPDD), wherein X is greater than or equal to 2. A sec-
ond disk array includes Y low power disk drives (LPDD), wherein Y is greater than or equal to 1. An array man-
gagement module communicates with the first and sec-
ond disk arrays and utilizes the second disk array to
cache data to and/or from the first disk array.

Further areas of applicability of the present in-
vvention will become apparent from the detailed descrip-
tion provided hereinafter. It should be understood that
the detailed description and specific examples, while
indicating the preferred embodiment of the invention, are
intended for purposes of illustration only and are not in-
tended to limit the scope of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become more fully
understood from the detailed description and the ac-
companying drawings, wherein:

FIG. 1A and 1B illustrate exemplary computer
architectures according to the prior art;

FIG. 2A illustrates a first exemplary computer
architecture according to the present invention with a
primary processor, a primary graphics processor, and
primary volatile memory that operate during an high
power mode and a secondary processor and a second-
ary graphics processor that communicate with the pri-
mary processor, that operate during a low power
mode and that employ the primary volatile memory
during the low power mode;

FIG. 2B illustrates a second exemplary com-
puter architecture according to the present inven-
tion that is similar to FIG. 2A that includes secondary
volatile memory that is connected to the secondary
processor and/or the secondary graphics processor;

FIG. 2C illustrates a third exemplary computer
architecture according to the present invention that is
similar to FIG. 2A that includes embedded volatile
memory that is associated with the secondary processor
and/or the secondary graphics processor;

FIG. 3A illustrates a fourth exemplary architec-
ture according to the present invention for a com-
puter with a primary processor, a primary graphics processor,
and primary volatile memory that operate during an high
power mode and a secondary processor and a second-
ary graphics processor that communicate with a
processing chipset, that operate during the low power
mode and that employ the primary volatile memory
during the low power mode;

FIG. 3B illustrates a fifth exemplary computer
architecture according to the present invention that is
similar to FIG. 3A and that includes secondary volatile
memory connected to the secondary processor and/or
the secondary graphics processor;

FIG. 3C illustrates a sixth exemplary computer
architecture according to the present invention that is
similar to FIG. 3A and that includes embedded volatile
memory that is associated with the secondary processor
and/or the secondary graphics processor;

FIG. 4A illustrates a seventh exemplary archi-
tecture according to the present invention for a com-
puter with a secondary processor and a secondary graph-
ics processor that communicate with an I/O chipset, that
operate during the low power mode and that employ
the primary volatile memory during the low power mode;

FIG. 4B illustrates an eighth exemplary com-
puter architecture according to the present invention
that is similar to FIG. 4A and that includes secondary
volatile memory connected to the secondary processor
and/or the secondary graphics processor;

FIG. 4C illustrates a ninth exemplary computer
architecture according to the present invention that is
similar to FIG. 4A and that includes embedded volatile
memory that is associated with the secondary processor
and/or the secondary graphics processor; and

FIG. 5 illustrates a caching hierarchy accord-
ing to the present invention for the computer architec-
tures of FIGS. 2A-4C;

FIG. 6 is a functional block diagram of a drive
control module that includes a least used block (LUB)
module and that manages storage and transfer of data
between the low-power disk drive (LPDD) and the high-
power disk drive (HPDD);

FIG. 7A is a flowchart illustrating steps that are
performed by the drive control module of FIG. 6;

FIG. 7B is a flowchart illustrating alternative steps
that are performed by the drive control module of
FIG. 6;

FIGS. 7C and 7D are flowcharts illustrating alter-
ative steps that are performed by the drive control
module of FIG. 6;

FIG. 8A illustrates a cache control module that
includes an adaptive storage control module and that
controls storage and transfer of data between the LPDD
and HPDD;

FIG. 8B illustrates an operating system that in-
cludes an adaptive storage control module and that
controls storage and transfer of data between the LPDD
and HPDD;

FIG. 8C illustrates a host control module that
includes an adaptive storage control module and that
controls storage and transfer of data between the LPDD
and HPDD;

FIG. 9 illustrates steps performed by the adap-
tive storage control modules of FIGS. 8A-8C;

FIG. 10 is an exemplary table illustrating one
method for determining the likelihood that a program or
file will be used during the low power mode;

FIG. 11A illustrates a cache control module that
includes a disk drive power reduction module;

FIG. 11B illustrates an operating system that
includes a disk drive power reduction module;

FIG. 11C illustrates a host control module that
includes a disk drive power reduction module;

FIG. 12 illustrates steps performed by the disk
drive power reduction modules of FIGS. 11A-11C;

FIG. 13 illustrates a multi-disk drive system in-
cluding a high-power disk drive (HPDD) and a lower power disk drive (LPDD);

[0049] FIGS. 14-17 illustrate other exemplary implementations of the multi-disk drive system of FIG. 13;

[0050] FIG. 18 illustrates the use of low power non-volatile memory such as Flash memory or a low power disk drive (LPDD) for increasing virtual memory of a computer;

[0051] FIGS. 19 and 20 illustrates steps performed by the operating system to allocate and use the virtual memory of FIG. 18;

[0052] FIG. 21 is a functional block diagram of a Redundant Array of Independent Disks (RAID) system according to the prior art;

[0053] FIG. 22A is a functional block diagram of an exemplary RAID system according to the present invention with a disk array including X HPDD and a disk array including Y LPDD;

[0054] FIG. 22B is a functional block diagram of the RAID system of FIG. 22A where X and Y are equal to Z;

[0055] FIG. 23A is a functional block diagram of another exemplary RAID system according to the present invention with a disk array including Y LPDD that communicates with a disk array including X HPDD;

[0056] FIG. 23B is a functional block diagram of the RAID system of FIG. 23A where X and Y are equal to Z;

[0057] FIG. 24A is a functional block diagram of still another exemplary RAID system according to the present invention with a disk array including X HPDD that communicate with a disk array including Y LPDD;

[0058] FIG. 24B is a functional block diagram of the RAID system of FIG. 24A where X and Y are equal to Z;

[0059] FIG. 25 is a functional block diagram of a network attachable storage (NAS) system according to the prior art, and

[0060] FIG. 26 is a functional block diagram of a network attachable storage (NAS) system according to the present invention that includes the RAID system of FIGS. 22A, 22B, 23A, 23B, 24A and/or 24B and/or a multi-drive system according to FIGS. 6-17.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0061] The following description of the preferred embodiment(s) is merely exemplary in nature and is in no way intended to limit the invention, its application, or uses. For purposes of clarity, the same reference numbers will be used in the drawings to identify similar elements. As used herein, the term module and/or device refers to an application specific integrated circuit (ASIC), an electronic circuit, a processor (shared, dedicated, or group) and memory that execute one or more software or firmware programs, a combinational logic circuit, and/or other suitable components that provide the described functionality.

[0062] As used herein, the term "high power mode" refers to active operation of the host processor and/or the primary graphics processor of the host device. The term "low power mode" refers to low-power hibernating modes, off modes, and/or non-responsive modes of the primary processor and/or primary graphics processor when a secondary processor and a secondary graphics processor are operable. An "off mode" refers to situations when both the primary and secondary processors are off.

[0063] The term "low power disk drive" or LPDD refers to disk drives and/or microdrives having one or more platters that have a diameter that is less than or equal to 1.8". The term "high power disk drive" or HPDD refers to hard disk drives having one or more platters that have a diameter that is greater than 1.8". LPDDs typically have lower storage capacities and dissipate less power than the HPDDs. The LPDDs are also rotated at a higher speed than the HPDDs. For example, rotational speeds of 10,000 - 20,000 RPM or greater can be achieved with LPDDs.

[0064] The computer architecture according to the present invention includes the primary processor, the primary graphics processor, and the primary memory (as described in conjunction with FIGS. 1A and 1B), which operate during the high power mode. A secondary processor and a secondary graphics processor are operated during the low power mode. The secondary processor and the secondary graphics processor may be connected to various components of the computer, as will be described below. Primary volatile memory may be used by the secondary processor and the secondary graphics processor during the low power mode. Alternatively, secondary volatile memory, such as DRAM and/or embedded secondary volatile memory such as embedded DRAM can be used, as will be described below.

[0065] The primary processor and the primary graphics processor dissipate relatively high power when operating in the high power mode. The primary processor and the primary graphics processor execute a full-featured operating system (OS) that requires a relatively large amount of external memory. The primary processor and the primary graphics processor support high performance operation including complex computations and advanced graphics. The full-featured OS can be a Windows®-based OS such as Windows XP®, a Linux-based OS, a MAC®-based OS and the like. The full-featured OS is stored in the HPDD 15 and/or 50.

[0066] The secondary processor and the secondary graphics processor dissipate less power (than the primary processor and primary graphics processor) during the low power mode. The secondary processor and the secondary graphics processor operate a restricted-feature operating system (OS) that requires a relatively small amount of external volatile memory. The secondary processor and secondary graphics processor may also use the same OS as the primary processor. For example, a pared-down version of the full-featured OS may be used. The secondary processor and the sec-
ondary graphics processor support lower performance 
operation, a lower computation rate and less advanced 
graphics. For example, the restricted-feature OS can be 
Windows CE® or any other suitable restricted-feature 
OS. The restricted-feature OS is preferably stored in 
nonvolatile memory such as Flash memory and/or a LP-
DD. In a preferred embodiment, the full-featured and 
restricted-feature OS share a common data format to 
reduce complexity.

[0067] The primary processor and/or the primary 
graphics processor preferably include transistors that 
are implemented using a fabrication process with a rel-
atively small feature size. In one implementation, these 
transistors are implemented using an advanced CMOS 
fabrication process. Transistors implemented in the 
primary processor and/or primary graphics processor have 
relatively high standby leakage, relatively short chan-
nels and are sized for high speed. The primary proces-
sor and the primary graphics processor preferably em-
ploy predominantly dynamic logic. In other words, they 
cannot be shut down. The transistors are switched at a 
duty cycle that is less than approximately 20% and pref-
erably less than approximately 10%, although other duty 
cycles may be used.

[0068] In contrast, the secondary processor and/or 
the secondary graphics processor preferably include 
transistors that are implemented with a fabrication pro-
cess having larger feature sizes than the process used 
for the primary processor and/or primary graphics pro-
cessor. In one implementation, these transistors are im-
plemented using a regular CMOS fabrication process. 
The transistors implemented in the secondary proces-
sor and/or the secondary graphics processor have rel-
atively low standby leakage, relatively long channels and 
are sized for low power dissipation. The secondary 
processor and the secondary graphics processor prefer-
erably employ predominantly static logic rather than dy-
namic logic. The transistors are switched at a duty 
cycle that is greater than 80% and preferably greater 
than 90%, although other duty cycles may be used.

[0069] The primary processor and the primary 
graphics processor dissipate relatively high power when op-
erated in the high power mode. The secondary proces-
sor and the secondary graphics processor dissipate less 
power when operating in the low power mode. In the low 
power mode, however, the computer architecture is ca-
pable of supporting fewer features and computations 
and less complex graphics than when operating in the 
high power mode. As can be appreciated by skilled ar-
tisans, there are many ways of implementing the com-
puter architecture according to the present invention. 
Therefore, skilled artisans will appreciate that the archi-
tectures that are described below in conjunction with 
Fig. 2A-4C are merely exemplary in nature and are not 
limiting.

[0070] Referring now to FIG. 2A, a first exemplary 
computer architecture 60 is shown. The primary pro-
cessor 6, the volatile memory 9 and the primary graphics 
processor 11 communicate with the interface 8 and sup-
port complex data and graphics processing during the 
high power mode. A secondary processor 62 and a sec-
ondary graphics processor 64 communicate with the 
interface 8 and support less complex data and graphics 
processing during the low power mode. Optional non-
volatile memory 65 such as a LPDD 66 and/or Flash 
memory 68 communicates with the interface 8 and pro-
vides low power nonvolatile storage of data during the 
low power and/or high power modes. The HPDD 15 pro-
vides high power/capacity nonvolatile memory. The 
nonvolatile memory 65 and/or the HPDD 15 are used to 
store the restricted feature OS and/or other data and 
files during the low power mode.

[0071] In this embodiment, the secondary processor 
62 and the secondary graphics processor 64 employ the 
volatile memory 9 (or primary memory) while operating 
in the low-power mode. To that end, at least part of the 
interface 8 is powered during the low power mode to 
support communications with the primary memory and/or 
communications between components that are powered 
during the low power mode. For example, the key-
board 13, the pointing device 14 and the primary display 
16 may be powered and used during the low power 
mode. In all of the embodiments described in conjunc-
tion with Figs. 2A-4C, a secondary display with reduced 
capabilities (such as a monochrome display) and/or a 
secondary input/output device can also be provided and 
used during the low power mode.

[0072] Referring now to FIG. 2B, a second exemplary 
computer architecture 70 that is similar to the architec-
ture in FIG. 2A is shown. In this embodiment, the sec-
ondary processor 62 and the secondary graphics pro-
cessor 64 communicate with secondary volatile memory 
74 and/or 76. The secondary volatile memory 74 and 76 
can be DRAM or other suitable memory. During the low 
power mode, the secondary processor 62 and the sec-
ondary graphics processor 64 utilize the secondary vol-
atile memory 74 and/or 76, respectively. In addition to 
and/or instead of the primary volatile memory 9 shown 
and described in FIG. 2A.

[0073] Referring now to FIG. 2C, a third exemplary 
computer architecture 80 that is similar to FIG. 2A is 
shown. The secondary processor 62 and/or secondary 
graphics processor 64 include embedded volatile mem-
ory 84 and 86, respectively. During the low power mode, 
the secondary processor 62 and the secondary graphics 
processor 64 utilize the embedded volatile memory 84 
and/or 86, respectively, in addition to and/or instead of 
the primary volatile memory. In one embodiment, the 
embedded volatile memory 84 and 86 is embedded 
DRAM (eDRAM), although other types of embedded 
volatile memory can be used.

[0074] Referring now to FIG. 3A, a fourth exemplary 
computer architecture 100 according to the present in-
vention is shown. The primary processor 25, the primary 
graphics processor 26, and the primary volatile memory 
28 communicate with the processing chipset 22 and
support complex data and graphics processing during the high power mode. A secondary processor 104 and a secondary graphics processor 108 support less complex data and graphics processing when the computer is in the low power mode. In this embodiment, the secondary processor 104 and the secondary graphics processor 108 employ the primary volatile memory 28 while operating in the low power mode. To that end, the processing chipset 22 may be fully and/or partially powered during the low power mode to facilitate communications therebetween. The HPDD 50 may be powered during the low power mode to provide high power volatile memory. Low power nonvolatile memory 109 (LPDD 110 and/or Flash memory 112) is connected to the processing chipset 22, the I/O chipset 24 or in another location and stores the restricted-feature operating system for the low power mode.

[0075] The processing chipset 22 may be fully and/or partially powered to support operation of the HPDD 50, the LPDD 110, and/or other components that will be used during the low power mode. For example, the keyboard and/or pointing device 42 and the primary display may be used during the low power mode.

[0076] Referring now to FIG. 3B, a fifth exemplary computer architecture 150 that is similar to FIG. 3A is shown. Secondary volatile memory 154 and 158 is connected to the secondary processor 104 and/or secondary graphics processor 108, respectively. During the low power mode, the secondary processor 104 and the secondary graphics processor 108 utilize the secondary volatile memory 154 and 158, respectively, instead of and/or in addition to the primary volatile memory 28. The processing chipset 22 and the primary volatile memory 28 can be shut down during the low power mode if desired. The secondary volatile memory 154 and 158 can be DRAM or other suitable memory.

[0077] Referring now to FIG. 3C, a sixth exemplary computer architecture 170 that is similar to FIG. 3A is shown. The secondary processor 104 and/or secondary graphics processor 108 include embedded memory 174 and 176, respectively. During the low power mode, the secondary processor 104 and the secondary graphics processor 108 utilize the embedded memory 174 and 176, respectively, instead of and/or in addition to the primary volatile memory 28. In one embodiment, the embedded volatile memory 174 and 176 is embedded DRAM (eDRAM), although other types of embedded memory can be used.

[0078] Referring now to FIG. 4A, a seventh exemplary computer architecture 190 according to the present invention is shown. The secondary processor 104 and the secondary graphics processor 108 communicate with the I/O chipset 24 and employ the primary volatile memory 28 as volatile memory during the low power mode. The processing chipset 22 remains fully and/or partially powered to allow access to the primary volatile memory 28 during the low power mode.

[0079] Referring now to FIG. 4B, an eighth exemplary computer architecture 200 that is similar to FIG. 4A is shown. Secondary volatile memory 154 and 158 is connected to the secondary processor 104 and the secondary graphics processor 108, respectively, and is used instead of and/or in addition to the primary volatile memory 28 during the low power mode. The processing chipset 22 and the primary volatile memory 28 can be shut down during the low power mode.

[0080] Referring now to FIG. 4C, a ninth exemplary computer architecture 210 that is similar to FIG. 4A is shown. Embedded volatile memory 174 and 176 is provided for the secondary processor 104 and/or the secondary graphics processor 108, respectively in addition to and/or instead of the primary volatile memory 28. In this embodiment, the processing chipset 22 and the primary volatile memory 28 can be shut down during the low power mode.

[0081] Referring now to FIG. 5, a caching hierarchy 250 for the computer architectures illustrated in FIGS. 2A-4C is shown. The HP nonvolatile memory HPDD 50 is located at a lowest level 254 of the caching hierarchy 250. Level 254 may or may not be used during the low power mode if the HPDD 50 is disabled and will be used if the HPDD 50 is enabled during the low power mode. The LP nonvolatile memory such as LPDD 110 and/or Flash memory 112 is located at a next level 258 of the caching hierarchy 250. External volatile memory such as primary volatile memory, secondary volatile memory and/or secondary embedded memory is a next level 262 of the caching hierarchy 250, depending upon the configuration. Level 2 or secondary cache comprises a next level 266 of the caching hierarchy 250. Level 1 cache is a next level 268 of the caching hierarchy 250. The CPU (primary and/or secondary) is a last level 270 of the caching hierarchy. The primary and secondary graphics processor use a similar hierarchy.

[0082] The computer architecture according to the present invention provides a low power mode that supports less complex processing and graphics. As a result, the power dissipation of the computer can be reduced significantly. For laptop applications, battery life is extended.

[0083] Referring now to FIG. 6, a drive control module 300 or host control module for a multi-disk drive system includes a least used block (LUB) module 304, an adaptive storage module 306, and/or a LPDD maintenance module 308. The drive control module 300 controls storage and data transfer between a high-powered disk drive (HPDD) 310 such as a hard disk drive and a low-power disk drive (LPDD) 312 such as a microdrive based in part on LUB information. The drive control module 300 reduces power consumption by managing data storage and transfer between the HPDD and LPDD during the high and low power modes.

[0084] The least used block module 304 keeps track of the least used block of data in the LPDD 312. During the low-power mode, the least used block module 304 identifies the least used block of data (such as files and/
or programs) in the LPDD 312 so that it can be replaced when needed. Certain data blocks or files may be exempted from the least used block monitoring such as files that relate to the restricted-feature operating system only, blocks that are manually set to be stored in the LPDD 312, and/or other files and programs that are operated during the low power mode only. Still other criteria may be used to select data blocks to be overwritten, as will be described below.

[0085] During the low power mode during a data storing request the adaptive storage module 306 determines whether write data is more likely to be used before the least used blocks. The adaptive storage module 306 also determines whether read data is likely to be used only once during the low power mode during a data retrieval request. The LPDD maintenance module 308 transfers aged data from the LPDD to the HPDD during the high power mode and/or in other situations as will be described below.

[0086] Referring now to FIG. 7A, steps performed by the drive control module 300 are shown. Control begins in step 320. In step 324, the drive control module 300 determines whether there is a data storing request. If step 324 is true, the drive control module 300 determines whether there is sufficient space available on the LPDD 312 in step 328. If not, the drive control module 300 powers the HPDD 310 in step 330. In step 334, the drive control module 300 transfers the least used data block to the HPDD 310. In step 336, the drive control module 300 determines whether there is sufficient space available on the LPDD 312. If not, control loops to step 334. Otherwise, the drive control module 300 continues with step 340 and turns off the HPDD 310. In step 344, data to be stored (e.g. from the host) is transferred to the LPDD 312.

[0087] If step 324 is false, the drive control module 300 continues with step 350 and determines whether there is a data retrieving request. If not, control returns to step 324. Otherwise, control continues with step 354 and determines whether the data is located in the LPDD 312. If step 354 is true, the drive control module 300 retrieves the data from the LPDD 312 and step 356 and continues with step 324. Otherwise, the drive control module 300 powers the HPDD 310 in step 360. In step 364, the drive control module 300 determines whether there is sufficient space available on the LPDD 312 for the requested data. If not, the drive control module 300 transfers the least used data block to the HPDD 310 in step 366 and continues with step 364. When step 364 is true, the drive control module 300 transfers data to the LPDD 312 and retrieves data from the LPDD 312 in step 368. In step 370, control turns off the HPDD 310 when the transfer of the data to the LPDD 312 is complete.

[0088] Referring now to FIG. 7B, a modified approach that is similar to that shown in FIG. 7A is used and includes one or more adaptive steps performed by the adaptive storage module 306. When there is sufficient space available on the LPDD in step 328, control determines whether the data to be stored is likely to be used before the data in the least used block or blocks that are identified by the least used block module in step 372. If step 372 is false, the drive control module 300 stores the data on the HPDD in step 374 and control continues with step 324. By doing so, the power that is consumed to transfer the least used block(s) to the LPDD is saved. If step 372 is true, control continues with step 330 as described above with respect to FIG. 7A.

[0089] When step 354 is false during a data retrieval request, control continues with step 376 and determines whether data is likely to be used once. If step 376 is true, the drive control module 300 retrieves the data from the HPDD in step 378 and continues with step 324. By doing so, the power that would be consumed to transfer the data to the LPDD is saved. If step 376 is false, control continues with step 360. As can be appreciated, if the data is likely to be used once, there is no need to move the data to the LPDD. The power dissipation of the HPDD, however, cannot be avoided.

[0090] Referring now to FIG. 7C, a more simplified form of control can also be performed during low power operation. Maintenance steps can also be performed during high power and/or low power modes (using the LPDD maintenance module 308). In step 328, when there is sufficient space available on the LPDD, the data is transferred to the LPDD in step 344 and control returns to step 324. Otherwise, when step 328 is false, the data is stored on the HPDD in step 380 and control returns to step 324. As can be appreciated, the approach illustrated in FIG. 7C uses the LPDD when capacity is available and uses the HPDD when LPDD capacity is not available. Skilled artisans will appreciate that hybrid methods may be employed using various combinations of the steps of FIGs. 7A-7D.

[0091] In FIG. 7D, maintenance steps are performed by the drive control module 300 upon returning to the high power mode and/or at other times to delete unused or low use files that are stored on the LPDD. This maintenance step can also be performed in the low power mode, periodically during use, upon the occurrence of an event such as a disk full event, and/or in other situations. Control begins in step 390. In step 392, control determines whether the high power mode is in use. If not, control loops back to step 7D. If step 392 is true, control determines whether the last mode was the low power mode in step 394. If not, control returns to step 392. If step 394 is false, control performs maintenance such as moving aged or low use files from the LPDD to the HPDD in step 396. Adaptive decisions may also be made as to which files are likely to be used in the future, for example using criteria described above and below in conjunction with FIGs. 8A-10.

[0092] Referring now to FIGs. 8A and 8B, storage control systems 400-1, 400-2 and 400-3 are shown. In FIG. 8A, the storage control system 400-1 includes a cache control module 410 with an adaptive storage con-
The adaptive storage control module 414 monitors usage of files and/or programs to determine whether they are likely to be used in the low power mode or the high power mode. The cache control module 410 communicates with one or more data buses 416, which in turn, communicate with volatile memory 422 such as L1 cache, L2 cache, volatile RAM such as DRAM and/or other volatile electronic data storage. The buses 416 also communicate with low power nonvolatile memory 424 (such as Flash memory and/or a LPDD) and/or high power nonvolatile memory 426 such as an HPDD 426. In FIG. 8B, a full-featured and/or restricted feature operating system 430 is shown to include the adaptive storage control module 414. Suitable interfaces and/or controllers (not shown) are located between the data bus and the HPDD and/or LPDD.

[0093] In FIG. 8C, a host control module 440 includes the adaptive storage control module 414. The host control module 440 communicates with a LPDD 426 and a hard disk drive 426. The host control module 440 can be a drive control module, an Integrated Device Electronics (IDE), ATA, serial ATA (SATA) or other controller.

[0094] Referring now to FIG. 9, steps performed by the storage control systems in FIGS. 8A-8C are shown. In FIG. 9, control begins with step 450. In step 462, control determines whether there is a request for data storage to nonvolatile memory. If not, control loops back to step 462. Otherwise, the adaptive storage control module 414 determines whether data is likely to be used in the low-power mode in step 464. If step 464 is false, data is stored in the HPDD in step 468. If step 464 is true, the data is stored in the nonvolatile memory 444 in step 474.

[0095] Referring now to FIG. 10, one way of determining whether a data block is likely to be used in the low-power mode is shown. A table 490 includes a data block descriptor field 492, a low-power counter field 493, a high-power counter field 494, a size field 496, a last use field 496 and/or a manual override field 497. When a particular program or file is used during the low-power or high-power modes, the counter field 493 and/or 494 is incremented. When data storage of the program or file is required to nonvolatile memory, the table 492 is accessed. A threshold percentage and/or count value may be used for evaluation. For example, if a file or program is used greater than 80 percent of the time in the low-power mode, the file may be stored in the low-power nonvolatile memory such as flash memory and/or the microdrive. If the threshold is not met, the file or program is stored in the high-power nonvolatile memory.

[0096] As can be appreciated, the counters can be reset periodically, after a predetermined number of samples (in other words to provide a rolling window), and/or using any other criteria. Furthermore, the likelihood may be weighted, otherwise modified, and/or replaced by the size field 496. In other words, as the file size grows, the required threshold may be increased because of the limited capacity of the LPDD.

Further modification of the likelihood of use decision may be made on the basis of the time since the file was last used as recorded by the last use field 496. A threshold date may be used and/or the time since last use may be used as one factor in the likelihood determination. While a table is shown in FIG. 10, one or more of the fields that are used may be stored in other locations and/or in other data structures. An algorithm and/or weighted sampling of two or more fields may be used.

[0097] Using the manual override field 497 allows a user and/or the operating system to manually override the likelihood of use determination. For example, the manual override field may allow an L status for default storage in the LPDD, an H status for default storage in the HPDD and/or an A status for automatic storage decisions (as described above). Other manual override classifications may be defined. In addition to the above criteria, the current power level of the computer operating in the LPDD may be used to adjust the decision. Skilled artisans will appreciate that there are other methods for determining the likelihood that a file or program will be used in the high-power or low-power modes that fall within the teachings of the present invention.

[0098] Referring now to FIGS. 11A and 11B, drive power reduction systems 500-1, 500-2 and 500-3 (collectively 500) are shown. The drive power reduction system 500 bursts segments of a larger sequential access file such as not limited audio and/or video files to the low power nonvolatile memory on a periodic or other basis. In FIG. 11A, the drive power reduction system 500-1 includes a cache control module 520 with a drive power reduction control module 522. The cache control module 520 communicates with one or more data buses 526, which in turn, communicate with volatile memory 530, such as L1 cache, L2 cache, volatile RAM such as DRAM and/or other volatile electronic data storage, nonvolatile memory 534 such as Flash memory and/or a LPDD, and a HPDD 538. In FIG. 11B, the drive power reduction system 500-2 includes a full-featured and/or restricted feature operating system 542 with a drive power reduction control module 522. Suitable interfaces and/or controllers (not shown) are located between the data bus and the HPDD and/or LPDD.

[0100] In FIG. 11C, the drive power reduction system 500-3 includes a host control module 560 with an adaptive storage control module 522. The host control module 560 communicates with one or more data buses 564, which communicate with the LPDD 534 and the hard disk drive 538. The host control module 560 can be a drive control module, an Integrated Device Electronics (IDE), ATA, serial ATA (SATA) and/or other controller or interface.

[0101] Referring now to FIG. 12, steps performed by the drive power reduction systems 500 in FIGS. 11A-11C are shown. Control begins the step 582. In step 584, control determines whether the system is in a low-power mode. If not, control loops back to step 584. If step 586 is true, control continues with step 586 where control
determines whether a large data block access is typically requested from the HPPD in step 584. If not, control loops back to step 584. If step 586 is true, control continues with step 590 and determines whether the data block is accessed sequentially. If not, control loops back to 584. If step 590 is true; control continues with step 594 and determines the playback length. In step 598, control determines a burst period and frequency for data transfer from the high power nonvolatile memory to the low power nonvolatile memory.

[0102] In one implementation, the burst period and frequency are optimized to reduce power consumption. The burst period and frequency are preferably based upon the spin-up time of the HPDD and/or the LPDD, the capacity of the nonvolatile memory, the playback rate, the spin-up and steady state power consumption of the HPDD and/or LPDD, and/or the playback length of the sequential data block.

[0103] For example, the high power nonvolatile memory is a HPDD that consumes 1-2W operation, has a spin-up time of 4-10 seconds and a standby capacity that is typically greater than 20Gb. The low power nonvolatile memory is a microdrive that consumes 0.3-0.5W during operation, has a spin-up time of 0-3 seconds, and a standby capacity of 1-6Gb. As can be appreciated, the foregoing performance values and/or capacities will vary for other implementations. The HPDD may have a data transfer rate of 1Gb/s to the microdrive. The playback rate may be 10Mb/s (for example for video files). As can be appreciated, the burst period times the transfer rate of the HPDD should not exceed the capacity of the microdrive. The period between bursts should be greater than the spin-up time plus the burst period. Within these parameters, the power consumption of the system can be optimized. In the low power mode, if the HPDD is operated to play an entire video such as a movie, a significant amount of power is consumed. Using the method described above, the power dissipation can be reduced significantly by selectively transferring the data from the HPDD to the LPDD in multiple burst segments spaced at fixed intervals at a very high rate (e.g., 100X the playback rate) and then the HPDD can be shut down. Power savings that are greater than 50% can easily be achieved.

[0104] Referring now to FIG. 13, a multi-disk drive system 640 according to the present invention is shown to include a drive control module 650 and one or more HPDD 644 and one or more LPDD 648. The drive control module 650 communicates with a host device via host control module 651. To the host, the multi-disk drive system 640 effectively operates the HPDD 644 and LPDD 648 as a unitary disk drive to reduce complexity, improve performance and decrease power consumption, as will be described below. The host control module 651 can be an IDE, ATA, SATA and/or other control module or interface.

[0105] Referring now to FIG. 14, in one implementation the drive control module 650 includes a hard disk controller (HDC) 653 that is used to control one or both of the LPDD and/or HPDD. A buffer 656 stores data that is associated with the control of the HPDD and/or LPDD and/or aggressively buffers data to/from the HPDD and/or LPDD to increase data transfer rates by optimizing data block sizes. A processor 657 performs processing that is related to the operation of the HPDD and/or LPDD.

[0106] The HPDD 648 includes one or more platters 652 having a magnetic coating that stores magnetic fields. The platters 652 are rotated by a spindle motor that is schematically shown at 654. Generally the spindle motor 654 rotates the platter 652 at a fixed speed during the read/write operations. One or more read/write arms 658 move relative to the platters 652 to read and/or write data to/from the platters 652. Since the HPDD 648 has larger platters than the LPDD, more power is required by the spindle motor 654 to spin-up the HPDD and to maintain the HPDD at speed. Usually, the spin-up time is higher for HPDD as well.

[0107] A read/write device 659 is located near a distal end of the read/write arm 658. The read/write device 659 includes a write element such as an inductor that generates a magnetic field. The read/write device 659 also includes a read element (such as a magneto-resistive (MR) element) that senses the magnetic field on the platter 652. A preamp circuit 660 amplifies analog read/write signals.

[0108] When reading data, the preamp circuit 660 amplifies low level signals from the read element and outputs the amplified signal to the read/write channel device. While writing data, a write current is generated which flows through the write element of the read/write device 659 and is switched to produce a magnetic field having a positive or negative polarity. The positive or negative polarity is stored by the platter 652 and is used to represent data. The LPDD 644 also includes one or more platters 662, a spindle motor 664, one or more read/write arms 668, a read/write device 669, and a preamp circuit 670.

[0109] The HDC 653 communicates with the host control module 651 and with a first spindle/voice coil motor (VCM) driver 672, a first read/write channel circuit 674, a second spindle/VCM driver 676, and a second read/write channel circuit 678. The host control module 651 and the drive control module 650 can be implemented by a system on chip (SOC) 684. As can be appreciated, the spindle VCM drivers 672 and 676 and/or read/write channel circuits 674 and 678 can be combined. The spindle/VCM drivers 672 and 676 control the spindle motors 654 and 664, which rotate the platters 652 and 662, respectively. The spindle/VCM drivers 672 and 676 also generate control signals that position the read/write arms 658 and 668, respectively, for example using a voice coil actuator, a stepper motor or any other suitable actuator.

[0110] Referring now to FIGs. 15-17, other variations of the multi-disk drive system are shown. In FIG. 15, the drive control module 650 may include a direct interface
680 for providing an external connection to one or more LPDD 682. In one implementation, the direct interface is a Peripheral Component Interconnect (PCI) bus, a PCI Express (PCIx) bus, and/or any other suitable bus or interface.

[0111] In FIG. 16, the host control module 651 communicates with both the LPDD 644 and the HPDD 648. A low power drive control module 650LP and a high power disk drive control module 650HP communicate directly with the host control module. Zero, one or both of the LP and/or the HP drive control modules can be implemented as a SOC.

[0112] In FIG. 17, one exemplary LPDD 682 is shown to include an interface 690 that supports communications with the direct interface 680. As set forth above, the interfaces 680 and 690 can be a Peripheral Component Interconnect (PCI) bus, a PCI Express (PCIx) bus, and/or any other suitable bus or interface. The LPDD 682 includes an HDC 692, a buffer 694 and/or a processor 696. The LPDD 682 also includes the spindle/VCM driver 676, the read/write channel circuit 678, the platter 662, the spindle motor 665, the read/write arm 668, the read element 669, and the preamp 670, as described above. Alternately, the HDC 653, the buffer 656 and the processor 658 can be combined and used for both drives. Likewise the spindle/VCM driver and read channel circuits can optionally be combined. In the embodiments in FIGs. 13-17, aggressive buffering of the LPDD is used to increase performance. For example, the buffers are used to optimize data block sizes for optimum speed over host data buses.

[0113] In conventional computer systems, a paging file is a hidden file on the HPDD or HP nonvolatile memory that is used by the operating system to hold parts of programs and/or data files that do not fit in the volatile memory of the computer. The paging file and physical memory, or RAM, define virtual memory of the computer. The operating system transfers data from the paging file to memory as needed and returns data from the volatile memory to the paging file to make room for new data. The paging file is also called a swap file.

[0114] Referring now to FIGs. 18-20, the present invention utilizes the LP nonvolatile memory such as the LPDD and/or flash memory to increase the virtual memory of the computer system. In FIG. 18, an operating system 700 allows a user to define virtual memory 702. During operation, the operating system 700 addresses the virtual memory 702 via one or more buses 704. The virtual memory 702 includes both volatile memory 708 and LP nonvolatile memory 710 such as Flash memory and/or a LPDD.

[0115] Referring now to FIG. 19, the operating system allows a user to allocate some or all of the LP nonvolatile memory 710 as paging memory to increase virtual memory. In step 720, control begins. In step 724, the operating system determines whether additional paging memory is requested. If not, control loops back to step 724. Otherwise, the operating system allocates part of the LP nonvolatile memory for paging file use to increase the virtual memory in step 728.

[0116] In FIG. 20, the operating system employs the additional LP nonvolatile memory as paging memory. Control begins in step 740. In step 744, control determines whether the operating system is requesting a data write operation. If true, control continues with step 748 and determines whether the capacity of the volatile memory is exceeded. If not, the volatile memory is used for the write operation in step 750. If step 748 is true, data is stored in the paging file in the LP nonvolatile memory in step 754. If step 744 is false, control continues with step 780 and determines whether a data read is requested. If false, control loops back to step 744. Otherwise, control determines whether the address corresponds to a RAM address in step 764. If step 764 is true, control reads data from the volatile memory in step 768 and continues with step 744. If step 764 is false, control reads data from the paging file in the LP nonvolatile memory in step 770 and control continues with step 744.

[0117] As can be appreciated, using LP nonvolatile memory such as Flash memory and/or the LPDD to increase the size of virtual memory will increase the performance of the computer as compared to systems employing the HPDD. Furthermore, the power consumption will be lower than systems using the HPDD for the paging file. The HPDD requires additional spin-up time due to its increased size, which increases data access times as compared to the Flash memory, which has no spin-up latency, and/or the LPDD, which has a shorter spin-up time and lower power dissipation.

[0118] Referring now to FIG. 21, a Redundant Array of Independent Disks (RAID) system 800 is shown to include one or more servers and/or clients 804 that communicate with a disk array 808. The one or more servers and/or clients 804 include a disk array controller 812 and/or an array management module 814. The disk array controller 812 and/or the array management module 814 receive data and perform logical to physical address mapping of the data to the disk array 808. The disk array typically includes a plurality of HPDD 816.

[0119] The multiple HPDDs 816 provide fault tolerance (redundancy) and/or improved data access rates. The RAID system 800 provides a method of accessing multiple individual HPDDs as if the disk array 808 is one large hard disk drive. Collectively, the disk array 808 may provide hundreds of Gb to 10's of Tb of data storage. Data is stored in various ways on the multiple HPDDs 816 to reduce the risk of losing all of the data if one drive fails and to improve data access time.

[0120] The method of storing the data on the HPDDs 816 is typically called a RAID level. There are various RAID levels including RAID level 0 or disk striping. In RAID level 0 systems, data is written in blocks across multiple drives to allow one drive to write or read a data block while the next is seeking the next block. The advantages of disk striping include the higher access rate.
and full utilization of the array capacity. The disadvantage is there is no fault tolerance. If one drive fails, the entire contents of the array become inaccessible.

[0121] RAID level 1 or disk mirroring provides redundancy by writing twice - one to each drive. If one drive fails, the other contains an exact duplicate of the data and the RAID system can switch to using the mirror drive with no lapse in user accessibility. The disadvantages include a lack of improvement in data access speed and higher cost due to the increased number of drives (2N) that are required. However, RAID level 1 provides the best protection of data since the array management software will simply direct all application requests to the surviving HPDDs when one of the HPDDs fails.

[0122] RAID level 3 stripes data across multiple drives with an additional drive dedicated to parity, for error correction/recovery. RAID level 5 provides striping as well as parity for error recovery. In RAID level 5, the parity block is distributed among the drives of the array, which provides more balanced access load across the drives. The parity information is used to recover data if one drive fails. The disadvantage is a relatively slow write cycle (2 reads and 2 writes are required for each block written). The array capacity is N-1, with a minimum of 3 drives required.

[0123] RAID level 0+1 involves striping and mirroring without parity. The advantages are fast data access (like RAID level 0), and single drive fault tolerance (like RAID level 1). RAID level 0+1 still requires twice the number of disks (like RAID level 1). As can be appreciated, there can be other RAID levels and/or methods for storing the data on the array 808.

[0124] Referring now to FIGs. 22A and 22B, a RAID system 834-1 according to the present invention includes a disk array 836 that includes X HPDD and a disk array 838 that includes Y LPDD. One or more clients and/or a servers 840 include a disk array controller 842 and/or an array management module 844. While separate devices 842 and 844 are shown, these devices can be integrated if desired. As can be appreciated, X is greater than or equal to 2 and Y is greater than or equal to 1. X can be greater than Y, less than Y and/or equal to Y. For example, FIG. 22B shows a RAID system 834-1' where X = Y = Z.

[0125] Referring now to FIGs. 23A, 23B, 24A and 24B, RAID systems 834-2 and 834-3 are shown. In FIG. 23A, the LPDD disk array 838 communicates with the servers/clients 840 and the HPDD disk array 836 communicates with the LPDD disk array 838. The RAID system 834-2 may include a management bypass path that selectively circumvents the LPDD disk array 838. As can be appreciated, X is greater than or equal to 2 and Y is greater than or equal to 1. X can be greater than Y, less than Y and/or equal to Y. For example, FIG. 23B shows a RAID system 834-2' where X = Y = Z. In FIG. 24A, the HPDD disk array 836 communicates with the servers/clients 840 and the LPDD disk array 838 communicates with the HPDD disk array 836. The RAID system 834-2 may include a management bypass path shown by dotted line 846 that selectively circumvents the LPDD disk array 838. As can be appreciated, X is greater than or equal to 2 and Y is greater than or equal to 1. X can be greater than Y, less than Y and/or equal to Y. For example, FIG. 24B shows a RAID system 834-3' where X = Y = Z. The strategy employed may include write through and/or write back in FIGs. 23A-24B.

[0126] The array management module 844 and/or the disk controller 842 utilizes the LPDD disk array 838 to reduce power consumption of the HPDD disk array 836. Typically, the HPDD disk array 808 in the conventional RAID system in FIG. 21 is kept on at all times during operation to support the required data access times. As can be appreciated, the HPDD disk array 808 dissipates a relatively high amount of power. Furthermore, since a large amount of data is stored in the HPDD disk array 808, the platters of the HPDDs are typically as large as possible, which requires higher capacity spindle motors and increases the data access times since the read/write arms move further on average.

[0127] According to the present invention, the techniques that are described above in conjunction with FIGs. 6-17 are selectively employed in the RAID system 834 as shown in FIG. 22B to reduce power consumption and data access times. While not shown in FIGs. 22A and 23A-24B, the other RAID systems according to the present invention may also use these techniques. In other words, the LUB module 304, adaptive storage module 306 and/or the LPDD maintenance module that are described in FIGs. 6 and 7A-7D are selectively implemented by the disk array controller 842 and/or the array management controller 844 to selectively store data on the LPDD disk array 838 to reduce power consumption and data access times. The adaptive storage control module 414 that is described in FIGs. 8A-8C, 9 and 10 may also be selectively implemented by the disk array controller 842 and/or the array management controller 844 to reduce power consumption and data access times. The drive power reduction module 522 that is described FIGs. 11A-11C and 12 may also be implemented by the disk array controller 842 and/or the array management controller 844 to reduce power consumption and data access times. Furthermore, the multi-drive systems and/or direct interfaces that are shown in FIGs. 13-17 may be implemented with one or more of the HPDD in the HPDD disk array 836 to increase functionality and to reduce power consumption and access times.

[0128] Referring now to FIG. 25, a network attached storage (NAS) system 850 according to the prior art is shown to include storage devices 854, storage requesters 858, a file server 862, and a communications system 866. The storage devices 854 typically include disk drives, RAID systems, tape drives, tape libraries, optical drives, jukeboxes, and any other storage devices to be shared. The storage devices 854 are preferably but not necessarily object oriented devices. The storage devices 854 may include an I/O interface for data storage and
retrieval by the requesters 858. The requesters 858 typically include servers and/or clients that share and/or directly access the storage devices 854.

[0129] The file server 862 performs management and security functions such as request authentication and resource location. The storage devices 854 depend on the file server 862 for management direction, while the requesters 858 are relieved of storage management to the extent the file server 862 assumes responsibility in smaller systems, a dedicated file server may not be desirable. In this situation, a requester may take on the responsibility for overseeing the operation of the NAS system 850. As such, both the file server 862 and the requester 858 are shown to include management modules 870 and 872, respectively, though one or the other and/or both may be provided. The communications system 866 is the physical infrastructure through which components of the NAS system 850 communicate. It preferably has properties of both networks and channels, has the ability to connect all components in the networks and the low latency that is typically found in a channel.

[0130] When the NAS system 850 is powered up, the storage devices 854 identify themselves either to each other or to a common point of reference, such as the file server 862, one or more of the requesters 858 and/or to the communications system 866. The communications system 866 typically offers network management techniques to be used for this, which are accessible by connecting to a medium associated with the communications system. The storage devices 854 and requesters 858 log onto the medium. Any component wanting to determine the operating configuration can use medium services to identify all other components. From the file server 862, the requesters 858 learn of the existence of the storage devices 854 they could have access to, while the storage devices 854 learn where to go when they need to locate another device or invoke a management service like backup. Similarly the file server 862 can learn of the existence of storage devices 854 from the medium services. Depending on the security of a particular installation, a requester may be denied access to some equipment. From the set of accessible storage devices, it can then identify the files, databases, and free space available.

[0131] At the same time, each NAS component can identify to the file server 862 any special considerations it would like known. Any device level service attributes could be communicated once to the file server 862, where all other components could learn of them. For instance, a requester may wish to be informed of the introduction of additional storage subsequent to startup, this being triggered by an attribute set when the requester logs onto the file server 862. The file server 862 could do this automatically whenever new storage devices are added to the configuration, including conveying important characteristics, such as it being RAID 5, mirrored, and so on.

[0132] When a requester must open a file, it may be able to go directly to the storage devices 854 or it may have to go to the file server for permission and location information. To what extent the file server 854 controls access to storage is a function of the security requirements of the installation.

[0133] Referring now to FIG. 26, a network attached storage (NAS) system 900 according to the present invention is shown to include storage devices 904, requesters 908, a file server 912, and a communications system 916. The storage devices 904 include the RAID system 834 and/or multi-disk drive systems 900 described above in FIGs. 9-19. The storage devices 904 typically may also include disc drives, RAID systems, tape drives, tape libraries, optical drives, jukeboxes, and/or any other storage devices to be shared as described above. As can be appreciated, using the improved RAID systems and/or multi-disk drive systems 930 will reduce the power consumption and data access times of the NAS system 900.

[0134] Those skilled in the art can now appreciate from the foregoing description that the broad teachings of the present invention can be implemented in a variety of forms. Therefore, while this invention has been described in connection with particular examples thereof, the true scope of the invention should not be so limited since other modifications will become apparent to the skilled practitioner upon a study of the drawings, the specification and the following claims.

**Embodiments**

[0135]

Embodiment 1. A disk drive system for a computer with high power and low power modes, comprising:

- a low power disk drive (LPDD);
- a high power disk drive (HPDD); and
- a control module that includes a least used block (LUB) module that identifies a LUB in said LPDD, wherein said control module selectively transfers said LUB to said HPDD during said low power mode when at least one of a data storing request and a data retrieving request is received.

Embodiment 2. The disk drive system of Embodiment 1 wherein during said storing request for write data, said control module transfers said write data to said LPDD if sufficient space is available on said LPDD for said write data.

Embodiment 3. The disk drive system of Embodiment 2 wherein if there is insufficient space available for said write data on said LPDD, said control
module powers said HPDD and transfers said LUB from said LPDD to said HPDD and transfers said write data to said LPDD.

Embodiment 4. The disk drive system of Embodiment 2 wherein said control module includes an adaptive storage module that determines whether said write data is likely to be used before said LUB when there is insufficient space available for said write data on said LPDD.

Embodiment 5. The disk drive system of Embodiment 4 wherein if said write data is likely to be used after said LUB, said control module stores said write data on said HPDD.

Embodiment 6. The disk drive system of Embodiment 4 wherein if said write data is likely to be used before said LUB, said control module powers said HPDD and transfers said LUB from said LPDD to said HPDD and then transfers said write data to said LPDD.

Embodiment 7. The disk drive system of Embodiment 1 wherein during said data retrieving request for read data, said control module retrieves said read data from said LPDD if said read data is stored in said LPDD.

Embodiment 8. The disk drive system of Embodiment 7 wherein said control module includes an adaptive storage module that determines whether said read data is likely to be used once when said read data is not located on said LPDD and wherein said control module retrieves said read data from said HPDD if said read data is likely to be used once.

Embodiment 9. The disk drive system of Embodiment 8 wherein if said adaptive storage module determines that said read data is likely to be used more than once, said control module transfers said read data from said HPDD to said LPDD if sufficient space is available on said LPDD for said read data.

Embodiment 10. The disk drive system of Embodiment 8 wherein if said adaptive storage module determines that said read data is likely to be used more than once, said control module transfers said LUB from said LPDD to said HPDD and said read data from said HPDD to said LPDD if sufficient space is not available on said LPDD for said read data.

Embodiment 11. The disk drive system of Embodiment 7 wherein said control module transfers said read data from said HPDD to said LPDD if sufficient space is available on said LPDD for said read data.

Embodiment 12. The disk drive system of Embodiment 7 wherein said control module transfers said LUB from said LPDD to said HPDD and said read data from said HPDD to said LPDD if sufficient space is not available on said LPDD for said read data.

Embodiment 13. The disk drive system of Embodiment 7 wherein if said read data is not located on said LPDD, said control module retrieves said read data from said HPDD.

Embodiment 14. The disk drive system of Embodiment 1 wherein said HPDD includes one or more platters, wherein said one or more platters have a diameter that is greater than 1.8".

Embodiment 15. The disk drive system of Embodiment 1 wherein said LPDD includes one or more platters, wherein said one or more platters have a diameter that is less than or equal to 1.8".

Embodiment 16. A disk drive system for a computer with high power and low power modes, comprising: a low power disk drive (LPDD); a high power disk drive (HPDD); and a control module that communicates with said LPDD and said HPDD, wherein during a storing request for write data in said low power mode, said control module determines whether there is sufficient space available on said LPDD for said write data and transfers said write data to said LPDD if sufficient space is available.

Embodiment 17. The disk drive system of Embodiment 16 wherein said control module stores said write data on said HPDD if insufficient space is available.

Embodiment 18. The disk drive system of Embodiment 16 wherein said control module further includes a LPDD maintenance module that transfers data files from said LPDD to said HPDD during said high power mode to increase available disk space on said LPDD.

Embodiment 19. The disk drive system of Embodiment 18 wherein said LPDD maintenance module transfers said data files based on at least one of age, size and likelihood of future use in said low power mode.

Embodiment 20. The disk drive system of Embodi-
Embodiment 16 wherein said HPDD includes one or more platters, wherein said one or more platters have a diameter that is greater than 1.8"., wherein said LP-DD includes one or more platters, wherein said one or more platters have a diameter that is less than or equal to 1.8".

Embodiment 21. A data storage system for a computer including low power and high power modes, comprising:

- low power (LP) nonvolatile memory;
- high power (HP) nonvolatile memory; and
- an adaptive storage module that communicates with said LP and HP nonvolatile memory;

wherein when write data is to be written to one of said LP and HP nonvolatile memory, said adaptive storage module generates an adaptive storage decision that selects one of said LP and HP nonvolatile memory.

Embodiment 22. The data storage system of Embodiment 21 wherein said adaptive decision is based on at least one of power modes associated with prior uses of said write data, a size of said write data, a date of last use of said write data and a manual override status of said write data.

Embodiment 23. The data storage system of Embodiment 21 wherein said LP nonvolatile memory includes at least one of flash memory and a low power disk drive (LPDD).

Embodiment 24. The data storage system of Embodiment 23 wherein said LPDD includes one or more platters, wherein said one or more platters have a diameter that is less than or equal to 1.8".

Embodiment 25. The data storage system of Embodiment 21 wherein said HP nonvolatile memory comprises a hard disk drive including one or more platters, wherein said one or more platters have a diameter that is greater than 1.8".

Embodiment 26. The data storage system of Embodiment 21 further comprising a cache control module that includes said adaptive storage module.

Embodiment 27. The data storage system of Embodiment 21 further comprising a host control module that includes said adaptive storage module.

Embodiment 28. The data storage system of Embodiment 21 further comprising an operating system that includes said adaptive storage module.

Embodiment 29. A data storage system for a computer including low power and high power modes, comprising:

- low power (LP) nonvolatile memory;
- high power (HP) nonvolatile memory; and
- a drive power reduction module that communicates with said LP and HP nonvolatile memory,

wherein when read data is read from said HP nonvolatile memory during said low power mode and said read data includes a sequential access data file, said drive power reduction module calculates a burst period for transfers of segments of said read data from said HP nonvolatile memory to LP nonvolatile memory.

Embodiment 30. The data storage system of Embodiment 29 wherein said drive power reduction module selects said burst period to reduce power consumption during playback of said read data during said low power mode.

Embodiment 31. The data storage system of Embodiment 29 wherein said LP nonvolatile memory includes at least one of flash memory and a low power disk drive (LPDD).

Embodiment 32. The data storage system of Embodiment 31 wherein said LPDD includes one or more platters, wherein said one or more platters have a diameter that is less than or equal to 1.8".

Embodiment 33. The data storage system of Embodiment 31 wherein said HP nonvolatile memory comprises a high power disk drive (HPDD).

Embodiment 34. The data storage system of Embodiment 33 wherein said HPDD includes one or more platters, wherein said one or more platters have a diameter that is greater than 1.8".

Embodiment 35. The data storage system of Embodiment 33 wherein said burst period is based on at least one of spin-up time of said LPDD, spin-up time of said HPDD, power consumption of said LP-DD, power consumption of said HPDD, playback length of said read data, and capacity of said LPDD.

Embodiment 36. The data storage system of Embodiment 29 further comprising a cache control module that includes said drive power reduction module.

Embodiment 37. The data storage system of Embodiment 29 further comprising a host control mod-
Embodyment 38. The data storage system of Embodiment 29 further comprising an operating system that includes said drive power reduction module.

Embodyment 39. A multi-disk drive system, comprising:

- a high power disk drive (HPDD) including one or more platters, wherein said one or more platters have a diameter that is greater than 1.8";
- a low power disk drive (LPDD) including one or more platters, wherein one or more platters have a diameter that is less than or equal to 1.8"; and
- a drive control module that collectively controls data access to said LPDD and said HPDD.

Embodyment 40. The multi-disk drive of Embodiment 39 further comprising a host control module that provides an interface between said drive control module and the host computer.

Embodyment 41. The multi-disk drive of Embodiment 40 wherein said drive control module includes:

- a hard drive controller (HDC) that communicates with said host control module;
- high power (HP) and low power (LP) spindle/voice coil motor (VCM) drivers that communicate with said HDC and said HPDD and said LPDD, respectively; and
- HP and LP read/write channel circuits that communicate with said HDC and said HPDD and said LPDD, respectively.

Embodyment 42. The multi-disk drive of Embodiment 41 wherein said drive control module includes:

- a drive processor that communicates with said HDC; and a buffer that communicates with said HDC.

Embodyment 43. The multi-disk drive of Embodiment 40 wherein said drive control module and said host control module are implemented as a system on chip (SOC).

Embodyment 44. The multi-disk drive of Embodiment 39 further comprising an interface for directly connecting said LPDD to said drive control module.

Embodyment 45. The multi-disk drive of Embodiment 44 wherein said interface is one of a Peripheral Component Interconnect (PCI) and PCI Express.

Embodyment 46. The multi-disk drive of Embodiment 40 wherein said drive control module comprises:

- a high power control module including:
  - a first hard drive controller (HDC) that communicates with said host control module;
  - a spindle/voice coil motor (VCM) driver that communicate with said first HDC and said HPDD; and
  - a first read/write channel circuit that communicates with said first HDC and said HPDD.

Embodyment 47. The multi-disk drive of Embodiment 46 wherein said high power control module is implemented by a system on chip (SOC).

Embodyment 48. The multi-disk drive of Embodiment 46 wherein said high power drive control module includes:

- a first drive processor that communicates with said first HDC; and a first buffer that communicates with said first HDC.

Embodyment 49. The multi-disk drive of Embodiment 40 wherein said drive control module comprises:

- a low power control module including:
  - a second hard drive controller (HDC) that communicates with said host control module;
  - a second spindle/voice coil motor (VCM) driver that communicates with said second HDC and said LPDD; and
  - a second read/write channel circuit that communicates with said second HDC and said LPDD.

Embodyment 50. The multi-disk drive of Embodiment 49 wherein said low power control module is implemented by a system on chip (SOC).

Embodyment 51. The multi-disk drive of Embodiment 49 wherein said low power drive control module includes:

- a second drive processor that communicates with said second HDC; and
- a first buffer that communicates with said sec-
ond HDC.

Embodyment 52. The multi-disk drive of Embodi-
ment 40 wherein said drive control module compri-
es:

a first hard drive controller (HDC) that com-
nunicates with said host control module;

a first spindle/voice coil motor (VCM) driver that
communicate with said first HDC and said HP-
DD;

a first read/write channel circuit that communi-
cicates with said first HDC and said HPDD; and

a first interface that communicates with said
LPDD.

Embodyment 53. The multi-disk drive of Embodi-
ment 52 wherein said HPDD further comprises:

a first drive processor that communicates with
said first HDC; and a first buffer that communi-
cates with said first HDC.

Embodyment 54. The multi-disk drive of Embodi-
ment 52 wherein said LPDD comprises:

a second interface that communicates with said
first interface;

a second hard drive controller (HDC) that com-
nunicates with said second interface;

a second spindle/voice coil motor (VCM) driver
that communicate with said second HDC; and

a second read/write channel circuit that com-
nunicates with said second HDC.

Embodyment 55. The multi-disk drive of Embodi-
ment 54 wherein said LPDD further comprises:

a second drive processor that communicates
with said second HDC; and

a second buffer that communicates with said
second HDC.

Embodyment 56. A redundant array of independent
disks (RAID) system, comprising;

a first disk array that includes \( X \) high power disk
drives (HPDD), wherein \( X \) is greater than or
equal to 2;

a second disk array that includes \( Y \) low power
disk drives (LPDD), wherein \( Y \) is greater than
or equal to 1;

an array management module that communi-
cates with said first and second disk arrays and
that utilizes said second disk array to cache data
to and/or from said first disk array.

Embodyment 57. The RAID system of Embodi-
ment 56 wherein said HPDD includes one or more platters,
wherein said one or more platters have a di-
ameter that is greater than 1.8".

Embodyment 58. The RAID system of Embodi-
ment 56 wherein said LPDD includes one or more platters,
wherein said one or more platters have a di-
ameter that is less than or equal to 1.8".

Embodyment 59. The RAID system of Embodi-
ment 56 wherein said first and second disk arrays com-
municate directly with said array management mod-
ule.

Embodyment 60. The RAID system of Embodi-
ment 56 wherein said first disk array communicates with
said array management module and said second
disk array communicates with said first disk array.

Embodyment 61. The RAID system of Embodi-
ment 56 wherein said second disk array communicates with
said array management module and said first
disk array communicates with said second disk
array.

Embodyment 62. The RAID system of Embodi-
ment 56 wherein said array management module main-
tains power to said second disk array during oper-
ation and selectively operates said first disk array
in an off mode during operation.

Embodyment 63. The RAID system of Embodi-
ment 60 further comprising a bypass path around said
first disk array, wherein said array management module selectively bypasses data around said first
disk array to said second disk array.

Embodyment 64. The RAID system of Embodi-
ment 61 further comprising a bypass path around said
second disk array, wherein said array management module selectively bypasses data around said sec-
ond disk array to said first disk array.

Embodyment 65. The RAID system of Embodi-
ment 61 wherein said array management module in-
cludes a least used block (LUB) module that iden-
tifies a LUB in a first LPDD, wherein said array man-
agement module selectively transfers said LUB to
a first HPDD during said low power mode when at
least one of a data storing request and a data retrieving request is received.

Embodiment 66. The RAID system of Embodiment 56 wherein during said storing request for write data, said array management module transfers said write data to said first LPDD if sufficient space is available on said first LPDD, wherein if there is insufficient space available for said write data on said first LPDD, said array management module powers said first HPDD and transfers said at least one said LUB from said first LPDD to said first HPDD and transfers said write data to said first LPDD.

Embodiment 67. The RAID system of Embodiment 66 wherein said array management module includes an adaptive storage module that determines whether said write data is likely to be used before said LUB when there is insufficient space available for said write data on said first LPDD, wherein if said write data is likely to be used after said LUB, said array management module stores said write data on said first HPDD, and wherein if said write data is likely to be used before said LUB, said array management module powers said first HPDD and transfers said LUB from said first LPDD to said first HPDD and then transfers said write data to said first LPDD.

Embodiment 68. The RAID system of Embodiment 65 wherein during said data retrieving request for read data, said array management module retrieves said read data from said first LPDD if said read data is stored in said first LPDD.

Embodiment 69. The RAID system of Embodiment 66 wherein said array management module includes an adaptive storage module that determines whether said read data is likely to be used once when said read data is not located on said first LPDD and wherein said array management module retrieves said read data from said first HPDD if said read data is likely to be used once, wherein if said adaptive storage module determines that read data is likely to be used more than once, said array management module transfers said read data from said first HPDD to said first LPDD if sufficient space is available on said first LPDD for said read data, and wherein if said adaptive storage module determines that said read data is likely to be used more than once, said array management module transfers said LUB from said first LPDD to said first HPDD and said read data from said first HPDD to said first LPDD if sufficient space is not available on said first LPDD for said read data.

Embodiment 70. The RAID system of Embodiment 68 wherein said array management module transfers said read data from said first HPDD to said first LPDD if sufficient space is available on said first LPDD for said read data.

Embodiment 71. The RAID system of Embodiment 68 wherein array management module transfers said LUB from said first LPDD to said first HPDD and said read data from said first HPDD to said first LPDD if sufficient space is not available on said first LPDD for said read data.

Embodiment 72. The RAID system of Embodiment 68 wherein if said read data is not located on said first LPDD, said array management module retrieves said read data from said first LPDD.

Embodiment 73. The RAID system of Embodiment 66 wherein during a storing request for write data, said array management module determines whether there is sufficient space available on a first LPDD for said write data and transfers said write data to said first LPDD if sufficient space is available, wherein said array management module stores said write data on a first HPDD if insufficient space is available.

Embodiment 74. The RAID system of Embodiment 73 wherein said array management module further includes a LPDD maintenance module that periodically transfers data files from said first LPDD to said first HPDD to increase available disk space on said first LPDD, and wherein said LPDD maintenance module transfers said data files based on at least one of age, size and likelihood of future use.

Embodiment 75. The RAID system of Embodiment 66 wherein when read data is read from said first HPDD and said read data includes a sequential access data file, said array management module calculates a burst period for transfers of segments of said read data from said first HPDD to a first LPDD, and wherein said burst period is based on at least one of spin-up time of said first LPDD, spin-up time of said first HPDD, power consumption of said first LPDD, power consumption of said first HPDD, playback length of said read data, and/or a capacity of said first LPDD.

Embodiment 76. A Network Attached Storage (NAS) system comprising the RAID system of Embodiment 66.

Claims

1. A disk drive system for a computer with high power and low power modes, comprising:
a low power disk drive (LPDD);  

a high power disk drive (HPDD); and  

a control module that includes a least used block (LUB) module that identifies a LUB in said LPDD, wherein said control module selectively transfers said LUB to said HPDD during said low power mode when at least one of a data storing request and a data retrieving request is received.

2. The disk drive system of Claim 1 wherein during said storing request for write data, said control module transfers said write data to said LPDD if sufficient space is available on said LPDD for said write data.

3. The disk drive system of Claim 2 wherein if there is insufficient space available for said write data on said LPDD, said control module powers said HPDD and transfers said LUB from said LPDD to said HPDD and transfers said write data to said LPDD.

4. The disk drive system of Claim 2 wherein said control module includes an adaptive storage module that determines whether said write data is likely to be used before said LUB when there is insufficient space available for said write data on said LPDD.

5. The disk drive system of Claim 4 wherein if said write data is likely to be used after said LUB, said control module stores said write data on said HPDD.

6. The disk drive system of Claim 4 wherein if said write data is likely to be used before said LUB, said control module powers said HPDD and transfers said LUB from said LPDD to said HPDD and then transfers said write data to said LPDD.

7. The disk drive system of Claim 1 wherein during said data retrieving request for read data, said control module retrieves said read data from said LPDD if said read data is stored in said LPDD.

8. The disk drive system of Claim 7 wherein said control module includes an adaptive storage module that determines whether said read data is likely to be used once when said read data is not located on said LPDD and wherein said control module retrieves said read data from said HPDD if said read data is likely to be used once.

9. The disk drive system of Claim 8 wherein if said adaptive storage module determines that said read data is likely to be used more than once, said control module transfers said read data from said HPDD to said LPDD if sufficient space is available on said LPDD for said read data.

10. The disk drive system of Claim 8 wherein if said adaptive storage module determines that said read data is likely to be used more than once, said control module transfers said LUB from said LPDD to said HPDD and said read data from said HPDD to said LPDD if sufficient space is not available on said LPDD for said read data.

11. The disk drive system of Claim 7 wherein said control module transfers said read data from said HPDD to said LPDD if sufficient space is available on said LPDD for said read data.

12. The disk drive system of Claim 7 wherein said control module transfers said LUB from said LPDD to said HPDD and said read data from said HPDD to said LPDD if sufficient space is not available on said LPDD for said read data.

13. The disk drive system of Claim 7 wherein if said read data is not located on said LPDD, said control module retrieves said read data from said HPDD.

14. The disk drive system of Claim 1 wherein said HPDD includes one or more platters, wherein said one or more platters have a diameter that is greater than 1.8".

15. The disk drive system of Claim 1 wherein said LPDD includes one or more platters, wherein said one or more platters have a diameter that is less than or equal to 1.8".

16. A disk drive system for a computer with high power and low power modes, comprising:

   a low power disk drive (LPDD);

   a high power disk drive (HPDD); and

   a control module that communicates with said LPDD and said HPDD,

   wherein during a storing request for write data in said low power mode, said control module determines whether there is sufficient space available on said LPDD for said write data and transfers said write data to said LPDD if sufficient space is available.

17. The disk drive system of Claim 16 wherein said control module stores said write data on said HPDD if insufficient space is available.

18. The disk drive system of Claim 16 wherein said con-
control module further includes a LPDD maintenance module that transfers data files from said LPDD to said HPDD during said high power mode to increase available disk space on said LPDD.

19. The disk drive system of Claim 18 wherein said LPDD maintenance module transfers said data files based on at least one of age, size and likelihood of future use in said low power mode.

20. The disk drive system of Claim 16 wherein said HPDD includes one or more platters, wherein said one or more platters have a diameter that is greater than 1.8", wherein said LPDD includes one or more platters, wherein said one or more platters have a diameter that is less than or equal to 1.8".

21. A data storage system for a computer including low power and high power modes, comprising:

   low power (LP) nonvolatile memory;
   
   high power (HP) nonvolatile memory; and
   
   an adaptive storage module that communicates with said LP and HP nonvolatile memory;

   wherein when write data is to be written to one of said LP and HP nonvolatile memory, said adaptive storage module generates an adaptive storage decision that selects one of said LP and HP nonvolatile memory.

22. The data storage system of Claim 21 wherein said adaptive decision is based on at least one of power modes associated with prior uses of said write data, a size of said write data, a date of last use of said write data and a manual override status of said write data.

23. The data storage system of Claim 21 wherein said LP nonvolatile memory includes at least one of flash memory and a low power disk drive (LPDD).

24. The data storage system of Claim 23 wherein said LPDD includes one or more platters, wherein said one or more platters have a diameter that is less than or equal to 1.8".

25. The data storage system of Claim 21 wherein said HP nonvolatile memory comprises a hard disk drive including one or more platters, wherein said one or more platters have a diameter that is greater than 1.8".

26. The data storage system of Claim 21 further comprising a cache control module that includes said adaptive storage module.

27. The data storage system of Claim 21 further comprising a host control module that includes said adaptive storage module.

28. The data storage system of Claim 21 further comprising an operating system that includes said adaptive storage module.
FIG. 4B

System Bus

PCI Bus

System Management Bus

ISA Bus

PCI to ISA Bridge

Flash

LPDD

Secondary GPU

Secondary CPU

Memory

Memory

I/O Chipset

Active

Optional mailbox

30

40

41

42

43

44

50

104

108

110

112

154

158

24

22

28

32

34

35

36

25

26

200
FIG. 7C

Start

Data storing request?

N

Y

320

324

Y

N

Data retrieving request?

350

N

Y

354

Data located in LPDD?

Y

N

Retrieve data from LPDD

Retrieve data from HPDD

356

Y

N

380

Store data on HPDD

Transfer data to LPDD

344

Y

N

Sufficient space avail. on LPDD?

328

FIG. 7D

Start

High power mode?

Y

N

382

Last mode low power mode?

Y

N

394

Perform housekeeping such as moving old files and/or other files that are unlikely to be used soon to HPDD.

396
# Electronic Acknowledgement Receipt

<table>
<thead>
<tr>
<th>EFS ID:</th>
<th>5991767</th>
</tr>
</thead>
<tbody>
<tr>
<td>Application Number:</td>
<td>11835816</td>
</tr>
<tr>
<td>International Application Number:</td>
<td></td>
</tr>
<tr>
<td>Confirmation Number:</td>
<td>2115</td>
</tr>
<tr>
<td>Title of Invention:</td>
<td>DIGITAL VIDEO RECORDER HAVING HIERARCHICAL MEMORIES AND METHOD FOR IMPLEMENTING HIERARCHICAL MEMORIES</td>
</tr>
<tr>
<td>First Named Inventor/Applicant Name:</td>
<td>Tae-Gyu KIM</td>
</tr>
<tr>
<td>Customer Number:</td>
<td>34610</td>
</tr>
<tr>
<td>Filer:</td>
<td>Daniel Y.J. Kim/Deborah Kimberlin</td>
</tr>
<tr>
<td>Filer Authorized By:</td>
<td>Daniel Y.J. Kim</td>
</tr>
<tr>
<td>Attorney Docket Number:</td>
<td>EZ-0001</td>
</tr>
<tr>
<td>Receipt Date:</td>
<td>01-SEP-2009</td>
</tr>
<tr>
<td>Filing Date:</td>
<td>08-AUG-2007</td>
</tr>
<tr>
<td>Time Stamp:</td>
<td>13:17:36</td>
</tr>
<tr>
<td>Application Type:</td>
<td>Utility under 35 USC 111(a)</td>
</tr>
</tbody>
</table>

**Payment information:**

Submitted with Payment  no

**File Listing:**

<table>
<thead>
<tr>
<th>Document Number</th>
<th>Document Description</th>
<th>File Name</th>
<th>File Size(Bytes)/Message Digest</th>
<th>Multi Part/.zip</th>
<th>Pages (if appl.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>EZ0001IDS.pdf</td>
<td>550881</td>
<td>c9280372376a0e880d3340030b099400</td>
<td>yes</td>
<td>3</td>
</tr>
<tr>
<td>Document Description</td>
<td>Start</td>
<td>End</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-----------------------------------------------------------</td>
<td>-------</td>
<td>-----</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transmittal Letter</td>
<td>1</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Information Disclosure Statement (IDS) Filed (SB/08)</td>
<td>3</td>
<td>3</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Warnings:**

**Information:**

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>NPL Documents</td>
<td>OPF863EPOA.pdf</td>
<td>63687</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>NPL Documents</td>
<td>HuYetal.pdf</td>
<td>949103</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Foreign Reference</td>
<td>EP1605453A2.pdf</td>
<td>2461778</td>
</tr>
</tbody>
</table>

**Warnings:**

**Information:**

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Tac-Gyu KIM

Confirmation No.: 2115

Group Art Unit: 2621

Examiner: Thai Q. TRAN

Serial No.: 11/835,816

Customer No.: 34610

Filed: August 8, 2007

For: DIGITAL VIDEO RECORDER HAVING HIERARCHICAL MEMORIES AND METHOD FOR IMPLEMENTING HIERARCHICAL MEMORIES

INFORMATION DISCLOSURE STATEMENT

U.S. Patent and Trademark Office
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, Virginia 22314

Sir:

Pursuant to 37 C.F.R. § 1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO-1449. One copy of each non-U.S. reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the “References Cited” on any patent to issue therefrom.

Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the indicated date. Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that the information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered. This statement should not be construed as a representation that a search has been made, that information cited in the statement is considered to be and/or is material to patentability, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith. It is further understood that the Examiner will consider information that was cited or submitted to the U.S. Patent and Trademark Office in a prior application relied on under 35 U.S.C. § 120. 1138 OG 37, 38 (May 19, 1992).

1. This Information Disclosure Statement is being filed (i) within three months of the U.S. filing date of a U.S. application other than a CPA continued prosecution application under §1.53(d) OR (ii) within three months of the date of entry of the national stage as set forth in §1.491 in an international application OR (iii) before the mailing date of a first Office Action on the merits OR (iv) before the mailing of a first Office Action after the filing of a Request for continued examination under §1.114. No certification or fee is required. 37 C.F.R. §1.97(b).

2. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection OR Notice of Allowance OR an action that otherwise closes prosecution in the application. 37 C.F.R. §1.97(c).

a. I hereby state that each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. §1.97(e)(1). No fee is required.
b. I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. §1.97(e)(2).

c. Attached is our check no. _____ in the amount of $180.00 in payment of the fee under 37 C.F.R. §1.17(p). Please credit or debit Deposit Account No. 16-0607 as needed to ensure consideration of the disclosed information. Two duplicate copies of this paper are attached.

d. Please charge our Credit Card in the amount of $180.00 in payment of the fee under 37 C.F.R. §1.17(p) per the attached PTO 2038 form. Please credit or debit Deposit Account No. 16-0607 as needed to ensure consideration of the disclosed information. Two duplicate copies of this paper are attached.

3. This Information Disclosure Statement is being filed after the mailing date of a Final Rejection OR Notice of Allowance OR an action that otherwise closes prosecution in the application, but on or before payment of the Issue Fee.

a. Attached is our check no. _____ in the amount of $180.00 in payment of the fee under 37 C.F.R. §1.17(p). Please credit or debit Deposit Account No. 16-0607 as needed to ensure consideration of the disclosed information. Two duplicate copies of this paper are attached. 37 C.F.R. §1.97(d).

b. Please charge our Credit Card in the amount of $180.00 in payment of the fee under 37 C.F.R. §1.17(p) per the attached PTO 2038 form. Please credit or debit Deposit Account No. 16-0607 as needed to ensure consideration of the disclosed information. Two duplicate copies of this paper are attached. 37 C.F.R. §1.97(d).

c. I hereby state that each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. §1.97(e)(1).

d. I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. §1.97(e)(2).

4. The references were cited in a corresponding European application. An English language version of the Office Action issued by the European Patent Office dated May 28, 2009 is attached for the Examiner's information.

5. To the extent necessary, a petition for an extension of time under 37 C.F.R. §1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,
KED & ASSOCIATES, LLP

[Signature]

Daniel Y.J. Kim
Registration No. 36,186

Correspondence Address:
P.O. Box 221200
Chantilly, VA 20153-1200
Telephone: (703) 766-3777
Date: September 1, 2009

Please direct all correspondence to Customer Number 34610

DYK/dsk
\Files\2309\2309-001\206920.doc
34610
KED & ASSOCIATES, LLP
P.O. Box 221200
Chantilly, VA20153-1200

**Title:** DIGITAL VIDEO RECORDER HAVING HIERARCHICAL MEMORIES AND METHOD FOR IMPLEMENTING HIERARCHICAL MEMORIES

**Publication No.** US-2008-0040537-A1
**Publication Date:** 02/14/2008

**NOTICE OF PUBLICATION OF APPLICATION**

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Pre-Grant Publication Division, 703-605-4283
<table>
<thead>
<tr>
<th>APPLICATION NUMBER</th>
<th>FILING or 371(c) DATE</th>
<th>GRP ART UNIT</th>
<th>FIL FEE REC'D</th>
<th>ATTY.DOCKET NO</th>
<th>TOT CLAIMS</th>
<th>IND CLAIMS</th>
</tr>
</thead>
<tbody>
<tr>
<td>11/835,816</td>
<td>08/08/2007</td>
<td>2115</td>
<td>1700</td>
<td>EZ-0001</td>
<td>22</td>
<td>6</td>
</tr>
</tbody>
</table>

CONFIRMATION NO. 2115

FILING RECEIPT

Date Mailed: 08/24/2007

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination’s Filing Receipt Corrections. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a “Notice to File Missing Parts” for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections.

Applicant(s)

Tae-Gyu KIM, Seongnam-si, KOREA, REPUBLIC OF;

Power of Attorney: The patent practitioners associated with Customer Number 34610

Domestic Priority data as claimed by applicant

Foreign Applications

REPUBLIC OF KOREA 10-2006-0075348 08/09/2006

If Required, Foreign Filing License Granted: 08/24/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is US11/835,816

Projected Publication Date: 02/14/2008

Non-Publication Request: No

Early Publication Request: No

Title

DIGITAL VIDEO RECORDER HAVING HIERARCHICAL MEMORIES AND METHOD FOR IMPLEMENTING HIERARCHICAL MEMORIES

Preliminary Class
PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process simplifies the filing of patent applications on the same invention in member countries, but does not result in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

---

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to
espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+); and the Department of Energy.

**NOT GRANTED**

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of

Tae-Gyu KIM

Confirmation No.: 2115

Group Art Unit: To Be Assigned

Serial No.: 11/835,816

Examiner: To Be Assigned

Filed: August 8, 2007

Customer No.: 34610

For: DIGITALVIDEO RECORDER HAVING HIERARCHICAL MEMORIES AND METHOD FOR IMPLEMENTING HIERARCHICAL MEMORIES

TRANSMITTAL OF CERTIFIED PRIORITY DOCUMENT

U.S. Patent and Trademark Office
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, Virginia 22314

Sir:

At the time the above application was filed, priority was claimed based on the following application:


A copy of the priority application listed above is enclosed.

Respectfully submitted,
KED & ASSOCIATES, LLP

John C. Eisenhart
Registration No. 38,128

Correspondence Address:
P.O. Box 221200
Chantilly, VA 20153-1200
703 766-3777 DYK/JCEEdak

Date: August 10, 2007
Please direct all correspondence to Customer Number 34610
This is to certify that the following application annexed hereto is a true copy from the records of the Korean Intellectual Property Office.

출원번호 : 10-2006-0075348
Application Number

출원년월일 : 2006년 08월 09일
Filing Date
AUG 09, 2006

출원인 : 주식회사 휴맥스
Applicant(s)

2007년 07월 20일

COMMISSIONER

*This certificate was issued by Korean Intellectual Property Office. Please confirm any forgery or alteration of the contents by an issue number or a barcode of the document below through the KIPOnet- Online Issue of the Certificates' menu of Korean Intellectual Property Office homepage (www.kipo.go.kr). But please notice that the confirmation by the issue number is available only for 90 days.
【서지사항】
【서류명】 특허출원서
【권리구분】 특허
【수신처】 특허청장
【제출일자】 2006.08.09
【발명의 국문명칭】 계층적 메모리를 구비한 영상 기록 재생 장치 및 계층적 메모리 구현 방법
【발명의 영문명칭】 Digital video recorder having hierarchical memories and method for implementing hierarchical memories

【출원인】
【명칭】 주식회사 휴맥스
【출원인코드】 1-1998-000063-1

【대리인】
【성명】 이경란
【대리인코드】 9-1998-000651-6
【포괄위임등록번호】 2004-073908-7

【발명자】
【성명】 김태규
【성명의 영문표기】 KIM, TAE GYU
【주민등록번호】 740811-1XXXXXXX
【우편번호】 463-010
【주소】 경기도 성남시 분당구 정자동 90 노터마을 416동 1202호
【국적】 KR
【심사청구】 청구
【취지】 특허법 제42조의 규정에 의한 출원, 특허법 제60조의 규정에 의한 출원심사를 청구합니다.

대리인

이경란

(인) 43-1
<table>
<thead>
<tr>
<th>항목</th>
<th>면적</th>
<th>금액</th>
</tr>
</thead>
<tbody>
<tr>
<td>기본출원료</td>
<td>0 면</td>
<td>38,000 원</td>
</tr>
<tr>
<td>가산출원료</td>
<td>41 면</td>
<td>0 원</td>
</tr>
<tr>
<td>우선권주장료</td>
<td>0 건</td>
<td>0 원</td>
</tr>
<tr>
<td>실제청구료</td>
<td>22 항</td>
<td>813,000 원</td>
</tr>
<tr>
<td>합계</td>
<td>851,000 원</td>
<td></td>
</tr>
</tbody>
</table>
【요약서】

【요약】

계층적 메모리를 구비한 영상 기록 재생 장치 및 계층적 메모리 구현 방법이 개시된다. 본 발명의 실시예에 따른 영상 기록 재생 장치는, 휘발성 메모리, 비휘발성 메모리 및 하드디스크를 포함하는 저장부와, 역다중화부로부터 순차적으로 출력되는 오디오 및 비디오 스트림이 휘발성 메모리, 비휘발성 메모리 및 하드디스크의 순서로 이동되어 저장되도록 제어하는 메모리 제어부를 포함한다. 본 발명에 의해, 데이터 특성에 따라 각 저장 수단들을 계층적으로 이용하여 하드디스크의 사용량을 최대한 줄일 수 있다.

【대표도】

도 2

【색인어】

녹화, 디지털, 계층, 메모리
【명세서】

【발명의 명칭】

계층적 메모리를 구비한 영상 기록 재생 장치 및 계층적 메모리 구현 방법
{Digital video recorder having hierarchical memories and method for implementing hierarchical memories}

【도면의 간단한 설명】

<1>  도 1은 종래기술에 따르 PVR 시스템의 구성을 개략적으로 나타낸 블록 구성 도.

<2>  도 2는 본 발명의 바람직한 일 실시예에 따른 영상 기록 재생 장치의 블록 구성도.

<3>  도 3은 본 발명의 바람직한 일 실시예에 따른 메모리 계층 구조를 예시한 도면.

<4>  도 4는 본 발명의 바람직한 일 실시예에 따른 데이터 기록시의 저장 수단의 계층적 운용 방법을 나타낸 순서도.

<5>  도 5는 본 발명의 바람직한 일 실시예에 따른 데이터 재생시의 저장 수단의 계층적 운용 방법을 나타낸 순서도.

<6>  <도면의 주요 부분에 대한 부호의 설명>

<7>  210 : 튜너
220 : 역다중화부
230 : 북호화부
240 : 출력부
250 : 메모리 제어부
260 : 저장부
270 : 휘발성 메모리
280 : 비휘발성 메모리
290 : 하드디스크

【발명의 상세한 설명】

【발명의 목적】

【발명이 속하는 기술분야 및 그 분야의 종래기술】

본 발명은 영상 기록 제생 장치에 관한 것으로, 특히 효율적인 영상 기록 및 제생을 위해 계층적 메모리를 구비한 영상 기록 제생 장치 및 계층적 메모리 구현 방법에 관한 것이다.

 컴퓨터 산업을 시작으로 정보통신산업에까지 확산된 정보의 디지털화는 최근 들어 텔레비전 방송신호에까지 그 범위가 확산되었다. 텔레비전 방송신호의 디지털화는 컴퓨터, 통신분야의 기술과 융합되는 새로운 패러다임이 구현되는 양방향 멀티미디어 시대를 실현할 것이다.
디지털 방송은 유럽의 DVB(Digital Video Broadcasting) 규격과 미국 FCC의 ATV(Advanced TV) 규격을 중심으로 진행되고 있다. 미국이 차세대 TV 방식으로 결정 한 ATSC 규격을 준수한 것으로 기존의 아날로그 TV를 상장하는 NTSC 규격을 대체하 는 것이다.

일반적으로, PVR(Personal Video Recorder; 개인용 비디오 녹화재생장치) 장치는 방송국에서 송출되는 방송신호나 텔레비전 등의 장비로부터 신호를 수신하여 기존의 카세트 테이프(cassette tape)에 아날로그 신호를 저장하는 것과는 달리, 실시간으로 디지털 정보로 변환하고, 그 디지털 데이터를 장치 내에 내장된 대용량 저장장치인 하드디스크(HD)에 MPEG2 방식으로 압축하여 저장시켜둔 후 저장된 녹화 정보를 독출하여 실시간으로 디코딩한 영상을 디스플레이 장치로 송출하는 개인용 비디오 녹화 재생 장치이다.

도 1은 종래기술에 따른 PVR 시스템의 구성을 개략적으로 나타낸 블록 구성 도이다.

도 1을 참조하면, PVR 시스템은 IR 수신부(110), 제어부(120), 메모리(130), 튜너(140), 역타중화부(150), 디코더(160), 출력부(170), OSD부(180), IDE 인터페이스부(185), 하드디스크(Hard Disk Drive, 190)를 포함한다.

IR 수신부(110)는 사용자의 리모트 컨트롤러의 조작에 따른 리모콘 코드 정보를 수신하여 제어부(120)에 전송한다.

제어부(120)는 IR 수신부(110)로부터 수신한 리모콘 코드를 해석하여 리모콘
코드 해석 정보를 해당 장치에 전송한다. 예를 들어, 리모콘 코드 해석 정보가 채널 변경 요구 명령인 경우, 제어부(120)는 채널 변경 요구 명령을 튜너(140)로 전송할 것이다. 또한, 리모콘 코드 해석 정보가 프로그램 녹화 명령인 경우, 수신되는 방송 데이터가 하드디스크(190)에 저장되도록 제어한다. 또한, 제어부(120)는 리모콘 코드 해석 정보가 녹화 목록 요청 명령이라면, 하드디스크(190)에 저장된 녹화 목록을 출력부(170)를 통하여 출력한다.

메모리(130)는 PVR 시스템의 오퍼레이션(operation) 등을 위한 소프트웨어가 저장되는 플래시 드럼과 출력부(170)를 통해 디스플레이할 수 있는 비트맵 형태의 가상화면을 저장하는 DRAM을 포함할 수 있다.

튜너(140)는 제어부(120)에 제어에 의해 선호된 채널의 방송 신호를 수신하여 출력한다.

역다중화부(150)는 튜너(140)로부터 공급되는 방송 신호에 다중화되어 있는 오디오, 비디오, 기타 데이터 등의 여러 정보들을 파싱(parsing)한다.

디코더(160)는 역다중화부(150)에서 파싱되어 얻어지는 오디오 및 비디오 신호, 데이터 신호를 디코딩(decoding)하여 사용자가 인지할 수 있도록 출력부(170)를 통해 출력할 수 있는 시각 정보 및 청각 정보로 처리한다.

OSD부(180)는 제어부(120)로부터 특정 명령이 수행되면 이에 상응하는 상태 정보를 화면상에 표시한다. 예를 들어, 제어부(120)로부터 녹화 목록 출력 명령이 수신되면, 하드디스크(190)에서 추출된 녹화 목록이 출력부(170)를 통해 디스플레이
이도록 제어한다.

IDE 인터페이스부(185)는 녹화를 위해서 상기 역다중화부(150)로부터 전송된 TP(Transport Packet) 데이터를 수신하여 하드디스크(190)로 제공하고, 제어부(120)로부터 재생 요청 명령이 수신되는 경우 하드디스크(190)에 저장된 데이터를 제어부(120)를 통하여 디코더(160)에 전송한다.

하드디스크(190)는 IDE 인터페이스부(185)로부터 전송된 TP 데이터를 저장한다. 즉, 하드디스크(190)에는 사용자의 녹화 명령에 의해 선택된 프로그램을 저장한다.

일반적으로 멀티미디어 데이터는 그 특성상 많은 양의 데이터 흐름을 가진다. 이를 저장하기 위하여 PVR 등의 디지털 녹화 장치는 대용량의 하드디스크를 구비하고 있다.

그러나, 하드디스크는 적은 가격으로 대용량 데이터의 저장이 가능하다는 장점은 있으나, 플래시 메모리(flash memory)에 비해 느린 접근 속도, 동작 속도, 내구성 및 수명의 문제점은 가지고 있다. 여기서, 하드디스크의 내구성 및 수명은 디지털 녹화 장치의 내구성 및 수명을 결정하는 중요한 요소일 수 있다.

또한, 하드디스크를 구비한 종래의 디지털 녹화 장치는 녹화 기능이 이용되지 않는 시간 동안 하드디스크를 스턴바이(stand-by) 모드로 전환하거나 대용량 메모리를 사용하는 방법을 적용하고 있다. 그러나, 실시간(live) 시청을 정지시킬 수 있는 타임 쉐프트(time-shift) 재코딩과 같이 디지털 녹화 장치의 대부분 기능들이 하드디스크의 동작에 기반하기 때문에, 실제로 하드디스크가 스턴바이 모드로 유지
있는 시간은 매우 제한적이며, 대용량 메모리를 구성하는 방법도 하드디스크에 비해 큰 비용을 야기한다는 문제점이 있다. 또한 기계장치인 하드디스크의 동작 소음 및 발생 문제는 가전제품에 적합하지 않을 수 있다.

【발명이 이루고자 하는 기술적 과제】

따라서 본 발명은 상술한 문제점을 해결하기 위한 것으로, 데이터 특성에 따라 각 저장 수단들을 계층적으로 이용하여 하드디스크의 사용량을 최대한 줄일 수 있는 계층적 메모리를 구비한 영상 기록 재생 장치 및 계층적 메모리 구현 방법을 제공하는 것이다.

본 발명의 다른 목적은 하드디스크와 제어부 및 복호부 사이에 메모리를 구성하여 데이터 저장 및 재생을 수행함으로써 보다 빠른 속도로 데이터를 이용할 수 있도록 하고 하드디스크 사용량을 최소화 하는 계층적 메모리를 구비한 영상 기록 재생 장치 및 계층적 메모리 구현 방법을 제공하는 것이다.

그 외의 다른 본 발명의 목적들은 이하에 서술되는 바람직한 실시예를 통하여 보다 명확해질 것이다.

【발명의 구성】

상술한 목적을 달성하기 위하여 본 발명의 일 측면에 따르면, 영상 기록 재생 장치가 제공된다.
본 발명의 바람직한 일 실시예에 따른 영상 기록 재생 장치는, 휘발성 메모리, 비휘발성 메모리 및 하드디스크를 포함하는 저장부; 및 역다중화부로부터 순차적으로 출력되는 오디오 및 비디오 스트림이 상기 휘발성 메모리, 상기 비휘발성 메모리 및 상기 하드디스크의 순서로 이동되어 저장되도록 제어하는 메모리 제어부를 포함한다.

영상 저장절차에 있어서 상기 휘발성 메모리의 저장 영역은 복수의 VM 영역들로 분할되고, 각 VM 영역은 할당된 크기만큼 오디오 및 비디오 스트림을 연속적으로 저장하며, 저장 공간이 모두 이용된 VM 영역에 저장된 오디오 및 비디오 스트림은 상기 메모리 제어부에 의해 상기 비휘발성 메모리로 이동 또는 복사될 수 있다.

상기 비휘발성 메모리의 저장 영역은 버퍼링 영역과 NV 저장 영역을 포함하는 복수의 분할 영역으로 할당되고, 상기 휘발성 메모리의 VM영역에 저장된 오디오 및 비디오 스트림은 상기 NV 저장 영역에 저장되며, 저장 공간이 모두 이용된 상기 NV 저장 영역에 저장된 오디오 및 비디오 스트림은 상기 메모리 제어부에 의해 상기 하드디스크로 이동 또는 복사될 수 있다.

상기 메모리 제어부는 상기 NV 저장 영역의 저장 공간이 모두 이용된 경우 하드디스크로 이동 또는 복사되는 동안 상기 VM 영역들에 저장된 오디오 및 비디오 스트림이 상기 버퍼링 영역에 저장되도록 제어할 수 있다.

상기 메모리 제어부는 상기 NV 저장 영역에 기록된 오디오 및 비디오 스트림의 이동 또는 복사가 완료되면, 상기 버퍼링 영역의 크기를 상기 NV 저장 영역의
크기만큼 확장하여 확장된 버퍼링 영역을 새로운 NV 저장 영역으로 재지정하고, 축소된 NV 저장 영역을 새로운 버퍼링 영역으로 재지정할 수 있다.

상기 저장부에 저장되는 스트림 데이터는 PS(Program Stream) 또는 Partial TS(Transport Stream)일 수 있다.

본 발명의 바람직한 다른 실시예에 따른 영상 기록 재생 장치는, 휘발성 메모리, 비휘발성 메모리 및 하드디스크를 포함하는 저장부; 및 상기 하드디스크에 저장된 스트림 데이터가 휘발성 메모리 또는 비휘발성 메모리로 이동 또는 복사되어도 되는 메모리 제어부를 포함할 수 있다. 여기서, 복호화부는 상기 휘발성 메모리 또는 상기 비휘발성 메모리에 저장된 스트림 데이터를 복호화하여 출력할 수 있다.

영상 재생 절차에 있어서 상기 메모리 제어부는 하드디스크 상에서 상기 비휘발성 메모리로의 스트림 데이터 이동 또는 복사가 완료될 동안 상기 복호화부에 의해 복호화되어 재생될 수 있는 크기의 스트림 데이터를 상기 휘발성 메모리로 이동 또는 복사할 수 있다.

상기 비휘발성 메모리에는 연속적인 영상 재생을 위해서 상기 휘발성 메모리에 기록된 스트림 데이터에 후속하는 스트림 데이터가 기록될 수 있다.

상기 복호화부는 상기 휘발성 메모리에 기록된 스트림 데이터의 복호화가 완료되면 연속하여 상기 비휘발성 메모리에 저장된 스트림 데이터를 복호화하여 출력할 수 있다.
상기 스트림 데이터는 PS(Program Stream) 또는 Partial TS(Transport Stream)일 수 있다.

상술한 목적을 달성하기 위하여 본 발명의 다른 측면에 따르면, 영상 기록 재생 장치의 스트림 데이터 저장 방법 및/또는 스트림 데이터 재생 방법이 제공된다.

본 발명의 바람직한 일 실시에 따른 영상 기록 재생 장치의 스트림 데이터 저장 방법은, (a) 역다중화부로부터 순차적으로 출력되는 오디오 및 비디오 스트림이 미리 지정된 크기의 스트림 데이터로 휘발성 메모리에 촉적되면 비휘발성 메모리로 이동 저장되도록 하는 단계; 및 (b) 상기 단계 (a)의 반복 수행으로 상기 비휘발성 메모리에 미리 지정된 크기의 스트림 데이터가 촉적되거나 상응하는 방송 프로그램의 스트림 데이터 촉적이 완료되면 하드디스크로 이동 저장되도록 하는 단계를 포함할 수 있다.

상기 휘발성 메모리의 저장 영역이 제1 분할 영역 및 제2 분할 영역으로 할당된 경우, 상기 단계 (a)는 제1 분할 영역에 스트림 데이터의 촉적을 개시하는 단계; 상기 제1 분할 영역의 저장 공간이 모두 이용되면 촉적된 스트림 데이터를 상기 비휘발성 메모리로 이동 저장되도록 하고, 후속하는 오디오 및 비디오 스트림에 대한 스트림 데이터가 제2 분할 영역에 촉적되도록 제어하는 단계; 및 상기 제2 분할 영역의 저장 공간이 모두 이용되면 촉적된 스트림 데이터를 상기 비휘발성 메모리로 이동 저장되도록 하고, 후속하는 오디오 및 비디오 스트림에 대한 스트림 데이터의 촉적을 개시하는 단계.
이터가 상기 제1 분할 영역에 축적되도록 제어하는 단계를 포함할 수 있다.

상기 비휘발성 메모리의 저장 영역이 버퍼링 영역과 NV 저장 영역으로 할당된 경우, 상기 단계 (b)는 상기 NV 저장 영역에 상기 스트림 데이터의 축적을 개시하는 단계; 및 상기 NV 저장 영역의 저장 공간이 모두 이용되면 축적된 스트림 데이터를 상기 버퍼링 영역에 축적되도록 제어하는 단계를 포함할 수 있다. 여기서, 상기 NV 저장 영역에 축적된 스트림 데이터의 이동이 완료되면, 상기 버퍼링 영역은 상기 NV 저장 영역의 저장 공간만큼 확장되어 새로운 NV 저장 영역으로 재지정되고, 나머지 저장 공간이 새로운 버퍼링 영역으로 재지정될 수 있다.

상기 버퍼링 영역은 상기 NV 저장 영역에 축적된 스트림 데이터가 상기 하드 디스크로 이동 저장하기 위한 시간 동안 후속하는 스트림 데이터를 축적할 수 있는 크기의 저장 공간을 가질 수 있다.

본 발명의 바람직한 다른 실시예에 따르는 영상 기록 재생 장치의 스트림 데이터 재생 방법은, 하드디스크에 저장된 스트림 데이터들 중 앞선 재생 순서인 입력의 크기의 스트림 데이터가 회발성 메모리에 저장되도록 하는 단계; 및 상기 회발성 메모리에 저장된 스트림 데이터에 후속하는 스트림 데이터들이 비회발성 메모리에 저장되도록 하는 단계를 포함할 수 있다. 여기서, 상기 회발성 메모리에 저장되는 스트림 데이터의 크기는 최소한 상기 비회발성 메모리에 후속하는 스트림 데이터들이 저장되는 시간만큼 재생 처리될 수 있는 크기일 수 있다.

복호화부는 상기 회발성 메모리에 저장된 스트림 데이터의 복호화가 완료되
면 상기 비휘발성 메모리에 저장된 후속하는 스트림 데이터들을 복호화하도록 제어될 수 있다.

상기 스트림 데이터는 PS(Program Stream) 또는 Partial TS(Transport Stream)일 수 있다.

상술한 목적을 달성하기 위하여 본 발명의 또 다른 측면에 따르면, 영상 기록 재생 장치의 스트림 데이터 저장 방법 및/또는 스트림 데이터 재생 방법이 기록된 기록매체가 제공된다.

본 발명의 바람직한 일부 실시예에 따르면, 스트림 데이터 저장 방법을 수행하기 위해 영상 기록 재생 장치에 의해 실행될 수 있는 명령어들의 프로그램이 유형적으로 구현되어 있으며, 상기 영상 기록 재생 장치에 의해 판독될 수 있는 프로그램을 기록한 기록매체에 있어서, (a) 역다중화부로부터 순차적으로 출력되는 오디오 및 비디오 스트림이 미리 저장된 크기의 스트림 데이터로 회복발성 메모리에 축적되며, 비휘발성 메모리로 이동 저장되도록 하는 단계; 및 (b) 상기 단계 (a)의 반복 수행으로 상기 비휘발성 메모리에 미리 저장된 크기의 스트림 데이터가 축적되거나 상응하는 방송 프로그램의 스트림 데이터 축적이 완료되면 하드디스크로 이동 저장되도록 하는 단계를 실행하는 것을 특징으로 하는 프로그램이 기록된 기록매체가 제공된다.

상기 회복발성 메모리의 저장 영역이 제1 분할 영역 및 제2 분할 영역으로 할당된 경우 상기 단계 (a)는, 제1 분할 영역에 스트림 데이터의 축적을 개시하는 단
계; 상기 제1 분할 영역의 저장 공간이 모두 이용되면 축적된 스트림 데이터를 상
기 비휘발성 메모리로 이동 저장되도록 하고, 후속하는 오디오 및 비디오 스트림에
대한 스트림 데이터가 제2 분할 영역에 축적되도록 제어하는 단계; 및 상기 제2 분
할 영역의 저장 공간이 모두 이용되면 축적된 스트림 데이터를 상기 비휘발성 메모
리로 이동 저장되도록 하고, 후속하는 오디오 및 비디오 스트림에 대한 스트림 데
이터가 상기 제1 분할 영역에 축적되도록 제어하는 단계를 포함할 수 있다.

상기 비휘발성 메모리의 저장 영역이 버퍼링 영역과 NV 저장 영역으로 할당
된 경우 상기 단계 (b)는, 상기 NV 저장 영역에 상기 스트림 데이터의 축적을 개시
하는 단계; 및 상기 NV 저장 영역의 저장 공간이 모두 이용되면 축적된 스트림 데
이터를 상기 하드디스크로 이동 저장되도록 하고, 후속하는 스트림 데이터가 상기
버퍼링 영역에 축적되도록 제어하는 단계를 포함할 수 있다. 여기서, 상기 NV 저장
영역에 축적된 스트림 데이터의 이동이 완료되면, 상기 버퍼링 영역은 상기 NV 저장
영역의 저장 공간만큼 확장되어 새로운 NV 저장 영역으로 재지정되고, 나머지
저장 공간이 새로운 버퍼링 영역으로 재지정될 수 있다.

본 발명의 바람직한 다른 실시예에 따르면, 스트림 데이터 재생 방법을 수행
하기 위해 영상 기록 재생 장치에 의해 실행될 수 있는 명령어들의 프로그램이 유
형적으로 구현되어 있으며, 상기 영상 기록 재생 장치에 의해 판독될 수 있는 프로
그래프를 기록한 기록매체에 있어서, 하드디스크에 저장된 스트림 데이터들 중 앞선
재생 순서인 임의의 크기의 스트림 데이터가 휘발성 메모리에 저장되도록 하는 단
계; 및 상기 휘발성 메모리에 저장된 스트림 데이터에 후속하는 스트림 데이터들이
비례발생 메모리에 저장되도록 하는 단계를 실행하되, 상기 회발성 메모리에 저장되는 스트림 데이터의 크기는 최소한 상기 비례발생 메모리에 흡수하는 스트림 데이터들이 저장되는 시간만큼 재생 처리될 수 있는 크기인 것을 특징으로 하는 프로그램이 기록된 기록매체가 제공된다.

본 발명은 다양한 변경을 가할 수 있고 여러 가지 실시예를 가질 수 있는 바, 특정 실시예들을 도면에 예시하고 상세한 설명에 상세하게 설명하고자 한다. 그러나, 이는 본 발명을 특정한 실시 형태에 대해 한정하려는 것이 아니며, 본 발명의 사상 및 기술 범위에 포함되는 모든 변경, 균등율 내지 대체물들을 포함하는 것으로 이해되어야 한다. 각 도면을 설명하면서 유사한 참조부호를 유사한 구성요소에 대해 사용하였다. 본 발명을 설명함에 있어서 관련된 공지 기술에 대한 구체적인 설명이 본 발명의 요지를 흐릴 수 있다고 판단되는 경우 그 상세한 설명을 생략한다.

제1, 제2 등의 용어는 다양한 구성요소들을 설명하는데 사용될 수 있지만, 상기 구성요소들은 상기 용어들에 의해 한정되어서는 안 된다. 상기 용어들은 하나의 구성요소를 다른 구성요소로부터 구별하는 목적으로만 사용된다. 예를 들어, 본 발명의 권리 범위를 벗어나지 않으면서 제1 구성요소는 제2 구성요소로 명명될 수 있고, 유사하게 제2 구성요소도 제1 구성요소로 명명될 수 있다. 및/또는 이라는 용어는 복수의 관련된 기재된 항목들의 조합 또는 복수의 관련된 기재된 항목들 중의 어느 항목을 포함한다.
어떤 구성요소가 다른 구성요소에 "연결되어" 있거나 "접속되어" 있다고 언급된 때에는, 그 다른 구성요소에 직접적으로 연결되어 있거나 또는 접속되어 있을 수도 있지만, 중간에 다른 구성요소가 존재할 수도 있다고 이해되어야 할 것이 다. 반면에, 어떤 구성요소가 다른 구성요소에 "직접 연결되어" 있거나 "직접 접속되어" 있다고 언급된 때에는, 중간에 다른 구성요소가 존재하지 않는 것으로 이해되어야 할 것이다.

본 출원에서 사용한 용어는 단지 특정한 실시예를 설명하기 위해 사용된 것으로, 본 발명을 한정하려는 의도가 아니다. 단수의 표현은 문맥상 명백하게 다르게 뜻하지 않는 한, 복수의 표현을 포함한다. 본 출원에서, "포함하다" 또는 "가지다" 등의 용어는 명세서상에 기재된 특정, 숫자, 단계, 동작, 구성요소, 부품 또는 이들을 조합한 것이 존재함을 지정하려는 것이지, 하나 또는 그 이상의 다른 특징들이나 숫자, 단계, 동작, 구성요소, 부품 또는 이들을 조합한 것들의 존재 또는 부가 가능성을 미리 배제하지 않는 것으로 이해되어야 한다.

다르게 정의되지 않는 한, 기술적이거나 과학적인 용어를 포함해서 여기서 사용되는 모든 용어들은 본 발명이 속하는 기술 분야에서 통상의 지식을 가진 자에 의해 일반적으로 이해되는 것과 동일한 의미를 가지고 있다. 일반적으로 사용되는 사전에 정의되어 있는 것과 같은 용어들은 관련 기술의 문맥상 가지는 의미와 일치하는 의미를 가지는 것으로 해석되어야 하며, 본 출원에서 명백하게 정의하지 않는 한, 이상적이거나 과도하게 형식적인 의미로 해석되지 않는다.

이하, 첨부된 도면을 참조하여 본 발명에 따른 바람직한 실시예를 상세히 설
명하되, 도면 부호에 관계없이 동일하거나 대응하는 구성 요소는 동일한 참조 번호
를 부여하고 이에 대한 중복되는 설명은 생략하기로 한다.

도 2는 본 발명의 바람직한 일 실시예에 따른 영상 기록 재생 장치의 블록
구성도이고, 도 3은 본 발명의 바람직한 일 실시예에 따른 메모리 계층 구조를 예
시한 도면이다.

도 2를 참조하면, 본 발명의 바람직한 실시예에 따른 영상 기록 재생 장치는
튜너(210), 역다중화부(220), 복호화부(230), 출력부(240), 메모리 제어부(250) 및
저장부(260)를 포함한다. 저장부(260)는 휘발성 메모리(270), 비휘발성 메모리
(280) 및 하드디스크(290)를 포함할 수 있다.

튜너(210)는 재생 제어부(도시되지 않음)에 제어에 의해 선국된 채널의 방송
신호를 수신하여 출력한다. 재생 제어부는 영상 기록 재생 장치의 동작을 제어하는
메인 제어부일 수 있다.

역다중화부(220)는 튜너(140)로부터 공급되는 방송 신호에 다중화되어 있는
오디오, 비디오, 기타 데이터 등의 여러 정보들을 역다중화한다. 또한 역다중화부
(220)는 튜너를 통해 수신된 방송 신호들 중 사용자의 선국 입력에 따라 선택된 방
송 프로그램을 역다중화하여 선국된 방송 프로그램을 비디오 및 오디오 스트림으로
추출한다. 역다중화부(220)에 의해 추출되어 출력되는 방송 신호는 MPEG 데이터(예
를 들어, PS(Program Stream) 또는/및 Partial TS(Transport Stream) 등) 형태일
수 있다.

복호화부(230)는 역다중화부(220)에서 파생되어 얻어지는 오디오 및 비디오
스트림 등을 디코딩(decoding)하여 사용자가 인지할 수 있도록 출력부(240)를 통해 출력할 수 있는 시각 정보 및 청각 정보로 처리한다.

<73>
 출력부(240)는 복호화부(230)로부터 출력되는 디코딩된 오디오 및 비디오 신호 등을 시각 정보 및/또는 청각 정보로 출력한다. 출력부(240)는 표시부, 스피커부 등을 포함할 수 있다.

<74>
 메모리 제어부(250)는 역다중화부(220)로부터 출력되는 비디오 및 오디오 스트림이 저장될 저장 수단을 지정하여 해당 비디오 및 오디오 스트림이 복수의 저장 수단간의 계층적 구조에 따라 저장되도록 한다. 또한, 메모리 제어부(250)는 저장 수단의 계층적 구조에 따라 저장된 데이터들이 독립되어 복호화부(230) 및 출력부(240)를 통해 출력되도록 한다.

<75>
 저장부(260)는 휘발성 메모리(270), 비휘발성 메모리(270) 및 하드디스크(290)를 포함한다. 각 저장 수단에 저장되는 비디오 및 오디오 스트림은 PS(Program Stream) 또는/및 Partial TS(Transport Stream) 형태일 수 있다.

<76>
 휘발성 메모리(270)는 자유로운 읽기/쓰기가 가능하며 동작 속도는 가장 빠르지만, 전원 공급이 차단되면 저장된 데이터를 잃어버리는 특징을 가진다. 휘발성 메모리(270)는 예를 들어 램(RAM)일 수 있다. 도 3에 예시된 바와 같이, 휘발성 메모리(270)는 논리적으로 복수의 영역으로 분할될 수 있다. 예를 들어, 2개의 영역으로 분할되는 경우 휘발성 메모리(270)는 제1 VM(Volatile Memory) 영역(310) 및 제2 VM 영역(320)으로 분할될 수 있다.

<77>
 비휘발성 메모리(270)는 불록 단위의 읽기/쓰기가 가능하지만, 속도가 메모리

43-19
리 보다 느린 단점을 있다. 비휘발성 메모리(270)는 예를 들어 플래시 메모리일 수 있다. 도 3에 예시된 바와 같이, 비휘발성 메모리(270)는 논리적으로 복수의 영역으로 분할될 수 있다. 예를 들어, 2개의 영역으로 분할되는 경우 휘발성 메모리(270)는 비퍼링 영역(330) 및 NV(NonVolatile) 영역(340)으로 분할될 수 있다.

하드디스크(290)는 대용량의 데이터 저장 및 유지가 가능하지만, 동작 속도가 느리고 동작 소음을 발생하는 등의 문제점을 가지고 있다.

본 발명은 각 저장 수단의 장점을 극대화하면서 단점을 최소화하는 방법을 적용하여 각 저장 수단간의 계층적 구조를 적용한다. 즉, 메모리 제어부(250)는 저장부(260)에 구비된 각 저장 수단을 제어함에 있어, 역다중화부(220)로부터 출력되는 비디오 및 오디오 스트림이 저장 수단에 저장되는 경우 휘발성 메모리(270), 비휘발성 메모리(270) 및 하드디스크(290)의 계층 구조를 사용하여 제어함을 특징으로 한다. 이에 비해, 각 저장 수단에 저장된 데이터를 재생하는 경우에는 하드디스크(290), 비휘발성 메모리(270) 및 휘발성 메모리(270)의 계층 구조 또는 하드디스크(290), 휘발성 메모리(270) 및 비휘발성 메모리(270)의 계층 구조로 제어함을 특징으로 한다.

이하 도 3 내지 도 5를 참조하여 본 발명에 따른 영상 기록 재생 장치의 저장 수단 계층적 운용 방법에 대해 상세히 설명하기로 한다.

도 4는 본 발명의 바람직한 일 실시예에 따른 데이터 기록시의 저장 수단의
제출적 운용 방법을 나타낸 순서도이다.

도 4를 참조하면, 단계 410에서 메모리 제어부(250)는 사용자의 방송 데이터 저장 명령에 상응하여 역다중화부(220)로부터 출력되는 오디오 및 비디오 스트림을 휘발성 메모리(270)의 제1 VM 영역(310)에 저장한다.

단계 415에서 메모리 제어부(250)는 역다중화부(220)로부터 연속적으로 출력되는 오디오 및 비디오 스트림을 휘발성 메모리(270)의 제1 VM 영역(310)에 저장하는 과정에서 제1 VM 영역(310)의 저장 공간이 모두 이용되었는지 여부를 판단한다.

만일, 제1 VM 영역(310)의 저장 공간이 남아있는 경우에는 단계 410으로 진행하여 역다중화부(220)로부터 출력되는 오디오 및 비디오 스트림이 휘발성 메모리(270)의 제1 VM 영역(310)에 계속 저장되도록 제어한다.

그러나, 만일 제1 VM 영역(310)의 저장 공간이 모두 이용되었다면 단계 420으로 진행하여, 메모리 제어부(250)는 제2 VM 영역(320)에 후속하는 오디오 및 비디오 스트림을 저장되도록 제어한다. 또한, 메모리 제어부(250)는 제1 VM 영역에 기록된 데이터가 비휘발성 메모리(270)의 NV 저장 영역(340)에 기록되도록 제어한다 (단계 420, 단계 435).

상술한 바와 같이, 휘발성 메모리(270)의 저장 공간은 둘 이상의 분할 영역으로 분할되어 하나의 분할 영역만큼 오디오 및 비디오 스트림이 저장되면, 후속하는 오디오 및 비디오 스트림은 다른 분할 영역에 이어서 저장된다. 다른 분할 영역에 오디오 및 비디오 스트림이 저장되는 동안 진행하는 오디오 및 비디오 스트림이 저장된 분할 영역에 기록된 데이터가 비휘발성 메모리(270)의 NV 저장 영역(340)으로
로 저장되고, 저장이 완료되면 해당 분할 영역에 기록된 데이터는 삭제된다. 예를 들어, 도 3에 예시된 바와 같이 휘발성 메모리가 제1 VM 영역(310)과 제2 VM 영역(320)으로 구성되고, 순차적으로 이용되는 경우, 제2 VM 영역(320)에 오디오 및 비디오 스트림이 저장되는 동안 제1 VM 영역(310)에 기록된 데이터는 비휘발성 메모리(270)의 NV 저장 영역(340)에 기록된다. 다만, 제2 VM 영역(320)에 오디오 및 비디오 스트림의 기록이 완료되기 전에 제1 VM 영역(310)에 기록된 데이터가 모두 비휘발성 메모리(270)의 NV 저장 영역(340)으로 이동 또는 복사되어야 할 것이다. 물론, 제1 VM 영역(310)의 저장 공간이 모두 이용되기 전에 오디오 및 비디오 스트림의 기록이 완료된 경우, 제2 VM 영역(320)은 더 이상 이용되지 않아야 하며, 메모리 제어부(250)의 제어에 의해 제1 VM 영역(310)에 기록된 오디오 및 비디오 스트림이 NV 저장 영역(340)으로 이동 또는 복사될 것이다.

단계 425에서 메모리 제어부(250)는 역다중화부(220)로부터 연속적으로 출력되는 오디오 및 비디오 스트림을 휘발성 메모리(270)의 제2 VM 영역(320)에 저장하는 과정에서 제2 VM 영역(320)의 저장 공간이 모두 이용되었는지 여부를 판단한다.

만일, 제2 VM 영역(320)의 저장 공간이 남아있는 경우에는 단계 420으로 다시 진행하여 역다중화부(220)로부터 출력되는 오디오 및 비디오 스트림이 휘발성 메모리(270)의 제2 VM 영역(320)에 계속 저장되도록 제어한다. 이 경우, 제2 VM 영역(320)의 저장 공간이 모두 이용되기 전에 오디오 및 비디오 스트림의 기록이 완료된 경우, 상용하는 오디오 및 비디오 스트림의 기록을 위해 제1 VM 영역(310)은 더 이상 이용되지 않을 것이며, 메모리 제어부(250)의 제어에 의해 제2 VM 영역
(320)에 기록된 오디오 및 비디오 스트림이 NV 저장 영역(340)으로 이동 또는 복사될 것이다.

그러나, 반일 제2 VM 영역(320)의 저장 공간이 모두 이용되었다면 단계 430으로 진행하여, 메모리 제어부(250)는 제1 VM 영역(310)에 후속하는 오디오 및 비디오 스트림이 저장되도록 제어한다. 또한, 메모리 제어부(250)는 제2 VM 영역에 기록된 데이터가 비휘발성 메모리(270)의 NV 저장 영역(340)에 기록되도록 제어한다(단계 430, 단계 435).

단계 435에서 메모리 제어부(250)는 제1 VM 영역(310) 또는 제2 VM 영역(320)에 기록된 오디오 및 비디오 스트림이 NV 저장 영역(340)에 저장되도록 제어한다. 여기서, NV 저장 영역(340)의 크기는 방송 프로그램의 보편적인 1회 녹화 분량에 준하도록 설정함이 바람직하다. 보편적인 1회 녹화 분량은 디지털 방송에 따라 상이할 수 있으나 DVB SD급의 경우 4Mbps정도의 bit rate를 가지고 있으므로 2시간에 약 3.5 Gbyte 정도의 분량으로 산출될 수 있다. 즉 방송 환경의 전송률에 따라 조정되거나 미리 설정될 수 있다.

단계 440에서 메모리 제어부(250)는 NV 저장 영역(340)의 저장 공간이 모두 이용되었는지 여부를 판단한다.

반일, NV 저장 영역(340)의 저장 공간이 남아있는 경우에는, 단계 435로 다시 진행하여 메모리 제어부(250)는 제1 VM 영역(310) 또는 제2 VM 영역(320)으로부터 수신되는 오디오 및 비디오 스트림이 NV 저장 영역(340)의 저장 공간에 계속 저장되도록 제어한다.
그러나, 만일 NV 저장 영역(340)의 저장 공간이 모두 이용되었다면 단계 445로 진행하여, 메모리 제어부(250)는 버퍼링 영역(330)에 후속하는 오디오 및 비디오 스트림이 저장되도록 제어한다. 또한, 메모리 제어부(250)는 NV 저장 영역에 기록된 데이터가 하드디스크(290)의 HDD 저장 영역(350)에 저장되도록 제어한다(단계 445, 단계 460).

단계 450에서, 메모리 제어부(250)는 NV 저장 영역(340)에 기록된 오디오 및 비디오 스트림이 모두 하드디스크(290)로 이동 또는 복사되었는지 여부를 판단한다.

만일, 해당 오디오 및 비디오 스트림이 모두 하드디스크로 이동 또는 복사되지 않았다면 단계 445로 다시 진행한다. 그러나 만일 해당 오디오 및 비디오 스트림이 모두 하드디스크로 이동 또는 복사되었다면 단계 455로 진행하여 버퍼링 영역(330, 즉 휘발성 메모리(270)로부터 현재 오디오 및 비디오 스트림이 이동 또는 복사되고 있는 비휘발성 메모리(270)의 분할된 저장 영역)을 확장하여 NV 저장 영역(340)으로 재지정하고, 나머지 영역을 버퍼링 영역(330)으로 재지정한다. 이 경우, 버퍼링 영역(330)은 처음 NV 저장 영역(340)이 할당된 크기만큼 확장하여 NV 저장 영역(340)으로 재지정됨으로써, 버퍼링 영역(330)과 NV 저장 영역(340)의 크기는 일정하게 유지될 수 있다. 또한, 버퍼링 영역(330)의 최초 크기는 최소한 NV 저장 영역(340)에 저장된 오디오 및 비디오 스트림이 하드디스크(290)로 모두 이동 또는 복사되는 시간 동안 휘발성 메모리(270)로부터 이동 또는 복사되는 오디오 및 비디오 스트림을 저장할 수 있는 저장 용량의 크기를 가지고도 지정되어야 할 것이다.
상술한 바와 같이, 본 발명에 따른 비휘발성 메모리(270)도 2개 이상의 저장 영역을 가지고 논리적으로 분할됨으로써, 어느 하나의 분할 영역의 저장 공간이 모두 이용된 경우 해당 분할 영역에 기록된 데이터들을 하드디스크(290)로 이동 또는 복사하는 동안 다른 분할 영역에 후속하는 데이터들이 기록되도록 함으로써 데이터의 연속성을 보장할 수 있는 특징을 가진다.

다만, 상술한 바와 같이 NV 저장 영역(340)이 하나의 방송 프로그램에 상용하는 오디오 및 비디오 스트림들을 모두 저장 가능한 저장 용량으로 할당되는 경우, 버퍼링 영역(330)에 후속하는 오디오 및 비디오 스트림들의 저장은 실행되지 않을 것이다. 또한, 사용자의 방송 프로그램 저장 명령에 따른 오디오 및 비디오 스트림의 저장이 완료된 경우 해당 오디오 및 비디오 스트림은 하드디스크(290)로 이동 또는 복사될 것이다. 사용자의 저장 명령에 상용하는 방송 프로그램의 오디오 및 비디오 스트림이 모두 저장되었는지 여부는 각 방송 프로그램에 상용하도록 할당된 식별자 또는 방송 시간 등을 이용하여 판단할 수 있으며, 이를 판단하는 방법은 담당자에게 자명하므로 이에 대한 설명은 생략한다.

앞서 설명한 데이터 기록시의 저장 수단의 계층적 운영에 의해 하드디스크 (290)에 기록된 데이터를 재생하는 과정을 이하 도 5를 참조하여 설명한다.

도 5는 본 발명의 바람직한 일 실시예에 따른 데이터 재생시의 저장 수단의 계층적 운영 방법을 나타낸 순서도이다.
도 5를 참조하면, 단계 510에서 메모리 제어부(250)는 하드디스크(290)에 저장된 오디오 및 비디오 스트림들 중 원의 크기의 오디오 및 비디오 스트림을 휘발 성 메모리(350, 즉 제1 VM 영역(310) 또는 제2 VM 영역(320))로 이동 또는 복사(이하, '복사'라 통칭함)되도록 제어한다. 해당 오디오 및 비디오 스트림의 복사 주체는 메모리 제어부(250)일 수 있다. 또한, 재생 제어부 또는 메모리 제어부(250)는 휘발성 메모리(270)에 저장된 데이터를 이용하여 복호화부(230)가 복호화를 수행하여 복호화된 오디오 및 비디오 데이터가 출력부(240)를 통해 출력되도록 제어한다. 휘발성 메모리(270)로 복사하는 오디오 및 비디오 스트림의 최소 크기는 추후하여 재생된 오디오 및 비디오 스트림들이 하드디스크(290)로부터 비휘발성 메모리의 NV 저장 영역(340)으로 복사 완료되기 위한 시간만큼 재생을 위해 이용될 수 있는 크기이다. 메모리 제어부(250)가 초기에 재생된 오디오 및 비디오 스트림들을 휘발성 메모리(270)에 기록하는 이유는 휘발성 메모리(270)에 기록된 데이터의 처리가 보다 신속할 수 있기 때문이다. 물론, 초기에 재생된 오디오 및 비디오 스트림들은 버퍼링 영역(330)에 복사하여 재생하는 동안 추속하는 오디오 및 비디오 스트림들이 NV 저장 영역(340)에 복사되도록 할 수도 있음을 자명하다.

단계 520에서 메모리 제어부(250)는 단계 510을 통해 휘발성 메모리(270)로 복사된 오디오 및 비디오 스트림에 이어지는 오디오 및 비디오 스트림들을 하드디스크(290)로부터 NV 저장 영역(340)에 복사한다. 재생 제어부 또는 메모리 제어부 (250)는 휘발성 메모리(270)에 저장된 데이터를 이용한 재생이 완료되면, 비휘발성 메모리(270)의 NV 저장 영역(340)에 기록된 오디오 및 비디오 스트림들을 이용하여
복호화부(230)가 복호화를 수행하여 복호화된 오디오 및 비디오 데이터가 출력부(240)를 통해 출력되도록 제어한다.

단계 530에서 메모리 제어부(250)는 현재 재생되는 방송 프로그램에 상응하여 추속하여 재생되어야 하는 오디오 및 비디오 스트림들이 하드디스크(290)에 남아있는지 여부를 판단한다. 단계 530은 NV 저장 영역(340)에 복사된 오디오 및 비디오 스트림들을 재생하는 도중 임의의 시점에서 수행될 수 있다. 다만, 후속하여 재생될 오디오 및 비디오 스트림이 존재할 수 있으므로, 해당 데이터 전체 또는 일부가 휘발성 메모리(270) 또는 버퍼링 영역(330)에 복사되기 위해 필요한 시간이 전에 수행됨이 바람직할 것이다.

이는, 메모리 제어부(250) 또는 영상 기록 재생 장치가 특정 저장 수단에 기록된 데이터를 타 저장 수단으로 복사하기 위한 시간(즉, 전송 속도 및 전송할 데이터량을 이용하여 산출될 수 있음)과 특정 저장 수단에 기록된 데이터를 이용하여 재생하는 시간(즉, 재생 속도 및 재생할 데이터량을 이용하여 산출될 수 있음)을 이용하여 결정될 수 있다.

상술한 바와 같이, NV 저장 영역(340)의 저장 공간 크기가 하나의 방송 프로그램을 저장할 수 있는 용량으로 할당되었거나 후속하여 재생될 오디오 및 비디오 스트림들이 하드디스크(290)에 존재하지 않는 경우 단계 530 및 이후의 단계는 생략될 수 있을 것이다.

그러나 만일 후속하여 재생될 오디오 및 비디오 스트림들이 하드디스크(290)에 존재하는 경우, 메모리 제어부(250)는 단계 540에서 하드디스크(290)에 저장
된 오디오 및 비디오 스트림들 중 NV 저장 영역(340)에 복사된 오디오 및 비디오 스트립에 이어지는 임의 크기의 오디오 및 비디오 스트립이 휘발성 메모리(270)에 복사되도록 제어한다. 단계 540에 의해 복사된 오디오 및 비디오 스트립은 단계 520에 의해 NV 저장 영역(340)에 복사된 오디오 및 비디오 스트림들의 재생이 완료된 후 재생을 위해 이용될 것이다. 해당 오디오 및 비디오 스트립이 버퍼링 영역 (330)에 복사될 수도 있음을 상술한 바와 같다. 단계 540이 수행되는 이유는 앞서 설명한 단계 510과 같다.

단계 550에서 메모리 제어부(250)는 단계 540에서 휘발성 메모리(270)에 기록된 오디오 및 비디오 스트림에 이어지는 오디오 및 비디오 스트림들이 휘발성 메모리(270)의 NV 저장 영역(340)에 복사되도록 제어한다. 만일 단계 540을 통해 휘발성 메모리(270) 또는 버퍼링 영역(330)에 기록된 오디오 및 비디오 스트림이 해당 방송 프로그램에 상응하는 마지막 오디오 및 비디오 스트림인 경우 단계 550은 생략될 수 있을 것이다.

상술한 바와 같이, 본 발명에 따른 영상 기록 재생 장치는 하드디스크(290)에 기록된 오디오 및 비디오 스트림들을 재생함에 있어 하드디스크(290)에 해당 데이터들이 존재하는 상태로 재생하지 않고, 해당 데이터들을 휘발성 메모리(270) 또는 비휘발성 메모리(270)에 임의의 크기만큼 복사한 후 복사된 데이터들을 이용하여 재생하는 특징을 가진다.

즉, 본 발명에 따른 영상 기록 재생 장치는 저장부(260)에 데이터를 기록하거나 저장부(260)에 기록된 데이터를 이용한 재생을 수행하는 경우 각 저장 수단들
을 계층적 운용함으로써 중래의 데이터 저장 시간 및 재생을 위한 대기 시간 등을 최소화할 수 있다. 또한, 데이터 저장시 비휘발성 메모리(270)에 저장된 데이터들을 하드디스크(290)로 일괄 전송하는 경우 및 데이터 재생시 하드디스크에 저장된 데이터들을 휘발성 메모리(270) 또는 비휘발성 메모리(270)로 일괄 전송하는 경우 등에만 하드디스크(290)가 이용되도록 함으로써 중래의 데이터 저장 및 재생 방식에 비해 하드디스크(290) 이용량을 최소화할 수 있다.

【발명의 효과】

상술한 바와 같이 본 발명에 따른 계층적 메모리를 구비한 영상 기록 재생 장치 및 계층적 메모리 구현 방법은 데이터 특성에 따라 각 저장 수단들을 계층적으로 이용하여 하드디스크의 사용량을 최대한 줄일 수 있는 효과가 있다.

또한, 본 발명은 하드디스크보다 동작 속도가 빠른 메모리를 이용하여 데이터 저장 및 재생을 수행함으로써 보다 빠른 속도로 데이터를 이용할 수 있도록 하는 효과도 있다.

상기에서는 본 발명의 바람직한 실시예를 참조하여 설명하였지만, 해당 기술 분야에서 통상의 지식을 가진 자라면 하기의 특허 정구의 범위에 기재된 본 발명의 사상 및 영역으로부터 벗어나지 않는 범위 내에서 본 발명을 다양하게 수정 및 변경시킬 수 있음을 이해할 수 있을 것이다.
【특허청구범위】

【청구항 1】

영상 기록 재생 장치에 있어서,

휘발성 메모리, 비휘발성 메모리 및 하드디스크를 포함하는 저장부; 및

역다중화부로부터 순차적으로 출력되는 오디오 및 비디오 스트림이 상기 휘발성 메모리, 상기 비휘발성 메모리 및 상기 하드디스크의 순서로 이동되어 저장되도록 제어하는 메모리 제어부를 포함하는 영상 기록 재생 장치.

【청구항 2】

제1항에 있어서,

상기 휘발성 메모리의 저장 영역은 복수의 VM 영역들로 분할되고, 각 VM 영역은 할당된 크기만큼 오디오 및 비디오 스트림을 연속적으로 저장하며, 저장 공간이 모두 이용된 VM 영역에 저장된 오디오 및 비디오 스트림은 상기 메모리 제어부에 의해 상기 비휘발성 메모리로 이동 또는 복사되는 것을 특정으로 하는 영상 기록 재생 장치.

【청구항 3】

제2항에 있어서,

상기 비휘발성 메모리의 저장 영역은 비퍼링 영역과 NV 저장 영역을 포함하.
는 복수의 분할 영역으로 할당되고, 상기 VM 저장 영역에 저장된 오디오 및 비디오 스트림은 상기 NV 저장 영역에 저장되며, 저장 공간이 모두 이용된 상기 NV 저장 영역에 저장된 오디오 및 비디오 스트림은 상기 메모리 제어부에 의해 상기 하드디스크로 이동 또는 복사되는 것을 특정으로 하는 영상 기록 재생 장치.

【청구항 4】

제3항에 있어서,

상기 메모리 제어부는 상기 NV 저장 영역의 저장 공간이 모두 이용된 경우, 상기 하드디스크로 이동 또는 복사되는 동안 상기 VM 영역들에 저장된 오디오 및 비디오 스트림이 상기 버퍼링 영역에 저장되도록 제어하는 것을 특정으로 하는 영상 기록 재생 장치.

【청구항 5】

제4항에 있어서,

상기 메모리 제어부는 상기 NV 저장 영역에 기록된 오디오 및 비디오 스트림의 이동 또는 복사가 완료되면, 상기 버퍼링 영역의 크기를 상기 NV 저장 영역의 크기만큼 확장하여 확장된 버퍼링 영역을 새로운 NV 저장 영역으로 재지정하고, 축소된 NV 저장 영역을 새로운 버퍼링 영역으로 재지정하는 것을 특정으로 하는 영상 기록 재생 장치.
【청구항 6】

제1항에 있어서,

상기 저장부에 저장되는 스트림 데이터는 PS(Program Stream) 또는 Partial TS(Transport Stream)인 것을 특징으로 하는 영상 기록 재생 장치.

【청구항 7】

영상 기록 재생 장치에 있어서,

취발성 메모리, 비휘발성 메모리 및 하드디스크를 포함하는 저장부; 및

상기 하드디스크에 저장된 스트림 데이터가 취발성 메모리 또는 비휘발성 메모리로 이동 또는 복사되도록 제어하는 메모리 제어부를 포함하되,

복호화부는 상기 취발성 메모리 또는 상기 비휘발성 메모리에 저장된 스트림 데이터를 복호화하여 출력하는 것을 특징으로 하는 영상 기록 재생 장치.

【청구항 8】

제7항에 있어서,

상기 메모리 제어부는 상기 비휘발성 메모리로의 스트림 데이터 이동 또는 복사를 완료할 동안 상기 복호화부에 의해 복호화되어 재생될 수 있는 크기의 스트립 데이터를 상기 취발성 메모리로 이동 또는 복사하는 것을 특징으로 하는 영상
기록 재생 장치.

【청구항 9】

제8항에 있어서,

상기 비회본성 메모리에는 상기 회본성 메모리에 기록된 스트림 데이터에 후속하는 스트림 데이터가 기록되는 것을 특징으로 하는 영상 기록 장치.

【청구항 10】

제8항 또는 제9항에 있어서,

상기 복호화부는 상기 회본성 메모리에 기록된 스트림 데이터의 복호화가 완료되면 연속하여 상기 비회본성 메모리에 저장된 스트림 데이터를 복호화하여 출력하는 것을 특징으로 하는 영상 기록 재생 장치.

【청구항 11】

제7항에 있어서,

상기 스트림 데이터는 PS(Program Stream) 또는 Partial TS(Transport Stream)인 것을 특징으로 하는 영상 기록 재생 장치.
【청구항 12】

영상 기록 재생 장치의 스트림 데이터 저장 방법에 있어서,

(a) 역다중화부로부터 순차적으로 출력되는 오디오 및 비디오 스트림이 미리 지정된 크기의 스트림 데이터로 회발성 메모리에 촉적되면 비회발성 메모리로 이동 저장되도록 하는 단계; 및

(b) 상기 단계 (a)의 반복 수행으로 상기 비회발성 메모리에 미리 지정된 크기의 스트림 데이터가 촉적되거나 상응하는 방송 프로그램의 스트림 데이터 촉적이 완료되면 하드디스크로 이동 저장되도록 하는 단계를 포함하는 영상 기록 재생 장치의 스트림 데이터 저장 방법.

【청구항 13】

제12항에 있어서,

상기 회발성 메모리의 저장 영역이 제1 분할 영역 및 제2 분할 영역으로 할당된 경우 상기 단계 (a)는,

제1 분할 영역에 스트림 데이터의 촉적을 개시하는 단계;

상기 제1 분할 영역의 저장 공간이 모두 이용되면 촉적된 스트림 데이터를 상기 비회발성 메모리로 이동 저장되도록 하고, 후속하는 오디오 및 비디오 스트림에 대한 스트림 데이터가 제2 분할 영역에 촉적되도록 제어하는 단계; 및

상기 제2 분할 영역의 저장 공간이 모두 이용되면 촉적된 스트림 데이터를
상기 비휘발성 메모리로 이동 저장되도록 하고, 후속하는 오디오 및 비디오 스트림에 대한 스트림 데이터가 상기 제1 분할 영역에 축적되도록 제어하는 단계를 포함하는 것을 특징으로 하는 영상 기록 재생 장치의 스트림 데이터 저장 방법.

【청구항 14】

제12항에 있어서,

상기 비휘발성 메모리의 저장 영역이 버퍼링 영역과 NV 저장 영역으로 할당된 경우 상기 단계 (b)는,

상기 NV 저장 영역에 상기 스트림 데이터의 축적을 개시하는 단계; 및

상기 NV 저장 영역의 저장 공간이 모두 이용되면 축적된 스트림 데이터를 상기 하드디스크로 이동 저장되도록 하고, 후속하는 스트림 데이터가 상기 버퍼링 영역에 축적되도록 제어하는 단계를 포함하되,

상기 NV 저장 영역에 축적된 스트림 데이터의 이동이 완료되면, 상기 버퍼링 영역은 상기 NV 저장 영역의 저장 공간만큼 확장되어 새로운 NV 저장 영역으로 재지정되고, 나머지 저장 공간이 새로운 버퍼링 영역으로 재지정되는 것을 특징으로 하는 영상 기록 재생 장치의 스트림 데이터 저장 방법.

【청구항 15】

제14항에 있어서,
상기 버퍼링 영역은 상기 NV 저장 영역에 축적된 스트림 데이터가 상기 하드디스크로 이동 저장하기 위한 시간 동안 후속하는 스트림 데이터를 축적할 수 있는 크기의 저장 공간을 가지는 것을 특징으로 하는 영상 기록 재생 장치의 스트림 데이터 저장 방법.

【청구항 16】

영상 기록 재생 장치의 스트림 데이터 재생 방법에 있어서,

하드디스크에 저장된 스트림 데이터들 중 앞선 재생 순서인 임의의 크기의 스트림 데이터가 회발성 메모리에 저장되도록 하는 단계; 및

상기 회발성 메모리에 저장된 스트림 데이터에 후속하는 스트림 데이터들이 비회발성 메모리에 저장되도록 하는 단계를 포함하여,

상기 회발성 메모리에 저장되는 스트림 데이터의 크기는 최소한 상기 회발성 메모리에 후속하는 스트림 데이터들이 저장되는 시간만큼 재생 처리될 수 있는 크기인 것을 특징으로 하는 영상 기록 재생 장치의 스트림 데이터 재생 방법.

【청구항 17】

제16항에 있어서,

복호화부는 상기 회발성 메모리에 저장된 스트림 데이터의 복호화가 완료되면 상기 비회발성 메모리에 저장된 후속하는 스트림 데이터들을 복호화하도록 제어
되는 것을 특징으로 하는 영상 기록 재생 장치의 스트림 데이터 재생 방법.

【청구항 18】

제16항에 있어서,

상기 스트림 데이터는 PS(Program Stream) 또는 Partial TS(Transport Stream)인 것을 특징으로 하는 영상 기록 재생 장치의 스트림 데이터 재생 방법.

【청구항 19】

스트림 데이터 저장 방법을 수행하기 위해 영상 기록 재생 장치에 의해 실행될 수 있는 명령어들의 프로그램이 유형적으로 구현되어 있으며, 상기 영상 기록 재생 장치에 의해 판독될 수 있는 프로그램을 기록한 기록매체에 있어서,

(a) 역다중화부로부터 순차적으로 출력되는 오디오 및 비디오 스트림이 미리 지정된 크기의 스트림 데이터로 회발성 메모리에 촉적되면 비휘발성 메모리로 이동 저장되도록 하는 단계; 및

(b) 상기 단계 (a)의 반복 수행으로 상기 비휘발성 메모리에 미리 지정된 크기의 스트림 데이터가 촉적되거나 상응하는 방송 프로그램의 스트림 데이터 촉적이 완료되면 하드디스크로 이동 저장되도록 하는 단계를 실행하는 것을 특징으로 하는 프로그램이 기록된 기록매체.

43-37
【청구항 20】

제19항에 있어서,

상기 휘발성 메모리의 저장 영역이 제1 분할 영역 및 제2 분할 영역으로 할당된 경우 상기 단계 (a)는,

제1 분할 영역에 스트림 데이터의 축적을 개시하는 단계;

상기 제1 분할 영역의 저장 공간이 모두 이용되면 축적된 스트림 데이터를 상기 비휘발성 메모리로 이동 저장되도록 하고, 후속하는 오디오 및 비디오 스트림에 대한 스트림 데이터가 제2 분할 영역에 축적되도록 제어하는 단계; 및

상기 제2 분할 영역의 저장 공간이 모두 이용되면 축적된 스트림 데이터를 상기 비휘발성 메모리로 이동 저장되도록 하고, 후속하는 오디오 및 비디오 스트림에 대한 스트림 데이터가 상기 제1 분할 영역에 축적되도록 제어하는 단계를 포함하는 것을 특징으로 하는 프로그램이 기록된 기록매체.

【청구항 21】

제19항에 있어서,

상기 비휘발성 메모리의 저장 영역이 버퍼링 영역과 NV 저장 영역으로 할당된 경우 상기 단계 (b)는,

상기 NV 저장 영역에 상기 스트림 데이터의 축적을 개시하는 단계; 및

상기 NV 저장 영역의 저장 공간이 모두 이용되면 축적된 스트림 데이터를 상
기 하드디스크로 이동 저장되도록 하고, 후속하는 스트림 데이터가 상기 버퍼링 영역에 촉각되도록 제어하는 단계를 포함하되,

상기 NV 저장 영역에 촉각된 스트림 데이터의 이동이 완료되면, 상기 버퍼링 영역은 상기 NV 저장 영역의 저장 공간만큼 확장되어 새로운 NV 저장 영역으로 재지정되고, 나머지 저장 공간이 새로운 버퍼링 영역으로 재지정되는 것을 특징으로 하는 프로그램이 기록된 기록매체.

【청구항 22】

스트림 데이터 재생 방법을 수행하기 위해 영상 기록 재생 장치에 의해 실행될 수 있는 명령어들의 프로그램이 유형적으로 구현되어 있으며, 상기 영상 기록 재생 장치에 의해 판독될 수 있는 프로그램을 기록한 기록매체에 있어서,

하드디스크에 저장된 스트림 데이터들 중 앞선 재생 순서인 임의의 크기의 스트림 데이터가 휘발성 메모리에 저장되도록 하는 단계; 및

상기 휘발성 메모리에 저장된 스트림 데이터에 후속하는 스트림 데이터들이 비휘발성 메모리에 저장되도록 하는 단계를 실행하되,

상기 휘발성 메모리에 저장되는 스트림 데이터의 크기는 최소한 상기 비휘발성 메모리에 후속하는 스트림 데이터들이 저장되는 시간만큼 재생 처리될 수 있는 크기인 것을 특징으로 하는 프로그램이 기록된 기록매체.
【도면】

【도 1】

【도 2】
【도 3】

휘발성 메모리

310 320
제1 VM 영역  제2 VM 영역

비휘발성 메모리

330 340
버퍼링 영역  NV 저장영역

하드디스크

350
HDD 저장 영역
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Tae-Gyu KIM

Serial No.:  New U.S. Patent Application

Filed:  August 8, 2007

For:  DIGITAL VIDEO RECORDER HAVING HIERARCHICAL MEMORIES
AND METHOD FOR IMPLEMENTING HIERARCHICAL MEMORIES

PRELIMINARY AMENDMENT

U.S. Patent and Trademark Office
Customer Service Window, MAIL STOP AMENDMENT
Randolph Building
401 Dulany Street
Alexandria, VA  22314

Sir:

Prior to initial examination on the merits, please amend the above-identified application
as follows:

Amendments to the Claims are reflected in the listing of claims

Remarks/Arguments begin after the listing of the claims.
AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A digital video recorder, comprising:
   
a storage unit, including a volatile memory, a non-volatile memory, and a hard disk drive; and
   
a memory controller, controlling audio and video streams successively outputted from a demultiplexer to be moved to and stored in the volatile memory, the non-volatile memory, and the hard disk drive in the order of the volatile memory, non-volatile memory, and hard disk drive.

2. (Original) The digital video recorder of Claim 1, wherein a storage area of the volatile memory is partitioned into a plurality of VM areas; each VM area successively stores audio and video streams by a designated size; and audio and video streams stored in a VM area, the storage space of which is completely used up, are moved or copied to the non-volatile memory by the memory controller.
3. (Original) The digital video recorder of Claim 2, wherein a storage area of the non-volatile memory is allotted into a plurality of partitioned areas including a buffering area and an NV storage area; audio and video streams stored in the VM area are stored in the NV storage area; and audio and video streams stored in an NV storage area, the storage space of which is completely used up, are moved or copied to the hard disk drive by the memory controller.

4. (Original) The digital video recorder of Claim 3, wherein, if the storage space of the NV storage area is completely used up, the memory controller controls the audio and video streams stored in the VM area to be stored in the buffering area while the audio and video streams are moved or copied to the hard disk drive.

5. (Original) The digital video recorder of Claim 4, wherein, if the moving or copying of the audio and video streams written in the NV storage area is completed, the size of the buffering area is expanded by the size of the NV storage area; the expanded buffering area is re-designated as a new NV storage area; and a reduced NV storage area is re-designated as a new buffering area.

6. (Original) The digital video recorder of Claim 1, wherein stream data stored in the storage unit is a PS (program stream) or a partial TS (transport stream).
7. (Original) A digital video recorder, comprising:

a storage unit, including a volatile memory, a non-volatile memory, and a hard disk drive; and

a memory controller, controlling stream data stored in the hard disk drive to be moved or copied to the volatile memory or the non-volatile memory,

whereas a decoder decodes and outputs stream data stored in the volatile memory or the non-volatile memory.

8. (Original) The digital video recorder of Claim 7, wherein the memory controller moves or copies stream data in the size that can be decoded and played back by the decoder to the volatile memory, while stream data are moved or copied to the non-volatile memory.

9. (Original) The digital video recorder of Claim 8, wherein stream data, following the stream data written in the volatile memory, are written in the non-volatile memory.

10. (Currently Amended) The digital video recorder of Claim 8 or Claim 9, wherein, if decoding the stream data written in the volatile memory is completed, the decoder successively decodes and outputs stream data stored in the non-volatile memory.
11. (Original) The digital video recorder of Claim 7, wherein the stream data is a PS (program stream) or a partial TS (transport stream).

12. (Original) A method for storing stream data of a digital video recorder, comprising:

   (a) moving and storing audio and video streams, which are successively outputted from a demultiplexer, in a non-volatile memory if the audio and video streams are accumulated in a volatile memory as stream data in a predetermined size; and

   (b) if stream data in a predetermined size are accumulated in the non-volatile memory by repeating the above step (a), or accumulation of stream data of a corresponding broadcast program is completed, moving and storing the stream data in a hard disk drive.

13. (Original) The method of Claim 12, wherein, if a storage area of the volatile memory is divided into a first partitioned area and a second partitioned area, the step (a) comprises:

   starting an accumulation of stream data in the first partitioned area;

   if the storage space of the first partitioned area is completely used up, controlling the accumulated stream data to be moved to and stored in the non-volatile memory and controlling stream data for succeeding audio and video streams to be accumulated in the second partitioned area; and
if the storage space of the second partitioned area is completed used up, controlling the accumulated stream data to be moved to and stored in the non-volatile memory and controlling stream data for succeeding audio and video streams to be accumulated in the first partitioned area.

14. (Original) The method of Claim 12, wherein, if a storage area of the non-volatile memory is divided into a buffering area and an NV storage area, the step (b) comprises:

starting an accumulation of the stream data in the NV storage area; and

if the storage space of the NV storage area is completely used up, controlling the accumulated stream data to be moved to and stored in the hard disk drive and controlling succeeding stream data to be accumulated in the buffering area,

whereas, once the moving of the stream data accumulated in the NV storage area is completed, the buffering area is expanded by the storage space of the NV storage area and is re-designated as a new NV storage area, and the remaining storage space is re-designated as a new buffering area.

15. (Original) The method of Claim 14, wherein the buffering area has storage space that is sufficient to accumulate succeeding stream data while the stream data accumulated in the NV storage area are being moved and stored in the hard disk drive.
16. (Original) A method for playing back stream data of a digital video recorder, comprising:

having a certain size of stream data with an earlier playback order stored in a volatile memory, the stream data with an earlier playback order being among stream data stored in a hard disk; and

having stream data following the stream data, which are stored in the volatile memory, stored in a non-volatile memory;

whereas the size of the stream data stored in the volatile memory is large enough to be played back while the succeeding stream data are stored in the non-volatile memory.

17. (Original) The method of Claim 16, wherein a decoder controls the succeeding stream data stored in the non-volatile memory to be decoded, once decoding of the stream data stored in the volatile memory is completed.

18. (Original) The method of Claim 16, wherein the stream data is a PS (program stream) or a partial TS (transport stream).

19. (Original) A recorded medium tangibly embodying a program of instructions executable by a digital video recorder to execute a method for storing stream data, the program being readable by the digital video recorder, the program executing:
(a) moving and storing audio and video streams, which are successively outputted from a demultiplexer, in a non-volatile memory if the audio and video streams are accumulated in a volatile memory as stream data in a predetermined size; and

(b) if stream data in a predetermined size are accumulated in the non-volatile memory by repeating the above step (a), or accumulation of stream data of a corresponding broadcast program is completed, moving and storing the stream data in a hard disk drive.

20. (Original) The recorded medium of Claim 19, wherein, if a storage area of the volatile memory is divided into a first partitioned area and a second partitioned area, the step (a) comprises:

- starting an accumulation of stream data in the first partitioned area;
- if the storage space of the first partitioned area is completely used up, controlling the accumulated stream data to be moved to and stored in the non-volatile memory and controlling stream data for succeeding audio and video streams to be accumulated in the second partitioned area; and
- if the storage space of the second partitioned area is completed used up, controlling the accumulated stream data to be moved to and stored in the non-volatile memory and controlling stream data for succeeding audio and video streams to be accumulated in the first partitioned area.
21. (Original) The recorded medium of Claim 19, wherein, if a storage area of the non-volatile memory is divided into a buffering area and an NV storage area, the step (b) comprises:

starting an accumulation of the stream data in the NV storage area; and

if the storage space of the NV storage area is completely used up, controlling the accumulated stream data to be moved to and stored in the hard disk drive and controlling succeeding stream data to be accumulated in the buffering area,

whereas, once the moving of the stream data accumulated in the NV storage area is completed, the buffering area is expanded by the storage space of the NV storage area and is re-designated as a new NV storage area, and the remaining storage space is re-designated as a new buffering area.

22. (Original) A recorded medium tangibly embodying a program of instructions executable by a digital video recorder to execute a method for playing back stream data, the program being readable by the digital video recorder, the program executing:

having a certain size of stream data with an earlier playback order stored in a volatile memory, the stream data with an earlier playback order being among stream data stored in a hard disk; and

having stream data following the stream data, which are stored in the volatile memory, stored in a non-volatile memory,
whereas the size of the stream data stored in the volatile memory is large enough to be played back while the succeeding stream data are stored in the non-volatile memory.
REMARKS

Claims 1-22 are pending in this application. By this Amendment, claim 10 has been amended to eliminate the multiple dependency. Prompt examination and allowance in due course are respectfully solicited.

CONCLUSION

Should the Examiner have any questions regarding the above-identified application, the Examiner is invited to contact the undersigned attorney, Daniel Y.J. Kim, at the telephone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,
KED & ASSOCIATES, LLP

Daniel Y.J. Kim
Registration No. 36,186

Correspondence Address:
P.O. Box 221200
Chantilly, VA 20153-1200
703 766-3777  DYK/dsk
Date: August 8, 2007
Please direct all correspondence to Customer Number 34610
### Electronic Patent Application Fee Transmittal

**Application Number:**

**Filing Date:**

**Title of Invention:** DIGITAL VIDEO RECORDER HAVING HIERARCHICAL MEMORIES AND METHOD FOR IMPLEMENTING HIERARCHICAL MEMORIES

**First Named Inventor/Applicant Name:** Tae-Gyu KIM

**Filer:** Daniel Y.J. Kim/Deborah Kimberlin

**Attorney Docket Number:** EZ-0001

Filed as Large Entity

### Utility Filing Fees

<table>
<thead>
<tr>
<th>Description</th>
<th>Fee Code</th>
<th>Quantity</th>
<th>Amount</th>
<th>Sub-Total in USD($)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Basic Filing:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Utility application filing</td>
<td>1011</td>
<td>1</td>
<td>300</td>
<td>300</td>
</tr>
<tr>
<td>Utility Search Fee</td>
<td>1111</td>
<td>1</td>
<td>500</td>
<td>500</td>
</tr>
<tr>
<td>Utility Examination Fee</td>
<td>1311</td>
<td>1</td>
<td>200</td>
<td>200</td>
</tr>
<tr>
<td>Pages:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Claims:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Independent claims in excess of 3</td>
<td>1201</td>
<td>3</td>
<td>200</td>
<td>600</td>
</tr>
<tr>
<td>Miscellaneous-Filing:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Petition:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Description</td>
<td>Fee Code</td>
<td>Quantity</td>
<td>Amount</td>
<td>Sub-Total in USD ($)</td>
</tr>
<tr>
<td>-----------------------------------</td>
<td>----------</td>
<td>----------</td>
<td>--------</td>
<td>----------------------</td>
</tr>
<tr>
<td>Patent-Appeals-and-Interference:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Post-Allowance-and-Post-Issuance:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Extension-of-Time:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Miscellaneous:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Total in USD ($)</strong></td>
<td></td>
<td></td>
<td></td>
<td>1600</td>
</tr>
</tbody>
</table>
Electronic Acknowledgement Receipt

<table>
<thead>
<tr>
<th>EFS ID:</th>
<th>2062424</th>
</tr>
</thead>
<tbody>
<tr>
<td>Application Number:</td>
<td>11835816</td>
</tr>
<tr>
<td>International Application Number:</td>
<td></td>
</tr>
<tr>
<td>Confirmation Number:</td>
<td>2115</td>
</tr>
<tr>
<td>Title of Invention:</td>
<td>DIGITAL VIDEO RECORDER HAVING HIERARCHICAL MEMORIES AND METHOD FOR IMPLEMENTING HIERARCHICAL MEMORIES</td>
</tr>
<tr>
<td>First Named Inventor/Applicant Name:</td>
<td>Tae-Gyu KIM</td>
</tr>
<tr>
<td>Customer Number:</td>
<td>34610</td>
</tr>
<tr>
<td>Filer:</td>
<td>Daniel Y.J. Kim/Deborah Kimberlin</td>
</tr>
<tr>
<td>Filer Authorized By:</td>
<td>Daniel Y.J. Kim</td>
</tr>
<tr>
<td>Attorney Docket Number:</td>
<td>EZ-0001</td>
</tr>
<tr>
<td>Receipt Date:</td>
<td>08-AUG-2007</td>
</tr>
<tr>
<td>Filing Date:</td>
<td></td>
</tr>
<tr>
<td>Time Stamp:</td>
<td>16:34:58</td>
</tr>
<tr>
<td>Application Type:</td>
<td>Utility under 35 USC 111(a)</td>
</tr>
</tbody>
</table>

Payment information:

- Submitted with Payment: yes
- Payment was successfully received in RAM: $1600
- RAM confirmation Number: 8119
- Deposit Account:  

File Listing:

<table>
<thead>
<tr>
<th>Document Number</th>
<th>Document Description</th>
<th>File Name</th>
<th>File Size(Bytes)</th>
<th>Multi Part / .zip</th>
<th>Pages (if appl.)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Multipart Description/PDF files in .zip description</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>--------------------------------------------------</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Document Description</td>
<td>Start</td>
<td>End</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Specification</td>
<td>1</td>
<td>25</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Claims</td>
<td>26</td>
<td>33</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Abstract</td>
<td>34</td>
<td>34</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Drawings</td>
<td>35</td>
<td>39</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Oath or Declaration filed</td>
<td>40</td>
<td>41</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transmittal of New Application</td>
<td>42</td>
<td>42</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Authorization for Extension of Time all replies</td>
<td>43</td>
<td>43</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Preliminary Amendment</td>
<td>44</td>
<td>54</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Warnings:**

**Information:**

| 2 | Fee Worksheet (PTO-06) | fee-info.pdf | 8529 | no | 2 |

**Warnings:**

**Information:**

Total Files Size (in bytes): 2454966
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements, a Form PCT/DO/E0/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.
DIGITAL VIDEO RECORDER HAVING HIERARCHICAL MEMORIES AND METHOD
FOR IMPLEMENTING HIERARCHICAL MEMORIES

CROSS-REFERENCE TO RELATED PATENT APPLICATIONS

This application claims the benefit of Korean Patent Application No. 10-2006-0075348, filed on August 9, 2006, in the Korean Intellectual Property Office, the disclosure of which is incorporated herein in its entirety by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a digital video recorder. More specifically, the present invention relates to a digital video recorder having hierarchical memories for efficient video recording and playing back and a method for implementing hierarchical memories.

Description of the Related Technology

Started in the computer industry, digitalization of information has already reached its application in the telecommunications industry. Today, television broadcast signals are even digitalized. It is certain that the digitalization of television broadcast signals will open a new paradigm of two-way multimedia experience that is integrated with computer and telecommunications technologies.
Digital broadcasting is progressing around the European standard of DVD (Digital Video Broadcasting) and the American FCC standard of ATV (Advanced TV), which is in compliance with the ATSC standard, which the U.S. adopted as the next-generation TV standard to replace the conventional analog standard of NTSC.

Unlike the conventional storage of analog signals in a cassette tape, a PVR (Personal Video Recorder) receives signals, transmitted from a broadcast station or outputted from a television, converts the signals to digital information in real time, compresses the digital data into an MPEG2 file, and stores the data in a pre-installed hard disk (HD). The PVR then reads the stored data and outputs images, which are decoded in real time, to a display device.

FIG. 1 is a block diagram showing the structure of a conventional PVR system.

Referring to FIG. 1, the PVR system includes an IR receiver 110, a processor 120, a memory 130, a tuner 140, a demultiplexer 150, a decoder 160, an output unit 170, an OSD unit 180, an IDE interface 185, and a hard disk drive 190.

The IR receiver 110 receives remote control code information corresponding to a remote control operated by a user and transmits the remote control code information to the processor 120.

The processor 120 translates a remote control code received from the IR receiver 110 and transmits remote control code translation information to a corresponding device. For example, if the remote control code translation information is a command to request a channel change, the processor 120 transmits the command to the tuner 140. Likewise, if the remote
control code translation information is a command to record a program, the received broadcast
data is controlled to be stored in the hard disk drive 190. If the remote control code translation
information is a command to request a recording list, the recording list stored in the hard disk
drive 190 is outputted through the output unit 170.

The memory 130 can include a flash ROM, in which software for the operation of the
PVR system is stored, and a DRAM, which stores a bitmap-type virtual screen that can be
displayed through the output unit 170.

The tuner 140 receives and outputs the broadcast signals, which are selected by the
control of the processor 120.

The demultiplexer 150 parses various kinds of information, such as audio, video, and
other data, which are multiplexed in the broadcast signals supplied from the tuner 140.

The decoder 160 decodes audio signals, video signals, and data signals, parsed by the
demultiplexer 150, and processes these signals to visual and audio information that can be
outputted through the output unit 170 such that the user can recognize these signals.

The OSD unit 180 displays information corresponding to a particular command given
by the processor 120. For instance, if a recording list output command is received from the
processor 120, the OSD unit 180 controls the recording list extracted from the hard disk drive
190 to be displayed through the output unit 170.

The IDE interface 185 receives transport packet (TP) data, transmitted from the
demultiplexer 150 for recording, and provides the TD data to the hard disk drive 190. If a
playback command is received from the processor 120, the IDE interface 185 transmits the data stored in the hard disk drive 190 to the decoder 160 through the processor 120.

The hard disk drive 190 stores the TP data, transmitted from the IDE interface 185, that is, programs selected by the user through the recording command are stored in the hard disk drive 190.

It is natural that multimedia data usually have a large amount of data flow. Digital recording devices, such as the PVR, are equipped with a large capacity hard disk drive to store this large amount of data flow.

While the hard disk drive is capable of storing a large amount of data at a low cost, the hard disk drive also has its own shortcomings over the flash memories, namely, slow access speeds, slow operation speeds, low durability, and short life. The durability and life of a hard disk drive can be an important factor that determines the durability and life of a digital recording device.

As an attempt to address the above problems, the conventional digital recording device with a hard disk drive switches the hard disk drive to a stand-by mode or utilizes a large-capacity memory while the recording feature is not used. However, since most features of the digital recording device, for example, time-shift recording that can pause a live program, are based on the operation of the hard disk drive, the duration of maintaining the hard disk drive in a stand-by mode is very limited. Equipping the digital recording device with a large-capacity memory costs
a lot more than the hard disk drive. Being inevitably a machine device, the hard disk drive generates a great deal of noise and heat, which can be inappropriate for an appliance.

SUMMARY OF CERTAIN INVENTIVE ASPECTS

One aspect of the present invention provides a digital video recorder having hierarchical memories and a method for implementing the hierarchical memories that can minimize the use of a hard disk drive by hierarchically utilizing storage means in accordance with characteristics of data.

Another aspect of the present invention provides a digital video recorder having hierarchical memories and a method for implementing the hierarchical memories that can use data at a higher speed and minimize the use of a hard disk drive by placing a memory in between the hard disk drive, processor, and decoder to have the data stored and played back.

Another aspect of the present invention features a digital video recorder.

The digital video recorder in accordance with an embodiment of the present invention has a storage unit, which includes a volatile memory, a non-volatile memory, and a hard disk drive, and a memory controller, which controls audio and video streams successively outputted from a demultiplexer to be moved to and stored in the volatile memory, the non-volatile memory, and the hard disk drive in the order of the volatile memory, non-volatile memory, and hard disk drive.
A storage area of the volatile memory can be partitioned into a plurality of VM areas; each VM area can successively store audio and video streams by a designated size; and audio and video streams stored in a VM area, the storage space of which is completely used up, can be moved or copied to the non-volatile memory by the memory controller.

A storage area of the non-volatile memory can be allotted into a plurality of partitioned areas including a buffering area and an NV storage area; audio and video streams stored in the VM area can be stored in the NV storage area; and audio and video streams stored in an NV storage area, the storage space of which is completely used up, can be moved or copied to the hard disk drive by the memory controller.

If the storage space of the NV storage area is completely used up, the memory controller can control the audio and video streams stored in the VM area to be stored in the buffering area while the audio and video streams are moved or copied to the hard disk drive.

If the moving or copying of the audio and video streams written in the NV storage area is completed, the size of the buffering area can be expanded by the size of the NV storage area; the expanded buffering area can be re-designated as a new NV storage area; and a reduced NV storage area can be re-designated as a new buffering area.

The stream data stored in the storage unit can be a PS (program stream) or a partial TS (transport stream).

The digital video recorder in accordance with another embodiment of the present invention can include a storage unit, which includes a volatile memory, a non-volatile memory,
and a hard disk drive, and a memory controller, which controls stream data stored in the hard
disk drive to be moved or copied to the volatile memory or the non-volatile memory. A decoder
can decode and output stream data stored in the volatile memory or the non-volatile memory.

The memory controller can move or copy stream data in the size that can be decoded
and played back by the decoder to the volatile memory, while stream data are moved or copied to
the non-volatile memory.

Stream data, following the stream data written in the volatile memory, can be written in
the non-volatile memory.

If decoding the stream data written in the volatile memory is completed, the decoder can
successively decode and output stream data stored in the non-volatile memory.

The stream data can be a PS (program stream) or a partial TS (transport stream).

Another aspect of the present invention features a method for storing and/or playing
back stream data of a digital video recorder.

The method for storing stream data of a digital video recorder in accordance with an
embodiment of the present invention can include (a) moving and storing audio and video streams,
which are successively outputted from a demultiplexer, in a non-volatile memory if the audio
and video streams are accumulated in a volatile memory as stream data in a predetermined size
and (b) if stream data in a predetermined size are accumulated in the non-volatile memory by
repeating the above step (a), or accumulation of stream data of a corresponding broadcast
program is completed, moving and storing the stream data in a hard disk drive.
If a storage area of the volatile memory is divided into a first partitioned area and a second partitioned area, the step (a) can include i) starting an accumulation of stream data in the first partitioned area, ii) if the storage space of the first partitioned area is completely used up, controlling the accumulated stream data to be moved to and stored in the non-volatile memory and controlling stream data for succeeding audio and video streams to be accumulated in the second partitioned area, and iii) if the storage space of the second partitioned area is completely used up, controlling the accumulated stream data to be moved to and stored in the non-volatile memory and controlling stream data for succeeding audio and video streams to be accumulated in the first partitioned area.

If a storage area of the non-volatile memory is divided into a buffering area and an NV storage area, the step (b) can include i) starting an accumulation of the stream data in the NV storage area, and ii) if the storage space of the NV storage area is completely used up, controlling the accumulated stream data to be moved to and stored in the hard disk drive and controlling succeeding stream data to be accumulated in the buffering area. Once the moving of the stream data accumulated in the NV storage area is completed, the buffering area can be expanded by the storage space of the NV storage area and be re-designated as a new NV storage area, and the remaining storage space can be re-designated as a new buffering area.

The buffering area can have storage space that is sufficient to accumulate succeeding stream data while the stream data accumulated in the NV storage area are being moved and stored in the hard disk drive.
The method for playing back stream data of a digital video recorder in accordance with another embodiment of the present invention can include i) having a certain size of stream data with an earlier playback order stored in a volatile memory, the stream data with an earlier playback order being among stream data stored in a hard disk, and ii) having stream data following the stream data, which are stored in the volatile memory, stored in a non-volatile memory. The size of the stream data stored in the volatile memory can be large enough to be played back while the succeeding stream data are stored in the non-volatile memory.

A decoder can control the succeeding stream data stored in the non-volatile memory to be decoded, once decoding of the stream data stored in the volatile memory is completed.

The stream data can be a PS (program stream) or a partial TS (transport stream).

Still another aspect of the present invention features a recorded medium recording a method for storing and/or playing back stream data of a digital video recorder.

According to an embodiment of the present invention, the recorded medium tangibly embodies a program of instructions executable by a digital video recorder to execute a method for storing stream data. The program, which is readable by the digital video recorder, can execute (a) moving and storing audio and video streams, which are successively outputted from a demultiplexer, in a non-volatile memory if the audio and video streams are accumulated in a volatile memory as stream data in a predetermined size, and (b) if stream data in a predetermined size are accumulated in the non-volatile memory by repeating the above step (a), or
accumulation of stream data of a corresponding broadcast program is completed, moving and storing the stream data in a hard disk drive.

If a storage area of the volatile memory is divided into a first partitioned area and a second partitioned area, the step (a) can include i) starting an accumulation of stream data in the first partitioned area, ii) if the storage space of the first partitioned area is completely used up, controlling the accumulated stream data to be moved to and stored in the non-volatile memory and controlling stream data for succeeding audio and video streams to be accumulated in the second partitioned area, and iii) if the storage space of the second partitioned area is completed used up, controlling the accumulated stream data to be moved to and stored in the non-volatile memory and controlling stream data for succeeding audio and video streams to be accumulated in the first partitioned area.

If a storage area of the non-volatile memory is divided into a buffering area and an NV storage area, the step (b) can include i) starting an accumulation of the stream data in the NV storage area, and ii) if the storage space of the NV storage area is completely used up, controlling the accumulated stream data to be moved to and stored in the hard disk drive and controlling succeeding stream data to be accumulated in the buffering area. Once the moving of the stream data accumulated in the NV storage area is completed, the buffering area can be expanded by the storage space of the NV storage area and can be re-designated as a new NV storage area, and the remaining storage space can be re-designated as a new buffering area.
According to another embodiment of the present invention, the recorded medium tangibly embodies a program of instructions executable by a digital video recorder to execute a method for playing back stream data. The program, which is readable by the digital video recorder, can execute i) having a certain size of stream data with an earlier playback order stored in a volatile memory, the stream data with an earlier playback order being among stream data stored in a hard disk, and ii) having stream data following the stream data, which are stored in the volatile memory, stored in a non-volatile memory. The size of the stream data stored in the volatile memory can be large enough to be played back while the succeeding stream data are stored in the non-volatile memory.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a block diagram of conventional PVR system.

FIG. 2 shows a block diagram of a digital video recorder in accordance with an embodiment of the present invention.

FIG. 3 illustrates a hierarchical memory structure in accordance with an embodiment of the present invention.

FIG. 4 shows a flow chart of a method for hierarchically operating storage means when writing data in accordance with an embodiment of the present invention.

FIG. 5 shows a flow chart of a method for hierarchically operating storage means when playing back data in accordance with an embodiment of the present invention.
DESCRIPTION OF CERTAIN INVENTIVE EMBODIMENTS

Since there can be a variety of permutations and embodiments of the present invention, certain embodiments will be illustrated and described with reference to the accompanying drawings. This, however, is by no means to restrict the present invention to certain embodiments, and shall be construed as including all permutations, equivalents and substitutes covered by the spirit and scope of the present invention. Throughout the drawings, similar elements are given similar reference numerals. Throughout the description of the present invention, when describing a certain technology is determined to evade the point of the present invention, the pertinent detailed description will be omitted.

Terms such as “first” and “second” can be used in describing various elements, but the above elements shall not be restricted to the above terms. The above terms are used only to distinguish one element from the other. For instance, the first element can be named the second element, and vice versa, without departing the scope of claims of the present invention. The term “and/or” shall include the combination of a plurality of listed items or any of the plurality of listed items.

When one element is described as being “connected” or “accessed” to another element, it shall be construed as being connected or accessed to the other element directly but also as possibly having another element in between. On the other hand, if one element is described as
being “directly connected” or “directly accessed” to another element, it shall be construed that there is no other element in between.

The terms used in the description are intended to describe certain embodiments only, and shall by no means restrict the present invention. Unless clearly used otherwise, expressions in the singular number include a plural meaning. In the present description, an expression such as “comprising” or “consisting of” is intended to designate a characteristic, a number, a step, an operation, an element, a part or combinations thereof, and shall not be construed to preclude any presence or possibility of one or more other characteristics, numbers, steps, operations, elements, parts or combinations thereof.

Unless otherwise defined, all terms, including technical terms and scientific terms, used herein have the same meaning as how they are generally understood by those of ordinary skill in the art to which the invention pertains. Any term that is defined in a general dictionary shall be construed to have the same meaning in the context of the relevant art, and, unless otherwise defined explicitly, shall not be interpreted to have an idealistic or excessively formalistic meaning.

Hereinafter, some embodiments will be described in detail with reference to the accompanying drawings. Identical or corresponding elements will be given the same reference numerals, regardless of the figure number, and any redundant description of the identical or corresponding elements will not be repeated.
FIG. 2 is a block diagram showing a digital video recorder in accordance with an
embodiment of the present invention, and FIG. 3 is illustration of a hierarchical memory
structure in accordance with an embodiment of the present invention.

Referring to FIG. 2, the digital video recorder in accordance with an embodiment of the
present invention includes a tuner 210, a demultiplexer 220, a decoder 230, an output unit 240, a
memory controller 250, and a storage unit 260. The storage unit 260 can include a volatile
memory 270, a non-volatile memory, and a hard disk drive 290.

The tuner 210 receives and outputs a broadcast signal, selected by the control of a
playback processor (not shown). The playback processor can be a main processor that controls
the operation of the digital video recorder.

The demultiplexer 220 demultiplexes various kinds of information, such as audio, video,
and other data that are multiplexed in broadcast signals supplied by the tuner 210. The
demultiplexer 220 also demultiplexes a broadcast program, selected in accordance with the
user’s selection input, among broadcast signals received through the tuner and extracts the
selected broadcast program to video and audio streams. The broadcast signal extracted and
outputted by the demultiplexer 220 can be an MPEG data format, for example, program stream
(PS) and/or partial transport stream (TS).

The decoder 230 decodes the audio and video streams, parsed by the demultiplexer 220,
and processes the decoded audio and video streams to visual information and audio information
that can be outputted through the output unit 240 such that the user can recognize the
information.

The output unit 240 outputs the decoded audio and video signals, outputted from the
decoder 230, to video and/or audio information. The output unit 240 can include a display and/or
a speaker.

The memory controller 250 designates the storage means to which the video and audio
streams outputted from the demultiplexer 220 are to be stored and has the pertinent video and
audio streams stored in accordance with the hierarchical structure of a plurality of storage means.
The memory controller 250 also controls the stored data to be read and to be outputted through
the output unit 240 in accordance with the hierarchical structure of the storage means.

The storage unit 260 includes a volatile memory 270, non-volatile memory 280, and a
hard disk drive 290. The video and audio streams that are stored in the storage means can be a
form of PS and/or partial TS.

Although freely readable and writeable and fast to operate, the volatile memory 270
loses the stored data once the power is cut off. The volatile memory 270 can be a RAM, for
example. As illustrated in FIG. 3, the volatile memory 270 can be logically partitioned into a
plurality of areas. For example, the volatile memory can be partitioned into a first VM (volatile
memory) area 310 and a second VM area 320, if the volatile memory 270 is divided into 2 areas.

The non-volatile memory 270 is slower than the memory although it is possible to
read/write in block units. The non-volatile memory 270 can be, for example, a flash memory. As
shown in FIG. 3, the non-volatile memory 270 can be logically partitioned into a plurality of areas. For example, the non-volatile memory can be partitioned into a buffering area 330 and an NV (non-volatile) storage area 340.

Although the hard disk drive 290 can store and maintain a large capacity of data, it is slow and noisy.

The present invention maximizes the positive features and minimizes the negative features of the storage means to apply the hierarchical structure between the storage means. In other words, the memory controller 250 controls each of the storage means in the storage unit 260 as a hierarchical structure (i.e., data flow) of the volatile memory 270—non-volatile memory 280—hard disk drive 290, if the video and audio streams outputted from the demultiplexer 220 are stored in the storage means. On the other hand, the memory controller 250 controls the storage means as a hierarchical structure of the hard disk drive 290—non-volatile memory 280—volatile memory 270 or a hierarchical structure of the hard disk drive 290—volatile memory 270—non-volatile memory 280 if the data stored in each of the storage means are played back.

FIGS. 3 to 5 will be referenced below to describe how the storage means of the digital video recorder are operated hierarchically in accordance with the present invention.

FIG. 4 is a flow chart showing how the storage means are operated hierarchically, when data is written, in accordance with an embodiment of the present invention.
Referring to FIG. 4, in a step represented by 410, the memory controller 250 stores the audio and video streams, outputted from the demultiplexer 220 in accordance with the user's command to store broadcast data, in the first VM area 310 of the volatile memory 270.

In step 415, the memory controller determines whether the storage space of the first VM area 310 is used up while storing the audio and video streams, successively outputted from the demultiplexer 220, in the first VM area 310 of the volatile memory 270.

If there still is storage space in the first VM area 310, step 410 is repeated to continuously store the audio and video streams, outputted from the demultiplexer 220, in the first VM area 310 of the volatile memory 270.

If the storage space of the first VM area 310 is used up, however, step 420 is performed to have the memory controller 250 store following audio and video streams in the second VM area 320. The memory controller 250 also controls the data stored in the first VM area 310 to be written in the NV storage area 340 of the non-volatile memory 270, in steps represented by 420 and 435.

As described above, the storage space of the volatile memory 270 is divided into two or more partitioned areas, and if the audio and video streams fill up the storage space of one of the partitioned areas, succeeding audio and video streams will continue to be stored in another partitioned area. While the audio and video streams are stored in another partitioned area, the data written in the partitioned area, in which the preceding audio and video streams are stored, are stored in the NV storage area 340 of the non-volatile memory 270, and once the storing is
completed, the data written in the pertinent partitioned area is deleted. For example, if the volatile memory consists of and sequentially use the first VM area 310 and the second VM area 320, as shown in FIG. 3, the data written in the first VM area 310 is written in the NV storage area 340 of the non-volatile memory 280 while the audio and video streams are stored in the second VM area 320. However, all of the data written in the first VM area 310 will have to move to or be copied to the NV storage area 340 of the non-volatile memory 280 before completing the writing of the audio and video streams in the second VM area 320. If the writing of the audio and video streams is completed before the storage space of the first VM area 310 is used up, the second VM area 320 will no longer be used, and the audio and video streams written in the first VM area 310 will move to or be copied to the NV storage area 340 by the control of the memory controller 250.

In step 425, the memory controller 250 determines whether the storage space of the second VM area 320 is used up while storing the audio and video streams, successively outputted from the demultiplexer 220, in the second VM area 320 of the volatile memory 270.

If there is remaining storage space in the second VM area 320, step 420 is repeated to have the audio and video streams, outputted from the demultiplexer 220, stored continuously in the second VM area 320 of the volatile memory 270. In this case, especially if the writing of the audio and video streams is completed before the storage space of the second VM area 320 is used up, the first VM area 310 will no longer be used for writing the corresponding audio and
video streams, and the audio and video streams written in the second VM area 320 will move to
or be copied to the NV storage area 340 by the control of the memory controller 250.

However, if the storage area of the second VM area 320 is used up, the memory
controller 250 controls, in step 430, the succeeding audio and video streams to be stored in the
first VM area 310. The memory controller 250 also controls the data written in the second VM
area 320 to be written in the NV storage area 340 of the non-volatile memory 280, in steps 430
and 435.

In step 435, the memory controller 250 controls the audio and video streams, written in
the first VM area 310 or the second VM area 320, to be stored in the NV storage area 340. Here,
it is preferable that the size of the NV storage area 340 corresponds to a capacity that can record
an episode of a typical broadcast program. The recording capacity of a typical broadcast program
may vary depending on the digital broadcast, but an approximate amount of 3.5G bytes is
required for a 2-hour program since the DVB SD level has a bit rate of about 4Mbps. The size of
the NV storage area 340 can be adjusted or preconfigured according to the bit rate of the
broadcasting environment.

In step 440, the memory controller 250 determines whether the storage space of the NV
storage area 340 is used up.

If there remains storage space in the NV storage area 340, step 435 is repeated to have
the memory controller 250 control the audio and video streams, received from the first VM area
310 or the second VM area 320, to be continuously stored in the storage space of the NV storage area 340.

If, however, the storage space of the NV storage area 340 is used up, step 445 is performed to have the memory controller 250 control the succeeding audio and video streams to be stored in the buffering area 330. The memory controller also controls the data written in the NV storage area 340 to be stored in a HDD storage area 350 of the hard disk drive 290, in steps 445 and 460.

In step 450, the memory controller 250 determines whether all of the audio and video streams written in the NV storage area 340 are moved to or copied to the hard disk drive 290.

If all of the pertinent audio and video streams are not moved to or copied to the hard disk drive, the step 445 is repeated. If, however, all of the pertinent audio and video streams are moved to or copied to the hard disk drive, step 455 is performed to expand the buffering area 330 (i.e., the partitioned storage area of the non-volatile memory 280 to which the audio and video streams are presently moved from the volatile memory 270) to re-designate it as the NV storage area 340 and re-designates the remaining area as the buffering area 330. In this case, the size of the buffering area 330 and NV storage area 340 can be maintained constant by expanding the buffering area 330 by the originally-designated size of the NV storage area 340 and re-designating the expanded buffering area 330 as the NV storage area 340. Moreover, it is preferable that the original size of the buffering area 330 be at least large enough to store the audio and video stream, which are moved to or copied from the volatile memory 270, while all
of the audio and video streams stored in the NV storage area 340 are moved or copied to the hard
disk drive 290.

As described above, the non-volatile memory 280 is logically partitioned into 2 or more
storage areas in accordance with the present invention. Therefore, in case the storage space of
any one partitioned area is used up, succeeding data can be written in another partitioned area
while the data written in the used-up partitioned area are being moved or copied to the hard disk
drive 290, thereby guaranteeing the data-sequencing.

As described above, however, if the NV storage area 340 is configured to have a storage
capacity that can store all of the audio and video streams corresponding to one broadcast
program, the storing of the succeeding audio and video streams in the buffering area 330 will not
be performed. Moreover, if the storing of the audio and video streams according to the user’s
command to store a broadcast program is completed, the pertinent audio and video streams will
be moved or copied to the hard disk drive 290. It is possible to determine whether all of the audio
and video streams of a broadcast program corresponding to the user’s storage command are
stored, by using an assigned identifier or broadcast time corresponding to each broadcast
program. Since the method of the above determination is well known to anyone skilled in the art,
the pertinent description will not be provided herein.

Below, the procedure for playing back the data, written in the hard disk, through the
hierarchical operation of the storage means, as described above for writing the data, will be
described with reference to FIG. 5.
FIG. 5 is a flow chart showing a method for hierarchically operating storage means when playing back data in accordance with an embodiment of the present invention.

Referring to FIG. 5, in step 510, the memory controller 250 controls the audio and video streams stored in the hard disk drive 290 to have audio and video streams of a certain size moved or copied (collectively referred to as “copied”, hereinafter) to the volatile memory (i.e., the first VM area 310 or the second VM area 320). The subject of copying the pertinent audio and video streams can be the memory controller 250. The playback controller or the memory controller 250 also controls the decoder 230 to decode the audio and video data stored in the volatile memory 270 and output the decoded audio and video data through the output unit 240. The minimum size of the audio and video streams copied to the volatile memory 270 should be sufficient for playing back until audio and video streams to be played back successively are completely copied from the hard disk drive 290 to the NV storage area 340 of the non-volatile memory. The memory controller 250 writes audio and video streams, which will be initially played back, in the volatile memory 270 because the data written in the volatile memory 270 can be processed more quickly. It shall be also evident that the audio and video streams to be played back initially can be copied to the buffering area 330 to have succeeding audio and video streams copied to the NV storage area 340 during the playback.

In step 520, the memory controller 250 copies audio and video streams, which succeed the audio and video stream copied to the volatile memory 270 through the above step 510, from
the hard disk drive 290 to the NV storage area 340. Once the playing back using the data stored in the volatile memory 270 is completed, the playback controller or the memory controller 250 controls the decoder 230 to decode the audio and video streams written in the NV storage area 340 of the non-volatile memory 280 and output the decoded audio and video data through the output unit 240.

In step 530, the memory controller 250 determines whether there remain audio and video streams to be successively played back in accordance with the broadcast program, which is presently played back, in the hard disk drive 290. The step 530 can be performed any time while playing back the audio and video streams that are copied to the NV storage area 340. However, since there can be audio and video streams to be successively played back, it would be preferable that the step 530 be performed prior to the time required to have some or all of the pertinent data copied in the volatile memory 270 or the buffering area 330.

This can be determined by using the time required for the memory controller 250 or a digital video recorder to copy data written in particular storage means to other storage means (which can be calculated using the bit rate and the amount of data to transfer) and the time required for playing back using the data written in particular storage means (which can be calculated using the bit rate and the amount of data to play back).

The step 530 and following steps can be omitted if the size of the storage space of the NV storage area 340 is configured to a capacity that can store one broadcast program or if audio and video streams to be successively played back are not present in the hard disk drive 290.
If, however, the audio and video streams to be successively played back are present in the hard disk drive 290, the memory controller 250 controls, in step 540, the audio and video streams of a certain size, which follow the audio and video streams stored in the hard disk drive 290 that are copied to the NV storage area 340, to be copied to the volatile memory 270. The audio and video streams copied through the step 540 will be used for playback after the audio and video streams copied to the NV storage area 340 through the step 520 are completely played back. As described above, the pertinent audio and video streams can be copied to the buffering area 330. The step 540 is performed for the same reason as the step 510.

In step 550, the memory controller 250 controls audio and video streams that follow the audio and video streams written in the volatile memory 270 in the step 540 to be copied to the NV storage area 340 of the non-volatile memory 280. The step 550 can be omitted if the audio and video streams written in the volatile memory 270 or the buffering area 330 through the step 540 are the final audio and video streams for the corresponding broadcast program.

As described above, the digital video recorder of the present invention copies a certain amount of data, for the audio and video streams written in the hard disk drive 290, to the volatile memory 270 or the non-volatile memory 280 and plays back the audio and video streams by using the copied data, rather than playing back the data from the hard disk drive 290, when playing back the audio and video streams written in the hard disk drive 290.

Therefore, by operating the storage means hierarchically, the digital video recorder in accordance with the present invention can minimize the time required for storing the data and the
stand-by time required for playing back the data, when writing the data in the storage unit 260 or
performing the playback by using the data written in the storage unit 260. Furthermore, by
allowing the hard disk drive 290 to be used only when all of the data stored in the non-volatile
memory 280 are transferred to the hard disk drive 290 during the storing of the data or when all
of the data stored in the hard disk drive 290 are transferred to the volatile memory 270 or the
non-volatile memory 280 during the playback of the data., the use of the hard disk drive 290 can
be minimized over the conventional data storage and playback methods.

Although certain embodiments of the present invention have been described, anyone of
ordinary skill in the art to which the invention pertains should be able to understand that a very
large number of permutations are possible without departing the spirit and scope of the present
invention, which shall only be defined by the claims appended below.
WHAT IS CLAIMED IS:

1. A digital video recorder, comprising:

   a storage unit, including a volatile memory, a non-volatile memory, and a hard disk

   drive; and

   a memory controller, controlling audio and video streams successively outputted from a
demultiplexer to be moved to and stored in the volatile memory, the non-volatile memory, and
the hard disk drive in the order of the volatile memory, non-volatile memory, and hard disk
drive.

2. The digital video recorder of Claim 1, wherein a storage area of the volatile memory
is partitioned into a plurality of VM areas; each VM area successively stores audio and video
streams by a designated size; and audio and video streams stored in a VM area, the storage space
of which is completely used up, are moved or copied to the non-volatile memory by the memory
controller.

3. The digital video recorder of Claim 2, wherein a storage area of the non-volatile
memory is allotted into a plurality of partitioned areas including a buffering area and an NV
storage area; audio and video streams stored in the VM area are stored in the NV storage area;
and audio and video streams stored in an NV storage area, the storage space of which is completely used up, are moved or copied to the hard disk drive by the memory controller.

4. The digital video recorder of Claim 3, wherein, if the storage space of the NV storage area is completely used up, the memory controller controls the audio and video streams stored in the VM area to be stored in the buffering area while the audio and video streams are moved or copied to the hard disk drive.

5. The digital video recorder of Claim 4, wherein, if the moving or copying of the audio and video streams written in the NV storage area is completed, the size of the buffering area is expanded by the size of the NV storage area; the expanded buffering area is re-designated as a new NV storage area; and a reduced NV storage area is re-designated as a new buffering area.

6. The digital video recorder of Claim 1, wherein stream data stored in the storage unit is a PS (program stream) or a partial TS (transport stream).

7. A digital video recorder, comprising:

a storage unit, including a volatile memory, a non-volatile memory, and a hard disk drive; and
a memory controller, controlling stream data stored in the hard disk drive to be moved or copied to the volatile memory or the non-volatile memory,

whereas a decoder decodes and outputs stream data stored in the volatile memory or the non-volatile memory.

8. The digital video recorder of Claim 7, wherein the memory controller moves or copies stream data in the size that can be decoded and played back by the decoder to the volatile memory, while stream data are moved or copied to the non-volatile memory.

9. The digital video recorder of Claim 8, wherein stream data, following the stream data written in the volatile memory, are written in the non-volatile memory.

10. The digital video recorder of Claim 8 or Claim 9, wherein, if decoding the stream data written in the volatile memory is completed, the decoder successively decodes and outputs stream data stored in the non-volatile memory.

11. The digital video recorder of Claim 7, wherein the stream data is a PS (program stream) or a partial TS (transport stream).

12. A method for storing stream data of a digital video recorder, comprising:
(a) moving and storing audio and video streams, which are successively outputted from a demultiplexer, in a non-volatile memory if the audio and video streams are accumulated in a volatile memory as stream data in a predetermined size; and

(b) if stream data in a predetermined size are accumulated in the non-volatile memory by repeating the above step (a), or accumulation of stream data of a corresponding broadcast program is completed, moving and storing the stream data in a hard disk drive.

13. The method of Claim 12, wherein, if a storage area of the volatile memory is divided into a first partitioned area and a second partitioned area, the step (a) comprises:

starting an accumulation of stream data in the first partitioned area;

if the storage space of the first partitioned area is completely used up, controlling the accumulated stream data to be moved to and stored in the non-volatile memory and controlling stream data for succeeding audio and video streams to be accumulated in the second partitioned area; and

if the storage space of the second partitioned area is completely used up, controlling the accumulated stream data to be moved to and stored in the non-volatile memory and controlling stream data for succeeding audio and video streams to be accumulated in the first partitioned area.
14. The method of Claim 12, wherein, if a storage area of the non-volatile memory is divided into a buffering area and an NV storage area, the step (b) comprises:

starting an accumulation of the stream data in the NV storage area; and

if the storage space of the NV storage area is completely used up, controlling the accumulated stream data to be moved to and stored in the hard disk drive and controlling succeeding stream data to be accumulated in the buffering area,

whereas, once the moving of the stream data accumulated in the NV storage area is completed, the buffering area is expanded by the storage space of the NV storage area and is re-designated as a new NV storage area, and the remaining storage space is re-designated as a new buffering area.

15. The method of Claim 14, wherein the buffering area has storage space that is sufficient to accumulate succeeding stream data while the stream data accumulated in the NV storage area are being moved and stored in the hard disk drive.

16. A method for playing back stream data of a digital video recorder, comprising:

having a certain size of stream data with an earlier playback order stored in a volatile memory, the stream data with an earlier playback order being among stream data stored in a hard disk; and
having stream data following the stream data, which are stored in the volatile memory, stored in a non-volatile memory;

whereas the size of the stream data stored in the volatile memory is large enough to be played back while the succeeding stream data are stored in the non-volatile memory.

17. The method of Claim 16, wherein a decoder controls the succeeding stream data stored in the non-volatile memory to be decoded, once decoding of the stream data stored in the volatile memory is completed.

18. The method of Claim 16, wherein the stream data is a PS (program stream) or a partial TS (transport stream).

19. A recorded medium tangibly embodying a program of instructions executable by a digital video recorder to execute a method for storing stream data, the program being readable by the digital video recorder, the program executing:

(a) moving and storing audio and video streams, which are successively outputted from a demultiplexer, in a non-volatile memory if the audio and video streams are accumulated in a volatile memory as stream data in a predetermined size; and
(b) if stream data in a predetermined size are accumulated in the non-volatile memory by repeating the above step (a), or accumulation of stream data of a corresponding broadcast program is completed, moving and storing the stream data in a hard disk drive.

20. The recorded medium of Claim 19, wherein, if a storage area of the volatile memory is divided into a first partitioned area and a second partitioned area, the step (a) comprises:

   starting an accumulation of stream data in the first partitioned area;

   if the storage space of the first partitioned area is completely used up, controlling the accumulated stream data to be moved to and stored in the non-volatile memory and controlling stream data for succeeding audio and video streams to be accumulated in the second partitioned area; and

   if the storage space of the second partitioned area is completed used up, controlling the accumulated stream data to be moved to and stored in the non-volatile memory and controlling stream data for succeeding audio and video streams to be accumulated in the first partitioned area.

21. The recorded medium of Claim 19, wherein, if a storage area of the non-volatile memory is divided into a buffering area and an NV storage area, the step (b) comprises:

   starting an accumulation of the stream data in the NV storage area; and
if the storage space of the NV storage area is completely used up, controlling the accumulated stream data to be moved to and stored in the hard disk drive and controlling succeeding stream data to be accumulated in the buffering area,

whereas, once the moving of the stream data accumulated in the NV storage area is completed, the buffering area is expanded by the storage space of the NV storage area and is re-designated as a new NV storage area, and the remaining storage space is re-designated as a new buffering area.

22. A recorded medium tangibly embodying a program of instructions executable by a digital video recorder to execute a method for playing back stream data, the program being readable by the digital video recorder, the program executing:

having a certain size of stream data with an earlier playback order stored in a volatile memory, the stream data with an earlier playback order being among stream data stored in a hard disk; and

having stream data following the stream data, which are stored in the volatile memory, stored in a non-volatile memory,

whereas the size of the stream data stored in the volatile memory is large enough to be played back while the succeeding stream data are stored in the non-volatile memory.
ABSTRACT

A digital video recorder having hierarchical memories and a method for implementing the hierarchical memories are disclosed. The digital video recorder in accordance with an embodiment of the present invention includes i) a storage unit, which includes a volatile memory, a non-volatile memory, and a hard disk drive and ii) a memory controller, which controls audio and video streams successively outputted from a demultiplexer to be moved to and stored in the volatile memory, the non-volatile memory, and the hard disk drive in the order of the volatile memory, non-volatile memory, and hard disk drive.
FIG. 2

210 Tuner

220 Demultiplexer

230 Decoder

240 Output unit

250 Memory controller

260 Non-volatile memory

270 Volatile memory

280 Hard disk drive
FIG. 3

Volatile memory
- First VM area
- Second VM area

Non-volatile memory
- Buffering area
- NV storage area

Hard disk drive
- HDD storage area
DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter claimed and for which a patent is sought on the invention entitled DIGITAL VIDEO RECORDER HAVING HIERARCHICAL MEMORIES AND METHOD FOR IMPLEMENTING HIERARCHICAL MEMORIES, the specification of which

☑ is attached hereto ☐ was filed on _____________ as Application Serial No. _____________ and was

amended on ________________ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is known to me to be material to patentability in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(c) or 365 (b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s):
Number Country Foreign Filing Date
10-2006-0075348 Republic of Korea August 9, 2006

I hereby claim the benefit under 35 U.S.C. 119(c) of any United States provisional application(s) listed below.

Application Number(s): Filing Date (Month/Day/Year)

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

Prior U.S. Application or PCT Parent Number Filing Date (Month/Day/Year) Parent Patent Number (if applicable)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the attorney(s) and/or agent(s) associated with Customer Number 34610 to prosecute this application and transact all business in the Patent and Trademark Office.
**Direct all correspondence to Customer Number 34610**

Full name of sole or first inventor: Tae-Gyu KIM

Inventor's signature: [Signature]

Date: August 4, 2007

Mailing Address: HUMAX Village 11-4, Sunae-dong, Bundang-gu, Seongnam-si, Gyeonggi-do 463-825, Republic of Korea

Citizenship: Republic of Korea

(only if different from mailing address): #416-1202, Neutimaeul, 90, Joongi-dong, Bundang-gu, Seongnam-si, Gyeonggi-do 463-010, Republic of Korea

Full name of joint inventor(s):

Inventor's signature: [Signature]

Mailing Address: [Address]

Citizenship: [Citizenship]

Residence Address: [Address]

(only if different from mailing address):

Full name of joint inventor(s):

Inventor's signature: [Signature]

Mailing Address: [Address]

Citizenship: [Citizenship]

Residence Address: [Address]

(only if different from mailing address):

Full name of joint inventor(s):

Inventor's signature: [Signature]

Mailing Address: [Address]

Citizenship: [Citizenship]

Residence Address: [Address]

(only if different from mailing address):

Full name of joint inventor(s):

Inventor's signature: [Signature]

Mailing Address: [Address]

Citizenship: [Citizenship]

Residence Address: [Address]

(only if different from mailing address):

Full name of joint inventor(s):

Inventor's signature: [Signature]

Mailing Address: [Address]

Citizenship: [Citizenship]

Residence Address: [Address]

(only if different from mailing address):
UTILITY PATENT APPLICATION TRANSMITTAL UNDER 37 C.F.R. §1.53(b)

U.S. Patent and Trademark Office
Customer Service Window, MAIL STOP PATENT APPLICATION
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Docket No.: EZ-0001

Sir:

Transmitted herewith for filing is the patent application of
INVENTORS:   Tac-Gyu KIM

FOR:    DIGITAL VIDEO RECORDER HAVING HIERARCHICAL MEMORIES AND METHOD FOR IMPLEMENTING HIERARCHICAL MEMORIES

Enclosed are:

1. ☑ 34 pages of specification, claims, abstract
2. ☐ 5 sheets of FORMAL drawings
3. ☐ 2 pages of newly executed Declaration & Power of Attorney (copy)
4. ☐ Priority claimed to Appln. No. 10/2006-0075348 filed on August 9, 2006 in Korea, whose entire disclosure is incorporated herein by reference.
5. ☐ Applicants claims Small Entity Status
6. ☐ Information Disclosure Statement, Form PTO-1449 and references
7. ☐ Assignment papers for HUMAX, Co., Ltd. cover sheet, assignment and assignment fee) (To Follow)
8. ☐ Certified copy of Priority Application No. 10/2006-0075348 filed on August 9, 2006 in Korea (To Follow)
9. ☐ Two (2) return postcards
   ☐ Stamp & Return with Courier
   ☐ Prepaid postcard-stamped filing date & returned with unofficial Serial Number
10. ☑ Authorization under 37 C.F.R. §1.136(a)(3)
12. ☑ Other: Preliminary Amendment

CLAIMS AS FILED

<table>
<thead>
<tr>
<th>For Independent Claims</th>
<th>No. Filed</th>
<th>No. Extra</th>
<th>Rate</th>
<th>Fee</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Claims</td>
<td>22</td>
<td>0</td>
<td>X $50.00</td>
<td>$0.00</td>
</tr>
<tr>
<td>Independent Claims</td>
<td>6</td>
<td>3</td>
<td>X $200.00</td>
<td>$600.00</td>
</tr>
</tbody>
</table>

APPLICATION SIZE FEE ( 100 = /50 x 250.00) $0.00

BASIC FILING FEE $300.00
UTILITY SEARCH FEE $500.00
UTILITY EXAMINATION FEE $200.00
TOTAL FILING FEE $1,600.00

☐ A check in the amount of $________ (Check #________) is attached.
☒ Please charge my Credit Card.
☒ Please charge my Deposit Account No. 16-0607 in the amount of $________. A duplicate copy of this sheet is enclosed.
☒ The Commissioner is hereby authorized to charge payment of following fees during the pendency of this application or credit any overpayment to Deposit Account No. 16-0607.
☒ Any additional filing fees required under 37 C.F.R. 1.16.
☒ Any patent application processing fees under 37 C.F.R. 1.17.
☒ Any filing fees under 37 C.F.R. 1.16 for presentation of extra claims.

Respectfully submitted,
KED & ASSOCIATES, LLP

Daniel Y.J. Kim
Registration No. 36,186

Correspondence Address:
P.O. Box 221200
Chantilly, Virginia 20153-1200
703 766-3777 initials

Date: August 8, 2007
Please direct all correspondence to Customer Number 34610
\\Fkl\Documents\2309\2309-001\130905.doc
UTILITY PATENT APPLICATION TRANSMITTAL UNDER 37 C.F.R. §1.53(b)

U.S. Patent and Trademark Office
Customer Service Window, MAIL STOP PATENT APPLICATION
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Docket No.: EZ-0001

Sir:

Transmitted herewith for filing is the patent application of
INVENTORS:  Tac-Gyu KIM

FOR: DIGITAL VIDEO RECORDER HAVING HIERARCHICAL MEMORIES AND METHOD FOR IMPLEMENTING HIERARCHICAL MEMORIES

Enclosed are:

1. ☑ 34 pages of specification, claims, abstract
2. ☑ 5 sheets of FORMAL drawings
3. ☑ 2 pages of newly executed Declaration & Power of Attorney (copy)
4. ☑ Priority claimed to Appln. No. 10/2006-0075348
   filed on August 9, 2006 in Korea, whose entire disclosure is incorporated herein by reference.
5. ☑ Applicant claims Small Entity Status
6. ☑ Information Disclosure Statement, Form PTO-1449 and _____ references

7. ☑ Assignment papers for HUMAX, Co., Ltd. cover sheet, assignment and assignment fee) (To Follow)
   filed on August 9, 2006 in Korea (To Follow)
9. ☑ Two (2) return postcards
   □ Stamp & Return with Courier
   □ Prepaid postcard-stamped filing date & returned with
   unofficial Serial Number
10. ☑ Authorization under 37 C.F.R. §1.136(a)(3)
12. ☑ Other Preliminary Amendment

CLAIMS AS FILED

<table>
<thead>
<tr>
<th>For</th>
<th>No. Filed</th>
<th>No. Extra</th>
<th>Rate</th>
<th>Fee</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Claims</td>
<td>22 - 20</td>
<td>0</td>
<td>X $50.00</td>
<td>$0.00</td>
</tr>
<tr>
<td>Independent Claims</td>
<td>6 - 3</td>
<td>3</td>
<td>X $200.00</td>
<td>$600.00</td>
</tr>
</tbody>
</table>

Multiple Dependent Claims (If applicable)

APPLICATION SIZE FEE ( - 100 = /50 x 250.00) $0.00
BASIC FILING FEE $300.00
UTILITY SEARCH FEE $500.00
UTILITY EXAMINATION FEE $200.00
TOTAL FILING FEE $1,600.00

☐ A check in the amount of $________ (Check #________) is attached.

☐ Please charge my Credit Card.

☐ Please charge my Deposit Account No. 16-0607 in the amount of $________. A duplicate copy of this sheet is enclosed.

☐ The Commissioner is hereby authorized to charge payment of following fees during the pendency of this application or credit any overpayment to Deposit Account No. 16-0607.

☐ Any additional filing fees required under 37 C.F.R. 1.16.
☐ Any patent application processing fees under 37 C.F.R. 1.17.
☐ Any filing fees under 37 C.F.R. 1.16 for presentation of extra claims.

Respectfully submitted,
KED & ASSOCIATES, LLP

Daniel Y. J. Kim
Registration No. 36,186

Correspondence Address:
P.O. Box 221200
Chantilly, Virginia 20153-1200
703 666-3777 initials

Date: August 8, 2007
Please direct all correspondence to Customer Number 34610

\Documents\2309\2309-001\139095\doc
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Tae-Gyu KIM

Customer No.: 34610

Serial No.: New U.S. Patent Application

Filed: August 8, 2007

For: DIGITAL VIDEO RECORDER HAVING HIERARCHICAL MEMORIES AND METHOD FOR IMPLEMENTING HIERARCHICAL MEMORIES

AUTHORIZATION TO TREAT A REPLY AS INCORPORATING AN EXTENSION OF TIME UNDER 37 C.F.R. §1.136(a)(3)

U.S. Patent and Trademark Office
Customer Service Window, MAIL STOP PATENT APPLICATION
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

The U.S. Patent and Trademark Office is hereby authorized to treat any concurrent or future reply that requires a petition for an extension of time under this paragraph for its timely submission, as incorporating a petition for extension of time for the appropriate length of time under 37 C.F.R. 1.136(a)(3). The U.S. Patent and Trademark Office is hereby authorized to charge all required extension of time fees to our Deposit Account No. 16-0607, if such fees are not otherwise provided for in such reply. A duplicate copy of this sheet is enclosed.

Respectfully submitted,
KED & ASSOCIATES, LLP

Daniel Y.J. Kim
Registration No. 36,186

Correspondence Address:
P.O. Box 221200
Chantilly, VA 20153-1200
703 766-3777 DYG/dsk
Date: August 8, 2007
Please direct all correspondence to Customer Number 34610

\Documents\2309\2309-001\130922.doc
| BASIC FEE (37 CFR 1.16(a), (b), or (c)) | NUMBER FILED | NUMBER EXTRA |
| SEARCH FEE (37 CFR 1.16(i), (l), or (m)) | | |
| EXAMINATION FEE (37 CFR 1.16(o), (p), or (q)) | | |
| TOTAL CLAIMS (37 CFR 1.16(i)) | 22 minus 20 = 2 | |
| INDEPENDENT CLAIMS (37 CFR 1.16(h)) | 6 minus 3 = 3 | |
| APPLICATION SIZE FEE (37 CFR 1.16(e)) | | |
| MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j)) | | |

- If the difference in column 1 is less than zero, enter "0" in column 2.

<p>| SMALL ENTITY | OTHER THAN SMALL ENTITY |</p>
<table>
<thead>
<tr>
<th>RATE ($)</th>
<th>FEE ($)</th>
<th>RATE ($)</th>
<th>FEE ($)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OR</td>
<td>X 25=</td>
<td>300</td>
<td></td>
</tr>
<tr>
<td></td>
<td>X 100=</td>
<td>500</td>
<td></td>
</tr>
</tbody>
</table>

TOTAL 1700

<p>| APPLICATION AS AMENDED – PART II |
|---|---|---|
| AMENDMENT A | SMALL ENTITY | OTHER THAN SMALL ENTITY |
| (Column 1) | (Column 2) | (Column 3) | OR | (Column 1) | (Column 2) | (Column 3) | OR |</p>
<table>
<thead>
<tr>
<th>CLAIMS REMAINING AFTER AMENDMENT</th>
<th>HIGHEST NUMBER PREVIOUSLY PAID FOR</th>
<th>PRESENT EXTRA</th>
<th>RATE ($)</th>
<th>ADDITIONAL FEE ($)</th>
<th>RATE ($)</th>
<th>ADDITIONAL FEE ($)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total (37 CFR 1.16(i))</td>
<td>**</td>
<td>Minus **</td>
<td>=</td>
<td>x =</td>
<td>x =</td>
<td></td>
</tr>
<tr>
<td>Independent (37 CFR 1.16(h))</td>
<td>**</td>
<td>Minus ***</td>
<td>=</td>
<td>x =</td>
<td>x =</td>
<td></td>
</tr>
<tr>
<td>Application Size Fee (37 CFR 1.16(e))</td>
<td>N/A</td>
<td>N/A</td>
<td></td>
<td>N/A</td>
<td>N/A</td>
<td></td>
</tr>
<tr>
<td>FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

TOTAL ADD’T FEE

<table>
<thead>
<tr>
<th>AMENDMENT B</th>
<th>SMALL ENTITY</th>
<th>OTHER THAN SMALL ENTITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Column 1)</td>
<td>(Column 2)</td>
<td>(Column 3)</td>
</tr>
<tr>
<td>CLAIMS REMAINING AFTER AMENDMENT</td>
<td>HIGHEST NUMBER PREVIOUSLY PAID FOR</td>
<td>PRESENT EXTRA</td>
</tr>
<tr>
<td>---</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>Total (37 CFR 1.16(i))</td>
<td>**</td>
<td>Minus **</td>
</tr>
<tr>
<td>Independent (37 CFR 1.16(h))</td>
<td>**</td>
<td>Minus ***</td>
</tr>
<tr>
<td>Application Size Fee (37 CFR 1.16(e))</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

TOTAL ADD’T FEE

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a copy of the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.