UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.  12/178,347  
ISSUE DATE  03/13/2012  
PATENT NO.  8135104  
ATTORNEY DOCKET NO.  KYO-139  
CONFIRMATION NO.  6126

23995  7590  02/22/2012
RABIN & Berdo, PC
1101 14TH STREET, NW
SUITE 500
WASHINGTON, DC 20005

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determinations of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 802 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):
Chulwoo Kim, Seoul, KOREA, REPUBLIC OF;
Inhwa Jung, Seoul, KOREA, REPUBLIC OF;

IR103 (Rev. 10/09)
### Bib Data Sheet

**CONFORMATION NO. 6126**

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**APPLICANTS**

Chulwoo Kim, Seoul, KOREA, REPUBLIC OF;
Inhwa Jung, Seoul, KOREA, REPUBLIC OF;

**CONTINUING DATA ********************

**FOREIGN APPLICATIONS ******************


** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **

** SMALL ENTITY **

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**ADDRESS**

23995

**TITLE**

SERIAL TRANSCEIVER AND COMMUNICATION METHOD USED BY THE SERIAL TRANSCEIVER

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**PART B - FEE(S) TRANSMITTAL**

Complete and send this form, together with applicable fee(s), to: **Mail**

Mail Stop ISSUE FEE Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

23965  7590
11/21/2011
RABIN & Berdo, PC
1101 14TH STREET, NW
SUITE 500
WASHINGTON, DC 20005

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

**Certificate of Mailing or Transmission**

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Deponent's name)
(Signature)
(Date)

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<td>Kim Chulwooo</td>
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<td>6126</td>
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**TITLE OF INVENTION: SERIAL TRANSEIVER AND COMMUNICATION METHOD USED BY THE SERIAL TRANSEIVER**

**APPLN. TYPE** | **SMALL ENTITY** | **ISSUE FEE DUE** | **PUBLICATION FEE DUE** | **PREV. PAID ISSUE FEE** | **TOTAL FEES DUE** | **DATE DUE**
---|---|---|---|---|---|---
nonprovisional | YES | $870 | $300 | $0 | $1170 | 02/21/2012

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<th>EXAMINER</th>
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<tr>
<td>PATEL, DHAVAL V</td>
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<td>375-374000</td>
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1. Change of correspondence address or indication of "Fee Address" (37 CFR 3.303).

☑ Change of correspondence address (or Change of Correspondence Address form PT/SB/122) attached.

☑ "Fee Address" indication (or "Fee Address" Indication form PT/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

3. **ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT** (print or type)

**PLEASE NOTE:** Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is **NOT** a substitute for filing an assignment.

(A) NAME OF ASSIGNEE
---
KOREA UNIVERSITY INDUSTRIAL & ACADEMIC COLLABORATION FOUNDATION

(B) RESIDENCE: (CITY and STATE OR COUNTRY)
---
SEOUL, REPUBLIC OF KOREA

Please check the appropriate assignee category or categories (will not be printed on the patent):

☑ Individual ☑ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☑ Issue Fee
☑ Publication Fee (No small entity discount permitted)
☑ Advance Order - # of Copies

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

☑ A check is enclosed.
☑ Payment by credit card. Form PTO-2038 is attached.

The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 12-0002 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature: /Jun-Hwa Jeong/

Date: February 8, 2012

Typed or printed name: Jun-Hwa Jeong

Registration No.: 68,419

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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PTOL-85 (Rev. 02/11) Approved for use through 08/31/2013.

OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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# NOTICE OF ALLOWANCE AND FEE(S) DUE

**EXAMINER**

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<th>PATHEL, DHAVAL V</th>
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**DATE MAILED:** 11/21/2011

**APPLICATION NO.**

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**TITLE OF INVENTION:** SERIAL TRANSCEIVER AND COMMUNICATION METHOD USED BY THE SERIAL TRANSCEIVER

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

**APPLN. TYPE** | **SMALL ENTITY** | **ISSUE FEE DUE** | **PUBLICATION FEE DUE** | **PREV. PAID ISSUE FEE** | **TOTAL FEE(S) DUE** | **DATE DUE** |
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**HOW TO REPLY TO THIS NOTICE:**

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as **YES**, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as **NO**:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the Issue FEE shown above.

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III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

**IMPORTANT REMINDER:** Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.
PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail
Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

or Fax
(571) -273-2885

23955 7590 11/21/2011
RABIN & Berdo, PC
1101 14TH STREET, NW
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WASHINGTON, DC 20005

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   (A) NAME OF ASSIGNEE

   (B) RESIDENCE: (CITY and STATE OR COUNTRY)

   Please check the appropriate assignee category or categories (will not be printed on the patent):
   □ Individual  □ Corporation or other private group entity  □ Government

4a. The following fee(s) are submitted:
   □ Issue Fee
   □ Publication Fee (No small entity discount permitted)
   □ Advance Order - # of Copies

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)
   □ A check is enclosed.
   □ Payment by credit card. Form PTO-2038 is attached.
   □ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number ____________________________ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)
   □ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
   □ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature ____________________________  Date ____________

Typed or printed name ____________________________  Registration No. ____________

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PTOL-85 (Rev. 02/11) Approved for use through 08/31/2013.  OMB 0651-0033  U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 568 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 568 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.
Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.
Notice of Allowability

--- The MAILING DATE of this communication appears on the cover sheet with the correspondence address---

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 10/28/2011.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-6, 8 and 9.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All  b) ☐ Some*  c) ☐ None  of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____.
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER’S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as “replacement sheets”) must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson’s Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner’s Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner’s comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner’s Comment Regarding Requirement for Deposit of Biological Material
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date 11/4/2011
7. ☒ Examiner’s Amendment/Comment
8. ☒ Examiner’s Statement of Reasons for Allowance
9. ☐ Other _____.

/Dhaval Patel/
Primary Examiner, Art Unit 2611
Examiner-Initiated Interview Summary

Application No. 12/178,347
Applicant(s) CHULWOO ET AL.
Examiner DHAVAL PATEL
Art Unit 2611

All participants (applicant, applicant’s representative, PTO personnel):

(1) DHAVAL PATEL.

(2) Jihwang Yeo.

Date of Interview: 11/4/2011.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant’s representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.

If Yes, brief description: ______.

Issues Discussed ☐101 ☐112 ☐102 ☐103 ☒Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: 1 and 8.

Identification of prior art discussed: n/a.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

During the discussion with the applicant’s representative, examiner has proposed the necessary amendment to make the claim more clear. Applicant has agreed to the proposed changes. Examiner’s amendment has been made to make those changes.

Applicant recordation instructions: It is not necessary for applicant to provide a separate record of the substance of interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/Dhaval Patel/
Examiner, Art Unit 2611
DETAILED ACTION

1. Examiner has acknowledged the amendment received on 10/28/2011. Claims 1-6, 8 and 9 are pending in the application.

EXAMINER’S AMENDMENT

2. An examiner’s amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

    Authorization for this examiner’s amendment was given in a telephone interview with Jihwang Yeo on 11/4/2011.

    The application has been amended as follows:

    In claims:

    1. (Currently amended) A serial transceiver, comprising:

        a transmitter which receives parallel data to be transmitted to encode the received parallel data as transmission data including DC (direct current) balancing information and includes a serial transmission unit for performing serial transmission on data encoded according to a communication clock of an internal PLL (phase locked loop) operating based on an externally provided clock; and

        a receiver which includes a clock recovery unit including a frequency detector and a linear phase detector for receiving the encoded data from the transmitter and performing sequential synchronization by using the received encoded data and an
output of an internal voltage controlled oscillator, a parallelizer for converting the received serial data into parallel data by using clocks of a plurality of stages output generated by the voltage controller oscillator from the clock recovery unit, a start bit detector for detecting a start bit by comparing data in the output of the parallelizer through a logic circuit, and a decoder for decoding and outputting the output of the parallelizer,

wherein the frequency detector comprises:

a divider dividing, during a delay time, signals among outputs of each clock of the plurality of stages generated by the voltage controlled oscillator of the plurality of stages according to a rate of the received data and outputting the divided signals;

a serial data delay for delaying the serial data by the amount of said delay time, and outputting a signal of the delayed serial data;

one or more synchronization detectors comparing an output of the delay to one of the outputs of the divider to detect synchronization and providing a result of the comparison as a synchronization signal; and

a frequency controller which outputs a frequency falling down signal to continuously decrease the frequency of a periodic pulse signal, which is the output of the divider, when the output of the delay and a the periodic pulse signal, which is the output of the divider, are different,

wherein the frequency controller and block generates and maintains the frequency falling down signal to be "0", when the frequency of the synchronization signal of the synchronization detector and the frequency of the output of the delay are
synchronized in a case when two synchronization detectors are used, both of the two synchronization detectors detect a lock condition,

wherein the lock condition is detected when the frequency of the output of the delay and the frequency of the periodic pulse signal are in synchronization with each other.

3. (Original) The serial transceiver of claim 1, wherein the clock recovery unit of the receiver includes:

the voltage controlled oscillator of a the plurality of stages in which a frequency range is determined by a coarse code;

an internal coarse code generator receiving an output of the voltage controlled oscillator and the received serial data as inputs to provide the coarse code for controlling the voltage controlled oscillator to the voltage controlled oscillator;

the frequency detector receiving the voltage controlled oscillator output in the frequency range determined by the output of the coarse code generator and the received parallel data as inputs to output a signal for controlling a voltage applied to the voltage controlled oscillator for frequency synchronization;

the linear phase detector receiving the voltage controlled oscillator output and the received parallel data as inputs in a case where the frequency synchronization is performed by the frequency detector to output a signal for controlling the voltage applied to the voltage controlled oscillator for phase synchronization; and
a charge pump selectively receiving the output from the frequency detector and the linear phase detector to control the voltage applied to the voltage controlled oscillator.

8. (Currently amended) A serial receiver which is connected to a transmitter that encodes and transmits parallel data as serial data, in order to receive the serial data, recovers a clock included in the serial data, and converts and decodes the serial data into parallel data to output the received clock and the decoded parallel data, the serial receiver comprising:

a clock recovery unit including a frequency detector and a linear phase detector for receiving the serial data from the transmitter and performing sequential synchronization by using the received serial data and an output of an internal voltage controlled oscillator;

a parallelizer for converting the received serial data into parallel data by using clocks of a plurality of stages generated by the voltage controller oscillator from the clock recovery unit;

a start bit detector for detecting a start bit by comparing data in the output of the parallelizer through a logic circuit; and

a decoder for decoding and outputting the output of the parallelizer

wherein the frequency detector comprises:
a divider dividing, during a delay time, signals among outputs of a each clock of
the plurality of stages generated by the voltage controlled oscillator of the plurality of
stages according to a rate of the received data and outputting the divided signals;

a serial data delayer for delaying the serial data delayed by the amount of said
delay time, and outputting a signal of the delayed serial data;

one or more synchronization detectors comparing an output of the delayer to one
of the outputs of the divider to detect synchronization and providing a result of the
comparison as a synchronization signal; and

a frequency controller which outputs a frequency falling down signal to
continuously decrease the frequency of a periodic pulse signal, which is the output of
the divider, when the output of the delayer and a the periodic pulse signal, which is the
output of the divider, are different,

wherein the frequency controller and blocks generates and maintains the
frequency falling down signal to be "0", when the frequency of the synchronization
signal of the synchronization detector and the frequency of the output of the delayer are
synchronized in a case when two synchronization detectors are used, both of the two
synchronization detectors detect a lock condition,

wherein the lock condition is detected when the frequency of the output of the
delayer and the frequency of the periodic pulse signal are in synchronization with each
other.
9. (Original) The serial receiver of claim 8, wherein the clock recovery unit includes:

- a the voltage controlled oscillator of a the plurality of stages in which a frequency range is determined by a coarse code;
- an internal coarse code generator receiving an output of the voltage controlled oscillator and the received serial data as inputs to provide the coarse code for controlling the voltage controlled oscillator to the voltage controlled oscillator;
- a the frequency detector receiving a the voltage controlled oscillator output in the frequency range determined by the output of the coarse code generator and the received parallel data as inputs to output a signal for controlling a voltage applied to the voltage controlled oscillator for frequency synchronization;
- a the linear phase detector receiving the voltage controlled oscillator output and the received parallel data as inputs in a case where the frequency synchronization is performed by the frequency detector to output a signal for controlling the voltage applied to the voltage controlled oscillator for phase synchronization; and
- a charge pump selectively receiving the output from the frequency detector and the linear phase detector to control the voltage applied to the voltage controlled oscillator.

Allowable Subject Matter

3. Claims 1-6, 8 and 9 are allowed.
The following is an examiner’s statement of reasons for allowance: The prior arts, as a whole, do not explicitly disclose a receiver which includes a clock recovery unit including a frequency detector and a linear phase detector for receiving the encoded data from the transmitter and performing sequential synchronization by using the received encoded data and an output of an internal voltage controlled oscillator, a parallelizer for converting the received serial data into parallel data by using clocks of a plurality of stages output from the clock recovery unit, a start bit detector for detecting a start bit by comparing data in the output of the parallelizer through a logic circuit, and a decoder for decoding and outputting the output of the parallelizer, in combination with disclosed frequency detector comparing the output of each divided clock of the plurality of stages generated by the voltage controlled oscillator and delayed serial data by the delay time of the divider and a frequency controller which outputs a frequency down signal to continuously decrease the frequency of a periodic pulse signal, which is the output of the divider, when the output of the delayer and the periodic pulse signal, are different, wherein the frequency controller generates and maintains the frequency down signal to be zero when two synchronization detectors are used, both of the two synchronization detectors detects a lock condition, wherein the lock condition is detected when the frequency of the output of the delayer and the frequency of the periodic pulse signal are in synchronization with each other. The distinct feature of the claims 1 and 8 render them allowable over prior arts. Claims 2-6 and 9 are dependent upon claims 1 and 8 respectively and therefore allowable.
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DHAVAL PATEL whose telephone number is (571)270-1818. The examiner can normally be reached on M-F 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dhaval Patel/
Primary Examiner, Art Unit 2611

11/9/2011
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| S42 | 1 | "11624862" | US-PUB; USPAT; UPAD | OR | ON | 2011/07/25 14:14 |
### Issue Classification

**Application/Control No.**
12178347

**Applicant(s)/Patent Under Reexamination**
CHULWOO ET AL.

**Examiner**
DHAVAL PATEL

**Art Unit**
2611

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**None**

(Assistant Examiner)  
(DATE)  
/DHAVAL PATEL/  
Primary Examiner. Art Unit 2611

(Primary Examiner)  
(DATE)  

**Total Claims Allowed:**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: 2611
Examiner: Dhaval V. Patel

In Re PATENT APPLICATION of:

Applicant(s): Kim Chulwoo et al.
Serial No.: 12/178,347
Filing date: July 23, 2008
For: SERIAL TRANSCIEVER AND COMMUNICATION METHOD USED BY THE SERIAL TRANSCIEVER

Atty. ref.: KYO-139

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Examiner's Action mailed on July 28, 2011, please amend the above-identified application as follows:
IN THE DRAWINGS:

Please enter the replacement sheet of drawings submitted as an attachment of this Amendment. More particularly, FIG. 7 has been amended.
CLAIM AMENDMENTS:

1. (Currently amended) A serial transceiver, comprising:

   a transmitter which receives parallel data to be transmitted to encode the received parallel data as transmission data including DC (direct current) balancing information and includes a serial transmission unit for performing serial transmission on data encoded according to a communication clock of an internal PLL (phase locked loop) operating based on an externally provided clock; and

   a receiver which includes a clock recovery unit including a frequency detector and a linear phase detector for receiving the encoded data from the transmitter and performing sequential synchronization by using the received encoded data and an output of an internal voltage controlled oscillator, a parallelizer for converting the received serial data into parallel data by using clocks of a plurality of stages output from the clock recovery unit, a start bit detector for detecting a start bit by comparing data in the output of the parallelizer through a logic circuit, and a decoder for decoding and outputting the output of the parallelizer,

   wherein the frequency detector comprises:

   a divider dividing, during a delay time, signals among outputs of a voltage controlled oscillator of the plurality of stages according to a rate of the received data and outputting the divided signals;

   a serial data delay for delaying the serial data [[delayed]] by [[a]] the amount of said delay time of the divider for dividing the output of the voltage controlled oscillator, and outputting a signal of the delayed serial data:
one or more synchronization detectors comparing an output of the delayer to one of the outputs of the divider to detect synchronization and providing a result of the comparison as a synchronization signal; and

a frequency controller which outputs a frequency falling signal when the output of the delayer and a periodic pulse signal, which is the output of the divider, are different by using a periodic pulse signal due to one of the outputs of the divider and the output of the delayer, in a case where a frequency difference occurs, and blocks the frequency falling signal when the frequency of the synchronization signal of the synchronization detector and the frequency of the output of the delayer are synchronized in a case where the frequency is synchronized by the synchronization signal of the synchronization detector and the output of the delayer.

2. (Original) The serial transceiver of claim 1, wherein the transmitter includes an encoding unit which receives a plurality of parallel data signals to divide a corresponding parallel data signal into two or more units, inserts information for DC balancing into the divided position, and inserts start information and end information into start and end portions of the entire data.

3. (Original) The serial transceiver of claim 1, wherein the clock recovery unit of the receiver includes:

the voltage controlled oscillator of a plurality of states in which a frequency range is determined by a coarse code;
an internal coarse code generator receiving an output of the voltage controlled oscillator and the received serial data as inputs to provide the coarse code for controlling the voltage controlled oscillator to the voltage controlled oscillator;

a frequency detector receiving a voltage controlled oscillator output in the frequency range determined by the output of the coarse code generator and the received parallel data as inputs to output a signal for controlling a voltage applied to the voltage controlled oscillator for frequency synchronization;

the linear phase detector receiving the voltage controlled oscillator output and the received parallel data as inputs in a case where the frequency synchronization is performed by the frequency detector to output a signal for controlling the voltage applied to the voltage controlled oscillator for phase synchronization; and

a charge pump selectively receiving the output from the frequency detector and the linear phase detector to control the voltage applied to the voltage controlled oscillator.

4. (Original) The serial transceiver of claim 3, wherein the clock recovery unit further includes:

a sampler for sampling the received serial data by using the output of the voltage controlled oscillator; and

an initiation circuit unit for generating and providing a coarse enable signal for determining whether or not the coarse code generator is to operate according to the output of the sampler to the coarse code generator.
5. (Original) The serial transceiver of claim 4,
wherein the charge pump further includes a switch for selectively connecting the
voltage applied to the voltage controlled oscillator to a maximum voltage or a minimum
voltage to allow the voltage controlled oscillator to operate at a maximum frequency, and
wherein the coarse enable signal is used as a control signal for operating the switch.

6. (Original) The serial transceiver of claim 3, wherein the voltage controlled
oscillator of the plurality of the stages has a stage having the same size as a value obtained
by adding bits of a data block divided by the inserted DC balancing information from
among the serial signals provided for a signal external clock and the half the inserted DC
balancing information and a start or a stop bit.

7. (Cancelled).

8. (Currently amended) A serial receiver which is connected to a transmitter that
encodes and transmits parallel data as serial data, in order to receive the serial data,
recovers a clock included in the serial data, and converts and decodes the serial data into
parallel data to output the received clock and the decoded parallel data, the serial receiver
comprising:

a clock recovery unit including a frequency detector and a linear phase detector for
receiving the serial data from the transmitter and performing sequential synchronization by
using the received serial data and an output of an internal voltage controlled oscillator;
a parallelizer for converting the received serial data into parallel data by using clocks of a plurality of stages output from the clock recovery unit;

a start bit detector for detecting a start bit by comparing data in the output of the parallelizer through a logic circuit; and

a decoder for decoding and outputting the output of the parallelizer wherein the frequency detector comprises:

a divider dividing, during a delay time, signals among outputs of a voltage controlled oscillator of the plurality of stages according to a rate of the received data and outputting the divided signals;

a serial data delay for delaying the serial data delayed by the amount of [[a]] said delay time of the divider for dividing the output of the voltage controlled oscillator, and outputting a signal of the delayed serial data;

one or more synchronization detectors comparing an output of the delay to one of the outputs of the divider to detect synchronization and providing a result of the comparison as a synchronization signal; and

a frequency controller which outputs a frequency falling signal when the output of the delay and a periodic pulse signal, which is the output of the divide, are different by using a periodic pulse signal due to one of the outputs of the divider and the output of the delay, in a case where a frequency difference occurs, and blocks the frequency falling signal when the frequency of the synchronization signal of the synchronization detector and the frequency of the output of the delay are synchronized in a case where the frequency is
synchronized by the synchronization signal of the synchronization detector and the output of the delay.

9. (Original) The serial receiver of claim 8, wherein the clock recovery unit includes:

   a voltage controlled oscillator of a plurality of stages in which a frequency range is determined by a coarse code;

   an internal coarse code generator receiving an output of the voltage controlled oscillator and the received serial data as inputs to provide the coarse code for controlling the voltage controlled oscillator to the voltage controlled oscillator;

   a frequency detector receiving a voltage controlled oscillator output in the frequency range determined by the output of the coarse code generator and the received parallel data as inputs to output a signal for controlling a voltage applied to the voltage controlled oscillator for frequency synchronization;

   a linear phase detector receiving the voltage controlled oscillator output and the received parallel data as inputs in a case where the frequency synchronization is performed by the frequency detector to output a signal for controlling the voltage applied to the voltage controlled oscillator for phase synchronization; and

   a charge pump selectively receiving the output from the frequency detector and the linear phase detector to control the voltage applied to the voltage controlled oscillator.

10-14. (Canceled).
REMARKS

The Office Action mailed on July 28, 2011, has been received and its contents carefully considered.

In this Amendment, applicants have amended claims 1 and 8, and canceled claim 10. Claims 1 and 8 are the independent claims, and claims 1-6, 8 and 9 remain pending in the application. Reconsideration of the application in view of the above amendments and the following remarks is respectfully requested.

Initially, applicants wish to thank the Examiner for indicating that claims 1-6, 8 and 9 include allowable subject matter.

The Examiner's Action has objected to the specification as failing to provide proper antecedent basis for the claimed subject matter. FIG. 7 of the drawings has been amended to address the matter specifically noted by the Examiner's Action. More particularly, amended FIG. 7 shows the frequency controller recited by claims 1 and 8. Accordingly, it is respectfully submitted that this objection should be reconsidered and withdrawn.

The Examiner's Action has rejected claims 1-6 and 8-10 under 35 U.S.C. §112, second paragraph, as being indefinite. Claim 10 has been canceled, thereby rendering the rejection of claim 10 moot.

Independent claims 1 and 8 have been amended to address the matters specifically noted by the Examiner's Action. More particularly, amended claims 1 and 8 recite “a
divider dividing, *during a delay time*, signals among outputs of a voltage controlled
oscillator of the plurality of stages according to a rate of the received data . . . ; a serial data
delayer for delaying the serial data *delayed by the amount of said delay time.*” *(emphasis
added)* Support is found in at least FIG. 7 of the drawings, and page 11, line 35 through
page 12, line 3 of the specification. Amended claims 1 and 8 also recite that “a frequency
controller which outputs a frequency falling signal *when the output of the delayer and a
periodic pulse signal, which is the output of the divider, are different, and blocks the
frequency falling signal when the frequency of the synchronization signal of the
synchronization detector and the frequency of the output of the delayer are synchronized.*”
*(emphasis added)* Support is found in at least page 12, lines 11 through page 13, line 25 of
the specification.

Accordingly, it is respectfully submitted that this rejection should be reconsidered
and withdrawn.

The Examiner’s Action also rejected claim 10 under 35 U.S.C. §103(a) as being
unpatentable over U.S. Patent No. 7,184,512 to Takeshita et al. in view of U.S. Patent No.
6,310,521 to Dalmia et al. Claim 10 has been canceled, thereby rendering the rejection
moot. Accordingly, it is respectfully submitted that this rejection should be withdrawn.

Based on the above, it is submitted that the application is in condition for allowance
and such a Notice, with allowed claims 1-6, 8 and 9, earnestly is solicited.
Should the Examiner have any questions or comments regarding this response, or the present application, the Examiner is invited to contact the undersigned at the below-listed telephone or fax number.

Should any fee be required, the Commissioner is hereby authorized to charge such fees to our deposit account No. 18-0002, and is requested to advise us accordingly.

Respectfully submitted,

October 28, 2011
Date

Jun-Hwa Jeong – Reg. No. 68,419
RABIN & BERDO, PC – Customer No. 23995
Facsimile: 202-408-0924; 202-408-5297
Telephone: 202-371-8976

JJ/JY
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**Title of Invention:** SERIAL TRANSCIEVER AND COMMUNICATION METHOD USED BY THE SERIAL TRANSCIEVER

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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.
PATENT APPLICATION FEE DETERMINATION RECORD

**APPLICATION AS FILED – PART I**

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| Independent (37 CFR 1.16(h)) | - | Minus | | = | X $ = | OR | X $ = |

* If the difference in column 1 is less than the entry in column 2, write "0" in column 3.

**If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(d).**

Legal Instrument Examiner:
SHAREILL COLES/
Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.
**Office Action Summary**

**Application No.**
12/178,347

**Applicant(s)**
CHULWOO ET AL.

**Examiner**
DHAVAL PATEL

**Art Unit**
2611

--- The MAILING DATE of this communication appears on the cover sheet with the correspondence address ---

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) ☑ Responsive to communication(s) filed on 13 May 2011.
2a) ☐ This action is FINAL.
2b) ☑ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) ☑ Claim(s) 1-6 and 8-10 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☑ Claim(s) 1-6 and 8-10 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9) ☑ The specification is objected to by the Examiner.
10) ☑ The drawing(s) filed on 23 July 2008 is/are: a) ☑ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12) ☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☑ All   b) ☐ Some * c) ☐ None of:

1. ☑ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☑ Notice of References Cited (PTO-892)
2) ☑ Notice of Draftsperson’s Patent Drawing Review (PTO-948)
3) ☑ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date ____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date ____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: ____
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DETAILED ACTION

Specification

1. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: For example, claim recites the "frequency controller" however, in specification does not explicitly disclose details of frequency controller. Applicant is suggested to point out if any other such as counter is referring to the frequency controller or any other device in drawing which is referred as frequency controller.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-6 and 8-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1, 8 and 10, claim recites the "serial data delay for delaying the serial data delayed by a delay time of the divider for dividing the output of the voltage controlled oscillator" it is not clear to examiner as what this means. What applicant is meaning by delaying serial data by a delay time of the divider. Applicant is suggested to clarify the subject matter. Furthermore, it’s also unclear what it means by blocks the frequency falling signal in a case where the frequency is synchronized by the
synchronization signal of the synchronization detector and output of the delay. Claims 2-6,8 and 9 are rejected as being dependent upon claims 1 and 8 respectively and claims 1 and 8 are rejected.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

   (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

   The factual inquiries set forth in Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows: (See MPEP Ch. 2141)

   a. Determining the scope and contents of the prior art;
   b. Ascertaining the differences between the prior art and the claims in issue;
   c. Resolving the level of ordinary skill in the pertinent art; and
   d. Evaluating evidence of secondary considerations for indicating obviousness or nonobviousness.

4. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takeshita et al. (US 7,184,512) (hereafter Takeshita) in view of Dalmia et al. (US 6,310,521) (hereafter Dalmia).

   Regarding claim 10, Takeshita discloses a serial receiver which is connected to a transmitter that encodes and transmits parallel data as serial data, in order to receive the serial data, recovers a clock included in the serial data, converts and decodes the serial data into parallel data to output the received clock and the decoded parallel data,
and comprises a clock recovery unit including a frequency detector for recovering a clock, wherein the frequency detector (Fig. 1, 12) comprises:

- a divider dividing signals among outputs of a voltage controlled oscillator of the plurality of stages according to a rate of the received data (Fig. 1, VCO, 16, divider, 175 and phase shift circuit with I and Q clock generation);

- a serial data delay for delaying the serial data delayed by a delay time of the divider for dividing the output of the voltage controlled oscillator (Fig. 1, data, 18 to the D-FF, 124 and D-FF, 125, see, Fig. 5 and Fig. 6, frequency detector with data to the flip-flops delayed by a clock of VCO which is feedback clock, since, the data is sampled at different timing are considered as delayed data);

- one or more synchronization detectors comparing an output of the delay to one of the outputs of the divider to detect synchronization and providing a result of the comparison as a synchronization signal (Fig. 2 and Fig. 6, the gates, 36, 38, 39 are considered as synchronization detectors since its comparing the data sampled at the different clock signals both are phase shifted or delayed clocks); and

- a frequency controller which outputs a frequency falling signal by using a periodic pulse signal due to one of the outputs of the divider and the output of the delay, in a case where a frequency difference occurs, and blocks the frequency falling signal in a case where the frequency is synchronized by the synchronization signal of the synchronization detector and the output of the delay (see, Fig. 6, the flip flops after comparison generates the up and down control signal).
Takeshita does not explicitly disclose blocks the frequency falling signal in a case where the frequency is synchronized by the synchronization signal of the synchronization detector and the output of the delayer.

However, in the same field of endeavor, Dalmia teaches frequency detector in which col. 4 lines 22-30 teaches during lock acquisition, the frequency detector 104 is generally active and when the loop is locked (here considered as both are in synchronization) the frequency detector 104 may stop generating the up and down signals, the counter may eventually reaching the count value and stop (here considered as blocking). The counter may decode the value N to generate the control signal to VCO, so, here, clearly teaches the frequency detector stops generating control signal using counter, also, one of ordinary skilled in the art would know that, up and down signal can be generated as rising or falling signal. Furthermore, see, col. 4 lines 54-60 that the output signal can be of different state including reset state.

Therefore, it would have been obvious to one of ordinary skilled in the art at the time of the invention to combine the teachings of Dalmia, into the system of Takeshita, as a whole, to generate the control signal using the frequency detector based on the frequency comparison, the motivation is to improve the jitter tolerance and improve clock data recovery.

**Allowable Subject Matter**

5. Claims 1-6, 8 and 9 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patel Dhaval whose telephone number is (571) 270-1818. The examiner can normally be reached on M-F 8:30-6:00. If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Shuwang Liu can be reached on (571) 272-3036. Customer Service can be reached at (571) 272-2600. The fax number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Dhaval Patel/
Primary Examiner, Art Unit 2611

7/26/2011
**Notice of References Cited**

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**FOREIGN PATENT DOCUMENTS**

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**NON-PATENT DOCUMENTS**

Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages

| U | |
| V | |
| W | |
| X | |

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)

Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.*
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**APPLICANTS**
- Kim Chulwoo, Seoul, KOREA, REPUBLIC OF;
- Jung Inhwa, Seoul, KOREA, REPUBLIC OF;

**CONTINUING DATA**

**FOREIGN APPLICATIONS**

**IF REQUIRED, FOREIGN FILING LICENSE GRANTED**
- **SMALL ENTITY**
- 08/01/2008

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**ADDRESS**

RABIN & Berdo, PC  
1101 14TH STREET, NW  
SUITE 500  
WASHINGTON, DC 20005  
UNITED STATES

**TITLE**

SERIAL TRANSEceiver AND COMMUNICATION METHOD USED BY THE SERIAL TRANSEceiver

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## EAST Search History

### EAST Search History (Prior Art)

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group art unit: 2611
Examiner: Dhaval V. Patel

Re PATENT APPLICATION of:

Applicant(s): Chulwoo KIM et al.
Serial No.: 12/178,347
Filing date: June 23, 2008
For: SERIAL TRANSCEIVER AND
COMMUNICATION METHOD USED BY
THE SERIAL TRANSCEIVER
Atty. ref.: KYO 139

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Examiner Patel:

Responsive to the Restriction Requirement mailed on April 14, 2011, Applicants elect the invention of Group II, i.e., the subject matter of claim 10, for further examination. The election is made with traverse, along with a Preliminary Amendment filed herewith.

May 13, 2011

In the Preliminary Amendment, independent claims 1 and 8 have been amended to include all of the limitations of claim 10, and claims 7 and 11-14 have been canceled. Accordingly, in response to the Examiner's consideration provided in the Action, page 2, lines 4-5 from the bottom, it is submitted that the clock recovery circuit of amended claim 1 now necessarily require the same functionality as disclosed in claim 10 for frequency detector. In the same token, the clock recovery unit of amended claim 8 now necessarily require the same functionality as disclosed in claim 10 for frequency detector.
The Examiner's attention is further respectfully directed to MPEP § 803, which specifically states that if the search and examination of the entire application can be made without serious burden, the Examiner must examine the entire application on the merits, even though it includes claims to independent or distinct inventions. It is submitted that examination of the entire application, including claims 1-6 and 8-10 pending after the Preliminary Amendment, would not constitute a serious burden on the part of the Examiner, since there is substantial overlap between the elected claims (claim 10) and the non-elected claims (amended claims 1-6 and 8-9). It is thus requested that the Examiner examine all of the claims pending in the application.

Please amend the claims as follows:

Claim Amendments begin on page 3 of this paper

Remarks begin on page 8 of this paper.
CLAIM AMENDMENTS:

1. (Currently amended) A serial transceiver comprising:
   a transmitter which receives parallel data to be transmitted to encode the
   received parallel data as transmission data including DC (direct current) balancing
   information and includes a serial transmission unit for performing serial transmission on
   data encoded according to a communication clock of an internal PLL (phase locked
   loop) operating based on an externally provided clock; and
   a receiver which includes a clock recovery unit including a frequency detector
   and a linear phase detector for receiving the encoded data from the transmitter and
   performing sequential synchronization by using the received encoded data and an
   output of an internal voltage controlled oscillator, a parallelizer for converting the
   received serial data into parallel data by using clocks of a plurality of stages output from
   the clock recovery unit, a start bit detector for detecting a start bit by comparing data in
   the output of the parallelizer through a logic circuit, and a decoder for decoding and
   outputting the output of the parallelizer,
   wherein the frequency detector comprises:
   a divider dividing signals among outputs of a voltage controlled oscillator of the
   plurality of stages according to a rate of the received data;
   a serial data delay for delaying the serial data delayed by a delay time of the
   divider for dividing the output of the voltage controlled oscillator;
   one or more synchronization detectors comparing an output of the delay to
   one of the outputs of the divider to detect synchronization and providing a result of the
   comparison as a synchronization signal; and
   a frequency controller which outputs a frequency falling signal by using a
   periodic pulse signal due to one of the outputs of the divider and the output of the
   delay, in a case where a frequency difference occurs, and blocks the frequency falling
   signal in a case where the frequency is synchronized by the synchronization signal of
   the synchronization detector and the output of the delay.

2. (Original) The serial transceiver of claim 1, wherein the transmitter includes an
   encoding unit which receives a plurality of parallel data signals to divide a
corresponding parallel data signal into two or more units, inserts information for DC balancing into the divided position, and inserts start information and end information into start and end portions of the entire data.

3. (Original) The serial transceiver of claim 1, wherein the clock recovery unit of the receiver includes:

   the voltage controlled oscillator of a plurality of states in which a frequency range is determined by a coarse code;

   an internal coarse code generator receiving an output of the voltage controlled oscillator and the received serial data as inputs to provide the coarse code for controlling the voltage controlled oscillator to the voltage controlled oscillator;

   a frequency detector receiving a voltage controlled oscillator output in the frequency range determined by the output of the coarse code generator and the received parallel data as inputs to output a signal for controlling a voltage applied to the voltage controlled oscillator for frequency synchronization;

   the linear phase detector receiving the voltage controlled oscillator output and the received parallel data as inputs in a case where the frequency synchronization is performed by the frequency detector to output a signal for controlling the voltage applied to the voltage controlled oscillator for phase synchronization; and

   a charge pump selectively receiving the output from the frequency detector and the linear phase detector to control the voltage applied to the voltage controlled oscillator.

4. (Original) The serial transceiver of claim 3, wherein the clock recovery unit further includes:

   a sampler for sampling the received serial data by using the output of the voltage controlled oscillator; and

   an initiation circuit unit for generating and providing a coarse enable signal for determining whether or not the coarse code generator is to operate according to the output of the sampler to the coarse code generator.
5. (Original) The serial transceiver of claim 4,
wherein the charge pump further includes a switch for selectively connecting the voltage applied to the voltage controlled oscillator to a maximum voltage or a minimum voltage to allow the voltage controlled oscillator to operate at a maximum frequency, and
wherein the coarse enable signal is used as a control signal for operating the switch.

6. (Original) The serial transceiver of claim 3, wherein the voltage controlled oscillator of the plurality of the stages has a stage having the same size as a value obtained by adding bits of a data block divided by the inserted DC balancing information from among the serial signals provided for a signal external clock and the half the inserted DC balancing information and a start or a stop bit.

7. (Cancelled).

8. (Currently amended) A serial receiver which is connected to a transmitter that encodes and transmits parallel data as serial data, in order to receive the serial data, recovers a clock included in the serial data, and converts and decodes the serial data into parallel data to output the received clock and the decoded parallel data, the serial receiver comprising:

   a clock recovery unit including a frequency detector and a linear phase detector for receiving the serial data from the transmitter and performing sequential synchronization by using the received serial data and an output of an internal voltage controlled oscillator;

   a parallelizer for converting the received serial data into parallel data by using clocks of a plurality of stages output from the clock recovery unit;

   a start bit detector for detecting a start bit by comparing data in the output of the parallelizer through a logic circuit; and

   a decoder for decoding and outputting the output of the parallelizer

   wherein the frequency detector comprises:
a divider dividing signals among outputs of a voltage controlled oscillator of the plurality of stages according to a rate of the received data;
a serial data delayer for delaying the serial data delayed by a delay time of the divider for dividing the output of the voltage controlled oscillator;
one or more synchronization detectors comparing an output of the delayer to one of the outputs of the divider to detect synchronization and providing a result of the comparison as a synchronization signal; and
a frequency controller which outputs a frequency falling signal by using a periodic pulse signal due to one of the outputs of the divider and the output of the delayer, in a case where a frequency difference occurs, and blocks the frequency falling signal in a case where the frequency is synchronized by the synchronization signal of the synchronization detector and the output of the delayer.

9. (Original) The serial receiver of claim 8, wherein the clock recovery unit includes:
a voltage controlled oscillator of a plurality of stages in which a frequency range is determined by a coarse code;
an internal coarse code generator receiving an output of the voltage controlled oscillator and the received serial data as inputs to provide the coarse code for controlling the voltage controlled oscillator to the voltage controlled oscillator;
a frequency detector receiving a voltage controlled oscillator output in the frequency range determined by the output of the coarse code generator and the received parallel data as inputs to output a signal for controlling a voltage applied to the voltage controlled oscillator for frequency synchronization;
a linear phase detector receiving the voltage controlled oscillator output and the received parallel data as inputs in a case where the frequency synchronization is performed by the frequency detector to output a signal for controlling the voltage applied to the voltage controlled oscillator for phase synchronization; and
a charge pump selectively receiving the output from the frequency detector and the linear phase detector to control the voltage applied to the voltage controlled oscillator.
10. (Original) A serial receiver which is connected to a transmitter that encodes and transmits parallel data as serial data, in order to receive the serial data, recovers a clock included in the serial data, converts and decodes the serial data into parallel data to output the received clock and the decoded parallel data, and comprises a clock recovery unit including a frequency detector for recovering a clock, wherein the frequency detector comprises:

- a divider dividing signals among outputs of a voltage controlled oscillator of the plurality of stages according to a rate of the received data;
- a serial data delay for delaying the serial data delayed by a delay time of the divider for dividing the output of the voltage controlled oscillator;
- one or more synchronization detectors comparing an output of the delay to one of the outputs of the divider to detect synchronization and providing a result of the comparison as a synchronization signal; and
- a frequency controller which outputs a frequency falling signal by using a periodic pulse signal due to one of the outputs of the divider and the output of the delay, in a case where a frequency difference occurs, and blocks the frequency falling signal in a case where the frequency is synchronized by the synchronization signal of the synchronization detector and the output of the delay.

11. (Cancelled).

12. (Cancelled).

13. (Cancelled).

14. (Cancelled).
REMARKS

In the Preliminary Amendment, claims 1 and 8 have been amended to include all of the limitations of claim 10, and claims 7 and 11-14 have been canceled. Claims 1-6 and 8-10 remain pending in the application.

Again, Applicants' election of the invention of Group II, i.e., the subject matter of claim 10, is made with traverse. Examination of all of the pending claims on the merits is respectfully requested.

Respectfully submitted,

May 13, 2011
Date

Jun-Hwa Jeong
Limited Recognition No. L0471
RABIN & BERDO, PC
Customer No. 23995
Telephone: 202-371-8976
Fax: 202-408-0924

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Legal Instrument Examiner:
SHERRY DAVIS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.
Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.
Office Action Summary

Application No. 12/178,347
Applicant(s) CHULWOO ET AL.

Examiner DHAVAL PATEL
Art Unit 2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply to the Notice will result in ABANDONMENT of this application. See 37 CFR 1.136(c).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on 23 July 2008.
2a)☐ This action is FINAL. 2b)☐ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-14 are pending in the application.
   4a) Of the above claim(s) ______ is/are withdrawn from consideration.
5)☐ Claim(s) ______ is/are allowed.
6)☐ Claim(s) ______ is/are rejected.
7)☐ Claim(s) ______ is/are objected to.
8)☒ Claim(s) 1-14 are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☐ The drawing(s) filed on ______ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a)☐ All  b)☐ Some *  c)☐ None of:
       1.☐ Certified copies of the priority documents have been received.
       2.☐ Certified copies of the priority documents have been received in Application No. ______.
       3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson’s Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date ______.
4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date ______.
5)☐ Notice of Informal Patent Application
6)☐ Other: ______.
DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-9 and 12-14, drawn to transceiver, classified in class 375, subclass 219.

   II. Claim 10, drawn to a frequency detector, classified in class 375, subclass 344 or 375

   III. Claim 11, drawn to a linear phase detector, classified in class 375, subclass 371 or 373

The inventions are distinct, each from the other because of the following reasons:

2. Inventions I, II and III are related as combination and subcombination. Claim 1 recites transmitter and receiver with the receiver having frequency detector, linear phase detector etc. in the clock recovery circuit. So, clock data recovery circuit with frequency and phase detector can be used in any phase locking circuit during synchronization process or when the transmitter and receiver has to be synchronized with each other with the clock recovery circuit which does not require any specific details about as how the frequency detector as claimed in claim 10 and linear phase detector as in claim 11. Claim 1 clock recovery circuit which does not necessarily require the same functionality as disclosed in claim 10 for frequency detector and claim 11 for linear phase detector for clock and data synchronization, and the frequency detector and phase as disclosed would work in any other circuit not necessarily require in serial transceiver. Receiver with frequency synchronization would use such circuit which does
not require phase synchronization. As frequency and phase detector it-self does not required to be working together for synchronization as frequency and phase synchronization is separate synchronization process. Therefore, it is an additional burden for examiner to search for broad claim as clock data recovery circuit and specific details about the frequency and phase detector in clock data recovery circuit, thus, claim 1, claim 10 and 11 is distinct in nature and restriction is required.

3. The examiner has required restriction between combination and subcombination inventions. Where applicant elects a subcombination, and claims thereto are subsequently found allowable, any claim(s) depending from or otherwise requiring all the limitations of the allowable subcombination will be examined for patentability in accordance with 37 CFR 1.104. See MPEP § 821.04(a). Applicant is advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application.

4. Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and/or examination burden if restriction were not required because at least the following reason(s) apply:

   Applicant is advised that the reply to this requirement to be complete must include (i) an election of a invention to be examined even though the requirement
may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected invention.**

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DHAVAL PATEL whose telephone number is (571)270-1818. The examiner can normally be reached on M-F 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dhaval Patel/
Examiner, Art Unit 2611
4/11/2011
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Title: SERIAL TRANSCEIVER AND COMMUNICATION METHOD USED BY THE SERIAL TRANSCEIVER

Publication Date: 01/29/2009

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

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CONFIRMATION NO. 6126

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Date Mailed: 08/07/2008

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Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted: 08/01/2008
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is US 12/178,347

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Application Data Sheet

Application Information

Application Type:: Regular
Subject Matter:: Utility
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Correspondence Customer Number: 23995

Representative Information
Representative Customer Number: 23995

Domestic Priority Information

Foreign Priority Information

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Assignee Information
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As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and that I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SERIAL TRANSCEIVER AND COMMUNICATION METHOD USED BY THE SERIAL TRANSCEIVER

the specification of which
[X] is attached hereto.
[ ] was filed on ________________________, as Application Serial No. ________________________,
and was amended on ________________________ [If applicable];
[ ] was filed under the Patent Cooperation Treaty on ________________________
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I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims as amended by any amendments specifically referred to herein.

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I hereby appoint the following attorneys to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith: Steven M. Rabin (Reg. No. 29,102), Robert H. Bordo, Jr. (Reg. No. 36,075), Phillip G. Avruch (Reg. No. 48,076), Allen Wood (Reg. No. 28,134) and Nicholas S. Bromer (Reg. No. 33,478), 1101 14 Street, N.W., Suite 500, Washington, D.C. 20005, Telephone: (202)37 1-8976; Fax: (202)408-0924. Address all correspondence to:

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SERIAL TRANSCEIVER AND COMMUNICATION METHOD USED BY THE SERIAL TRANSCEIVER

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a serial transceiver, and more particularly, to a high speed transceiver without using an external clock signal and a communication method used by the high speed transceiver.

2. Description of the Related Art

As various communication methods have been developed and widely used, the demand of users for multimedia increases. Accordingly, studies for transmitting a larger amount of data at a higher speed more stably and minimizing a hardware configuration needed for the transmission have been made.

In general, in order to increase a data rate, one is selected from among a parallel transmission method of increasing the number of channels and simultaneously transmitting a number of pieces of data and a serial transmission method of transmitting data at a high speed through a single channel, to maximize the functions. Here, the parallel transmission method has problems in that data skew which means time differences between data transmitted through difference channels may exist between the various transmission channels, and as the number of channels increases, hardware costs increase. Therefore, the serial data transmission method is employed as a standard for a high speed transceiver and has been widely used. Moreover, studies for configuring high speed serial communications in parallel have been carried out. Since a rate of data transceived in the serial data transceiver is very high, data uncertainty increases due to noise and channel bandwidths. In order to reduce the data transmission uncertainty, the receiver has to recover a clock to have a smaller amount of jitter to perform sampling on input data and has to maintain a phase relationship between the recovered clock and the input data at an optimal state so that a bit error ratio (BER) is minimized. Therefore, in the high speed serial communications, a role of a clock recovery circuit for re-arranging clock signals in an optimal state to enable the receiver to receive a clock and data from the transmitter and perform sampling on the input data, is very important.
A general high speed data transceiver is constructed to simultaneously transmit a reference clock signal for providing a synchronization reference for high speed transception data in order to transmit data from the transmitter to the receiver. However, in this method, in a case where data has to be transmitted for a long distance ranging several meters, due to skew between the data and the reference clock, the receiver may have problems in recovering data. In addition, in order to change the transmission speed, the conventional transceiver has to change a reference clock signal of the receiver according to the transmission speed. In addition, in order to control the operation speed of the receiver, the transceiver has to change a digital code.

In order to solve the aforementioned problems, US Patent No. 6,680,970 discloses statistical methods and systems for data rate detection for multi-speed embedded clock serial receivers to detect an edge of data. However, in this case, due to limitations of data edge detection, jitter of a recovered clock signal is higher than in a case of using a linear phase detector. Therefore, speed limitations occur, and error possibility increases.

For another method, US Patent No. 5,838,749 discloses a method and apparatus for extracting an embedded clock from a digital data signal. In this method and apparatus, a scheme for loading a clock supplier on a clock recovery circuit is used in order to solve the aforementioned problems. However, due to the loaded clock supplier, there are problems in that areas, costs, and power are increased.

**SUMMARY OF THE INVENTION**

<Technical Problem>

The present invention provides a serial transceiver and a communication method used by the serial transceiver which applies a clock recovery circuit including a coarse code generator, a frequency detector, and a linear phase detector to the receiver so as to solve problems such as skew between a reference clock and data that may occur during data transmission and jitter of a recovered clock while an embedded clock method of applying clock information to data is used.

The present invention also provides a serial transceiver and a communication method used by the serial transceiver which do not transmit a reference clock while transmits data so as to solve a problem of skew between the data and the reference
clock and reduce the number of transmission channels and hardware costs.

The present invention also provides a serial transceiver and a communication method used by the serial transceiver which can control a speed without an additional external operation so as not to allow data to be transmitted along with a reference clock and applies a linear phase detection method to significantly decrease jitter of a recovered clock signal.

The present invention also provides a serial transceiver and a communication method used by the serial transceiver which can recover a clock signal without an additional circuit such as a clock supplier.

The present invention also provides a serial transceiver and a communication method used by the serial transceiver which applies a frequency detector for controlling an operation frequency of a voltage controlled oscillator by comparing an output of the voltage controlled oscillator with data delayed by dividing the output by a data rate to a clock recovery unit so as to generate an accurate lock signal.

The present invention also provides a serial transceiver and a communication method used by the serial transceiver which applies a linear phase detector for detecting a case of having a rising edge of serial data and controlling a charge pump by using a pulse according to a phase difference between a clock signal and the serial data signal to a clock recovery unit.

<Technical Solution>

According to an aspect of the present invention, there is provided a serial transceiver including: a transmitter which receives parallel data to be transmitted to encode the received parallel data as transmission data including direct current (DC) balancing information and includes a serial transmission unit for performing serial transmission on data encoded according to a communication clock of an internal phase locked loop (PLL) operating based on an externally provided clock; and a receiver which includes a clock recovery unit including a frequency detector and a linear phase detector for receiving the encoded data from the transmitter and performing sequential synchronization by using the received encoded data and an output of an internal voltage controlled oscillator, a parallelizer for converting the received serial data into parallel data by using clocks of a plurality of stages output from the clock recovery unit, a start bit detector for detecting a start bit by comparing data in the output of the parallelizer through a logic circuit, and a decoder for
decoding and outputting the output of the parallelizer.

In the above aspect of the present invention, the transmitter may include an encoding unit which receives a plurality of parallel data signals to divide a corresponding parallel data signal into two or more units, inserts information for DC balancing into the divided position, and inserts start information and end information into start and end portions of the entire data.

In addition, the clock recovery unit of the receiver may include: the voltage controlled oscillator of a plurality of states in which a frequency range is determined by a coarse code; an internal coarse code generator receiving an output of the voltage controlled oscillator and the received serial data as inputs to provide the coarse code for controlling the voltage controlled oscillator to the voltage controlled oscillator; a frequency detector receiving a voltage controlled oscillator output in the frequency range determined by the output of the coarse code generator and the received parallel data as inputs to output a signal for controlling a voltage applied to the voltage controlled oscillator for frequency synchronization; the linear phase detector receiving the voltage controlled oscillator output and the received parallel data as inputs in a case where the frequency synchronization is performed by the frequency detector to output a signal for controlling the voltage applied to the voltage controlled oscillator for phase synchronization; and a charge pump selectively receiving the output from the frequency detector and the linear phase detector to control the voltage applied to the voltage controlled oscillator.

In addition, the clock recovery unit may further include: a sampler for sampling the received serial data by using the output of the voltage controlled oscillator; and an initiation circuit unit for generating and providing a coarse enable signal for determining whether or not the coarse code generator is to operate according to the output of the sampler to the coarse code generator.

According to another aspect of the present invention, there is provided a serial transmitter connected to a serial receiver to transmit parallel data as serial data, including: an encoding unit receiving the parallel data to be transmitted and encoding the received parallel data as transmission data including DC balancing information and start and end information; a serializer using an output clock of an internal PLL according to an externally provided clock as a communication clock to provide synchronization signals in a serial communication manner; and a serial transmission unit for performing serial transmission on data encoded according to the
communication clock.

According to another aspect of the present invention, there is provided a serial receiver which is connected to a transmitter that encodes and transmits parallel data as serial data, in order to receive the serial data, recovers a clock included in the serial data, and converts and decodes the serial data into parallel data to output the received clock and the decoded parallel data, the serial receiver including: a clock recovery unit including a frequency detector and a linear phase detector for receiving the serial data from the transmitter and performing sequential synchronization by using the received serial data and an output of an internal voltage controlled oscillator; a parallelizer for converting the received serial data into parallel data by using clocks of a plurality of stages output from the clock recovery unit; a start bit detector for detecting a start bit by comparing data in the output of the parallelizer through a logic circuit; and a decoder for decoding and outputting the output of the parallelizer.

According to another aspect of the present invention, there is provided a serial receiver including a clock recovery unit including a frequency detector for recovering a clock, wherein the frequency detector includes: a divider dividing signals among outputs of a voltage controlled oscillator of the plurality of stages according to a rate of the received data; a serial data delay for delaying the serial data delayed by a delay time of the divider for dividing the output of the voltage controlled oscillator; one or more synchronization detectors comparing an output of the delay to one of the outputs of the divider to detect synchronization and providing a result of the comparison as a synchronization signal; and a frequency controller which outputs a frequency falling signal by using a periodic pulse signal due to one of the outputs of the divider and the output of the delay, in a case where a frequency difference occurs, and blocks the frequency falling signal in a case where the frequency is synchronized by the synchronization signal of the synchronization detector and the output of the delay.

According to another aspect of the present invention, there is provided a serial receiver including a clock recovery unit including a linear phase detector for recovering a clock, wherein the linear phase detector includes: a delay for delaying initial stage and final stage output signals from among the outputs of the voltage controlled oscillator of the plurality of the stages and the received data; a rising edge detector for detecting a rising edge of the serial data by sampling the serial received
data according to the initial stage and the final stage output signals; and a phase
detector receiving the received data delayed by the delayer, an output of the rising
edge detector, the initial stage and the final stage output of the voltage controlled
oscillator delayed by the delayer as inputs, and based on the rising edge of the
delayed serial data, outputting a pulse between rising edges of the delayed final
stage output and the initial stage output of the voltage controlled oscillator as a
signal for adjusting a voltage to be applied to the voltage controlled oscillator.

According to another aspect of the present invention, there is provided a
communication method used in a serial transceiver including: a transmitting step of,
in a case where the transmitter and the receiver are connected through a serial
channel, dividing practical data into a plurality of uniform sizes to insert DC balancing
information into every divided area, and inserting start and end information into the
entire data to encode and perform serial transmission on practical transmission data
having redundant information through the serial channel, by the transmitter, and a
receiving step of generating a clock signal corresponding to a data transmission rate
trough a frequency detection manner by using the practical transmission data
received through the serial channel, recovering a clock by controlling a phase of the
clock synchronized in a linear phase detection manner, acquiring data from the
practical transmission data serially received, and decoding and outputting the data
as original data without the redundant information, by the receiver.

BRIEF DESCRIPTION OF THE DRAWINGS
The above and other features and advantages of the present invention will
become more apparent by describing in detail exemplary embodiments thereof with
reference to the attached drawings in which:

FIG. 1 is a block diagram illustrating a construction of a high speed
transceiver without using a reference clock;

FIG. 2 is a view illustrating a signal transmission type of the high speed
transceiver;

FIG. 3 is a block diagram illustrating a construction of a clock recovery circuit;

FIG. 4 is a block diagram illustrating a construction of an initiation circuit unit;

FIG. 5 is a block diagram illustrating a construction of a coarse voltage
generator;

FIG. 6 is a block diagram illustrating a construction of a 1-0 detector included
in the coarse voltage generator;

FIG. 7 is a block diagram illustrating a construction of a frequency detector circuit;

FIG. 8 is a block diagram illustrating a construction of a synchronization detector applied to the frequency detector circuit;

FIG. 9 is a block diagram illustrating a construction of a linear phase detector circuit; and

FIG. 10 is a view illustrating a case where a phase difference is detected by the linear phase detector.

DETAILED DESCRIPTION OF THE INVENTION

Exemplary embodiments of the present invention will now be described in detail with reference to the accompanying drawings.

FIG. 1 is a block diagram illustrating a construction of a transceiver according to an embodiment of the present invention. The transceiver includes a transmitter 100 for receiving a parallel signal and transmitting the parallel signal as a serial signal and a receiver 200 for receiving the corresponding serial signal. According to the illustrated embodiment, the parallel data to be transmitted is 24-bit parallel data and used for a control signal interface for controlling a liquid crystal display unit.

The transmitter 100 receives the 24-bit parallel data and a reference clock signal and generates parallel data to be generated as a serial signal according to a predetermined protocol through an encoder 20 of FIG. 1. According to the embodiment, the encoder 20 divides 24-bit data into two 12-bit data, inserts a 2-bit direct-current (DC) balancing signal into the divided region, and inserts a start bit and a stop bit for informing of a start and a stop of data. Otherwise, as needed, the encoder 20 may generate a signal having a predetermined pattern.

In a case where the encoded parallel signal is converted into the serial signal, the serial signal may have a structure as illustrated in FIG. 2. Here, the 1 start bit and the 1 stop bit exist, the parallel data to be transmitted is divided into blocks (in FIG. 2, two 12-bit blocks) having the same size, and a pair of DC balancing signals DC_A and DC_B are inserted into the divided area. Specifically, as illustrated in FIG. 2, the converted 28-bit signal has a start bit for representing a value of 1 to inform of a start of data and a stop bit for representing a value of 0 to inform of an end of the data as a code inserted to apply frequency information to the data and has the DC
balancing bits in the middle of 24-bit practical data. Since the start bit and the stop bit have the values of 1 and 0, respectively, when the first bit output and the last bit output of the receiver always have values of 1 and 0, respectively, this has a function of determining that the receiver 200 finishes a recovery operation. In addition, the DC balancing bits DC_A and DC_B have a function of DC balancing to minimize data deterioration due to long distance transmission.

The data generated by the encoder 20 is transmitted as encoded serial transmission data through a serializer 60 and a converter 70 for converting logic signals such as a complementary metal–oxide–semiconductor (CMOS) and the like into low voltage differential signaling (LVDS) signals in serial communication channels. First, when power is applied to the transmitter 100 and the receiver 200, the converter 70 in the transmitter 100 outputs only a signal of 0 until a phase locked loop (PLL) in the transmitter 100 is in synchronization with a reference clock. Here, the receiver 200 starts an internal initializing operation and maintains the entire circuit in the receiver in a reset state. When the PLL in the transmitter 100 is in synchronization with the external reference clock, the transmitter 100 transmits data through an encoding operation, and the receiver 200 generates a clock signal according to a data rate of the transmitted data and controls a phase of the clock so that the transmitted data can be sampled at an optimal position.

In the receiver 200, a signal is acquired in a data block unit divided according to a clock converted by a signal converter 210 for converting the LVDS signal (the serial data) received through the serial channel back into the logic level signal and recovered by a clock recovery unit 230 for clock recovery and a data re-timer 220 and parallelized through the parallelizer 250. Thereafter, a start bit detector 270 detects a fine lock by using redundant bits, a decoder 260 acquires a 24-bit signal that has practical data, and data OUT<0> to OUT<23> having the originally transmitted parallel signal type, a reception clock Rx Clock, and a lock signal DE are output through an output buffer 280.

FIG. 3 is a block diagram illustrating the clock recovery unit 230 according to the embodiment of the present invention.

By using jitter characteristics inversely proportional to a signal speed, for example, when the transmitter transmits a signal by applying 28-bit data information to a clock signal of from 5 to 65 MHz, the receiver is designed to extract 14-bit data information from every clock signal of from 10 to 130 MHz, so that jitter of the clock
in the receiver can be reduced. Specifically, data is extracted according to a size of the data block divided during encoding such that a jitter reducing operation is performed in the receiver.

Operations of the illustrated circuit are classified into three steps including a coarse voltage generation operation, a PLL synchronization operation, and a data sorting operation. The coarse voltage generation operations is related to low jitter characteristics of a broadband transceiver and enables the PLL in the receiver to divide the entire frequency range into a plurality of (for example, three) frequency ranges instead of controlling a wide frequency range (for example, from 10 to 130 MHz) as a single fine adjusting range and control only a frequency band corresponding to a coarse voltage having predetermined bits (for example, 2 bits in a case where three or less ranges are used) as a fine adjusting voltage, so that a gain of a voltage controlled oscillator 232 can be minimized. As the gain of the voltage controlled oscillator 232 is higher, a frequency change is increased even though change in the adjusting voltage is small, and the frequency change is very sensitive to external noise, so that jitter characteristics are degraded. Therefore, the control method of selecting an operation frequency band using a coarse voltage has been conventionally used, however, in this method, an external coarse voltage corresponding to a frequency band has to be directly applied, so that an additional external control signal is necessary. However, according to the embodiment, the receiver 200 is improved to include a coarse code generator 231 for generating a coarse voltage corresponding to an operation speed, so that an additional control signal is not needed.

A coarse voltage operation of the coarse code generator 231 is performed as follows. When initial power is applied to the transceiver, the PLL in the transmitter is operated to be in synchronization with a reference clock signal. In this case, a serial channel output of the transmitter 100 is set to 0 until the PLL is synchronized. Accordingly, the receiver 200 can receive the input of 0 until the transmitter 100 can normally operate.

Here, the serializer 60 in the transmitter 100 performs sampling on the serial data signal by using a clock signal generated by vibrating the PLL in the receiver 100. Since the serial data signal is fixed to 0, the sampled 14-bit signal is also fixed to 0. When the PLL in the transmitter 100 finishes the synchronization operation, the data signal encoded as described above is transmitted as an output of the transmitter,
that is, serial data to the receiver 200. If the serial data has another value instead of 0, a sampler 245 in the receiver 200 has at least an output among the 14-bit output as 1.

FIG. 4 illustrates a construction of an initiation circuit unit 241 included in the clock recovery unit 230. The initiation circuit unit 241 is constructed with a simple circuit 310 including NOR gates, NAND gates, inverters, and the like to distinguish a case where all 14-bit parallelizer outputs are 0 from a case where at least one of the outputs is 1 and allow the receiver 200 to determine whether or not the transmitter 100 finishes the internal synchronization operation and provides a signal. When the determination circuit 310 including the NOR gates, the NAND gates, and the inverters in the initiation circuit unit 241 determines that at least one of the parallelizer outputs is 1, 10 D flip-flops 320 connected to an end of the determination circuit 310 generate a long pulse signal having 80 periods through a clock signal divided by 8. This pulse signal serves as a coarse enable signal that is the final output of a start circuit to reset the entire receiver 200 and starts a coarse voltage generation operation. Here, a circuit and method of generating the long pulse having 80 periods are used to obtain a predetermined delay for initial synchronization of the receiver 200, and a detailed construction thereof and a time of the delay may be modified.

The coarse code generation operation is performed by the coarse code generator 231 illustrated in FIG. 5. The coarse enable signal is connected to a MOS1 so as to enable a control voltage Vctrl to be connected to a supply voltage VDD or a ground voltage GND (GND in FIG. 5) while the coarse enable signal has the value of 1 and enable the voltage controlled oscillator 232 to oscillate at the maximum speed of the current coarse code. Since the entire circuit in the receiver 200 has finished a reset operation by the start circuit 241, the initial coarse code has a state of 00, and the voltage controlled oscillator 232 is in a state of oscillating at the maximum frequency in the lowest frequency range according to the current coarse code. The coarse code generator 231 receives a clock signal of the voltage controlled oscillator 232 oscillating at the maximum frequency according to the current coarse code and a serial data signal applied in a form of the reference clock signal and applies the received signals to delay stages including inverters and D flip-flop stages 443. The D flip-flop stages connected to the delay stages output 1 when a clock signal delayed by sampling an input clock signal at a rising edge of the
delayed clock signal has a phase prior to a falling edge of the input clock signal and output 0 when the delayed clock signal has a phase later than the falling edge so that the output value is changed from 1 to 0 at a portion where the falling edge of the input clock signal and the rising edge of the delayed clock have similar phases.

This has a function of determining the number of delay cells that a signal passes, the signal having a similar phase to the falling edge of the clock signal. An identifier (referred to as 1-0 identifier) 444 is a block formed by arraying circuits illustrated in FIG. 6. Since the circuit outputs a signal of 1 at a point where the input signal is changed from 1 to 0, a signal of 1 is generated at a stage corresponding to a position of the falling edge of the clock signal. If the identifier 444 outputs the signal of 1 at an N-th stage through the aforementioned operation, it can be seen that a period of the input signal has a value similar to 2N. Therefore, by detecting an order of a stage of the identifier 444 outputting the value of 1, a faster signal can be easily detected. When it is determined that the serial data signal is faster than the clock signal of the voltage controlled oscillator 232 by the means of the aforementioned operation, the coarse code is increased by 1 by logic units 445 and 441 including simple digital logics. As the coarse code is increased, by comparing the clock signal of the voltage controlled oscillator 232 oscillating at the one step higher range to the serial data signal, the coarse code is increased by 1, or an operation for maintaining the current value is repeated.

After the 80 periods of the reference clock signal, the value of the coarse enable signal is changed to 0. When the coarse enable signal has the value of 0, the MOS1 for connecting the control voltage Vctrl to the ground voltage GND to perform the coarse code generation operation is turned off, and the generated coarse code is maintained. Here, the clock recovery circuit has a type of a frequency locked loop including the voltage controlled oscillator 232, a frequency detector 233, a charge pump 236, and a loop filter (including a resistor and a capacitor). A frequency locked loop synchronization operation is an operation of synchronizing an output clock of the voltage controlled oscillator 232 with the serial data applied through the frequency locked loop. The frequency detector 233 illustrated in FIG. 7 has a function of decreasing a frequency of the voltage controlled oscillator 232 that oscillates at the maximum frequency in the current frequency range by the coarse code generation operation down to a range corresponding to the data rate. According to the embodiment, since the voltage controlled oscillator
oscillates at the speed twice the data rate, the clock signal VCO<0>/2 divided by 2 as illustrated in FIG. 7 is compared with a serial data signal delayed for a delay time of a 2 divider. The D flip-flops FF1 and FF2 in a frequency comparator 530 generate signals of 1 at the rising edges of the clock signal VCO<0>/2 and the delayed serial data signal, respectively, the flip-flop FF1 is reset when the signals of the two flip-flops are 1, and the flip-flop FF2 is reset at every falling edge of the serial data delayed by the operation of an FF2 reset unit. Since a period of the VCO<0>/2 includes 28-bit data, the delayed serial data signal has a larger number of rising edges than the VCO<0>/2. In this case, when all of the rising edges of the delayed serial data generate 1, an accurate frequency cannot be easily extracted. Therefore, the flip-flop FF1 receives the VDD signal as data of the flip-flop to generate 1 at every rising edge of the VCO<0>/2, and the flip-flop FF2 receives the VCO<0>/2 as data of the flip flop to generate 1 only at the rising edge of the delayed serial data generated after the rising edge of the VCO<0>/2 (a section where the VCO<0>/2 is 1), so that a phase difference with the rising edge of the delayed serial data that occurs first after the rising edge of the VCO<0>/2 can be detected. After a signal Freq_diff representing a frequency difference has a value of 1 at the rising edge of the VCO<0>/2, the value of the signal is changed to 0 as the flip-flop FF1 is reset at the rising edge of the delayed serial data that occurs next, so that the signal has a pulse width corresponding to the phase difference between the VCO<0>/2 and the delayed serial data, and this signal is transmitted to the charge pump 236 to decrease the frequency until a signal PD_Enable representing frequency synchronization occurs. A time delay between the rising edge of the VCO<0>/2 and the rising edge of the delayed serial data signal is continuously in a predetermined range (a lock range designated by a synchronization detector), the synchronization detector generates a lock signal Freq_lock.

The synchronization detector 540 illustrated in FIG. 8 receives the serial data and the output clock of the voltage controlled oscillator 232 during the frequency locked loop synchronization operation, and when a phase difference between the two signals is smaller than a delay time of a buffer cell of an input terminal of the D flip-flop, the synchronization detector 540 determines that the two signals are in synchronization with each other and outputs a signal lock0 as 1. A counter connected to the signal lock0 has a function of outputting a final output lock<n> as 1 only when the lock signal is output as 1 for 8 or more periods (according to the
embodiment) in preparation for errors of the synchronization detector 540.

The delayed serial data includes arbitrary signals excluding the start/stop bits and the DC balancing bits \( DC_A / DC_B \), so that a lock condition of the synchronization detector 540 cannot be satisfied until the rising edge of the delayed serial data that occurs right after the VCO<0>/2 becomes the rising edge of the start bit. When the synchronization detector 540 does not generate the lock signal, the frequency detector 233 generates a signal Freq_DN for continuously decreasing the frequency, and as a result, in the final lock state, the rising edge of the VCO<0>/2 and the rising edge of the start bit of the delayed serial data exist in the lock range. A synchronization detector 1 has a function of detecting a time delay between the rising edges of the VCO<0>/2 and the start bit of the delayed serial data as described above, and a synchronization detector 2 has a function of detecting a time delay between the falling edges of a VCO<7>b/2 and the DC_A bit that is the fourteenth bit.

When the rate of the serial data and the frequency of the clock are in synchronization with each other and phases of the rising edges of the VCO<0>/2 and the start bit are in synchronization with each other, due to a data structure according to the embodiment, the falling edges of the VCO<7>/2 and the DC_A bit have to be in synchronization with each other. Therefore, for more accurate synchronization detection, the two synchronization detectors are used, and the number of the synchronization detectors may be changed according to designing. Here, when both of the two synchronization detectors generate the lock signals, a PD_Enable signal is generated, and at the same time, an input of a NAND gate having an output as a signal Freq_DN becomes 0 and the signal Freq_DN is maintained as 0.

When the synchronization signal PD_Enable of the synchronization detector 233 outputs 1, the receiver 200 stops the frequency locked loop synchronization operation and changes an output of a multiple phase selector 234 to form a new loop. The new loop includes the voltage controlled oscillator 232, a linear phase detector 239, and the charge pump CP 236, and a clock of the voltage controlled oscillator 232 generated through the loop and a sorted serial data signal are connected to the parallelizer 250.

The new loop is a loop for a data sorting operation and has a function of arranging the rising edge of the clock of the voltage controlled oscillator 232 to be
disposed at the center of each bit of the practical data signal. A conventional high speed transceiver mainly uses a bang-bang phase locked loop to form the clock recovery circuit. However, there are problems in that a recovered clock signal has relatively higher jitter and this increases a bit error ratio (BER). Therefore, according to the embodiment, the linear phase detector 239 is designed to be used to decrease the jitter and the BER.

The voltage controlled oscillator 232 may provide an oscillating output for a 14-bit data block (12-bit data and redundant 2 bits) by using 14 stages, that is, the voltage controlled oscillator having 14 different phases. If an input signal is divided by data blocks having different sizes, different stages are needed.

FIGS. 9 and 10 are views illustrating an example circuit diagram and operation waveforms of the circuit of the linear phase detector 239. The linear phase detector 239 includes a serial data rising edge detector 510. The serial data rising edge detector 510 receives two multiple phase clock signals VCO<13> and VCO<0> and serial data signals, and when output signals sam<13> and sam<0> obtained by sampling the serial data using the clock signals have values of 0 and 1, respectively, in other words, when the serial data signal has a rising edge, the serial data rising edge detector 510 outputs a pulse signal corresponding to a phase difference between the clock signal and the serial data signal. In this case, operations of the serial data rising edge detector 510 for determining whether or not the rising edge of the serial data exists have to be finished before signals PD_UP and PD_DN are generated. However, the signal sam<0> that is a result of sampling the serial data by using the VCO<0> signal that is generated after a data bit from the VCO<13> is generated after the PD_DN is generated by the VCO<13>.

In order to solve the aforementioned problems, the three input signals VCO<13>, VCO<0>, and the serial data are connected to the delay cell 521 having a delay more than a data bit, and the detection of the signals PD_DN and PD_UP is performed by using signals CK1D, CK2D, and DD obtained by delaying the signals. For example, in a case where 13-th and 0-th multiple phase clock signals are used from among 14 multiple phases, if the serial data signal sampled by the 13-th clock signal and the serial data signal sampled by the 0-th clock signal have values of 0 and 1, respectively, that is, if the rising edge of the serial data signal is between the 13-th and 0-th clock signals as illustrated in FIG. 10, the linear phase detector 239 represents a phase difference between the rising edge of the delayed 13-th clock
signal CK1D and the rising edge of the delayed serial data DD as the PD_DN signal, and represents a phase difference between the rising edge of the DD and the rising edge of the delayed 0-th clock signal CK2D as the PD_UP signal. Since the signals PD_DN and PD_UP are represented as pulses proportional to the phase difference between the multiple phase clock signal and the serial data signal, in a case where the signal PD_DN has a pulse wider than the signal PD_UP, a signal is transmitted to the charge pump 236 to allow the multiple clock signal to be slower. In the opposite case, a signal is transmitted to the charge pump 236 to allow the multiple clock signals to be faster. In a case where the signals PD_DN and PD_UP have the same width, it means that the 0-th clock is disposed at the center of the serial data. Therefore, in this case, output current of the charge pump 236 is maintained.

Since the signals PD_DN and PD_UP are signals input to the charge pump, in a case where a phase difference between the two signals exists, current errors may occur in the charge pump and phase locked error may occur. Therefore, the signal PD_DN that is output first is output to be delayed for a delay of a stage of a delay cell, that is, a phase that is half the phase difference between the multiple phase clock signals so as to minimize locked phase errors.

After the data sorting using the linear phase detector 239, the first output and the last output of the parallelizer 250 are fixed to 1 and 0 representing the start bit and the stop bit, respectively. When the start bit detector 270 that is a circuit having a simple logic for detecting whether or not the first output and the last output are output as 1 and 0, respectively, checks that the start bit and the stop bit are fixed to 1 and 0, respectively, the start bit detector 270 provides an enabling signal for fixing the DE signal that is the final lock signal to 1 and enabling the output of the parallelizer 250 to be used. Finally, the receiver 200 outputs a practical 24-bit output excluding the start bit, the stop bit, DCA, and DCB from the 28-bit output signal and the clock signal synchronized with the data rate.

The serial transceiver and the communication method according to the embodiment of the present invention apply the clock recovery unit including the coarse code generator, the frequency detector, and the linear phase detector to the receiver. Therefore, while the embedded clock method of applying clock information to data is used, problems such as skew between the reference clock and data that may occur during data transmission and jitter of the recovered clock can be solved.
The serial transceiver and the communication method used by the serial transceiver according to the embodiment of the present invention do not transmit the reference clock while transmits data. Therefore, skew between the data and the reference clock can be removed, and the number of transmission channels can be minimized, so that hardware costs can be reduced.

The serial transceiver and the communication method used by the serial transceiver according to the embodiment of the present invention can control speed of the serial communications using a single channel without additional external operations and significantly reduce jitter of the recovered clock signal by applying the linear phase detection method, thereby increasing the maximum communication speed and stability.

The serial transceiver and the communication method used by the serial transceiver according to the embodiment of the present invention do not need an initial synchronization operation between the transmitter and the receiver although the embedded clock method is used, so that operations and the construction of the transceiver are simple. In addition, clock recovery reliability of the receiver is high, so that the construction for connecting the transmitter and the receiver can be simplified with low costs.
What is claimed is:

1. A serial transceiver comprising:
   a transmitter which receives parallel data to be transmitted, including
   an encoder to encode the received parallel data as transmission data
   including DC (direct current) balancing information,
   an internal PPL (phase locked loop), and
   a serial transmission unit for performing serial transmission on data encoded
   according to a communication clock of the internal PLL operating based on an
   externally provided clock; and
   a receiver which includes
   a clock recovery unit having an internal voltage controlled oscillator and
   including a frequency detector and a linear phase detector for receiving the encoded
   data from the transmitter and performing sequential synchronization by using the
   received encoded data and an output of the internal voltage controlled oscillator,
   a parallelizer for converting the received serial data into parallel data by using
   clocks of a plurality of stages output from the clock recovery unit, a start bit detector
   for detecting a start bit by comparing data in the output of the parallelizer through a
   logic circuit, and
   a decoder for decoding and outputting the output of the parallelizer.

2. The serial transceiver of claim 1, wherein the transmitter includes an
   encoding unit which receives a plurality of parallel data signals to divide a
   corresponding parallel data signal into two or more units, inserts information for DC
   balancing into the divided position, and inserts start information and end information
   into start and end portions of the entire data.

3. The serial transceiver of claim 1, wherein the clock recovery unit of the
   receiver includes an internal coarse code generator and a charge pump, and
   wherein:
   the voltage controlled oscillator includes a plurality of states in which a
   frequency range is determined by a coarse code;
   the internal coarse code generator receives an output of the voltage controlled
   oscillator and the received serial data as inputs to provide the coarse code for
controlling the voltage controlled oscillator to the voltage controlled oscillator;
the frequency detector receives a voltage controlled oscillator output in the
frequency range determined by the output of the coarse code generator and the
received parallel data as inputs to output a signal for controlling a voltage applied to
the voltage controlled oscillator for frequency synchronization;
the linear phase detector receives the voltage controlled oscillator output and
the received parallel data as inputs in a case where the frequency synchronization is
performed by the frequency detector to output a signal for controlling the voltage
applied to the voltage controlled oscillator for phase synchronization; and
the charge pump selectively receives the output from the frequency detector
and the linear phase detector to control the voltage applied to the voltage controlled
oscillator.

4. The serial transceiver of claim 3, wherein the clock recovery unit further
includes:
a sampler for sampling the received serial data by using the output of the
voltage controlled oscillator; and
an initiation circuit unit for generating and providing a coarse enable signal for
determining whether or not the coarse code generator is to operate according to the
output of the sampler to the coarse code generator.

5. The serial transceiver of claim 4,
wherein the charge pump further includes a switch for selectively connecting
the voltage applied to the voltage controlled oscillator to a maximum voltage or a
minimum voltage to allow the voltage controlled oscillator to operate at a maximum
frequency, and
wherein the coarse enable signal is used as a control signal for operating the
switch.

6. The serial transceiver of claim 3, wherein the voltage controlled
oscillator of the plurality of the stages has a stage having the same size as a value
obtained by adding bits of a data block divided by the inserted DC balancing
information from among the serial signals provided for a signal external clock and the
half the inserted DC balancing information and a start or a stop bit.
7. A serial transmitter connected to a serial receiver to transmit parallel data as serial data, comprising:
   an encoding unit receiving the parallel data to be transmitted and encoding the received parallel data as transmission data including DC balancing information and start and end information;
   a serializer using an output clock of an internal PLL according to an externally provided clock as a communication clock to provide synchronization signals in a serial communication manner; and
   a serial transmission unit for performing serial transmission on data encoded according to the communication clock.

8. A serial receiver which is connected to a transmitter that encodes and transmits parallel data as serial data, in order to receive the serial data, recovers a clock included in the serial data, and converts and decodes the serial data into parallel data to output the received clock and the decoded parallel data, the serial receiver comprising:
   a clock recovery unit including a frequency detector and a linear phase detector for receiving the serial data from the transmitter and performing sequential synchronization by using the received serial data and an output of an internal voltage controlled oscillator;
   a parallelizer for converting the received serial data into parallel data by using clocks of a plurality of stages output from the clock recovery unit;
   a start bit detector for detecting a start bit by comparing data in the output of the parallelizer through a logic circuit; and
   a decoder for decoding and outputting the output of the parallelizer.

9. The serial receiver of claim 8, wherein the clock recovery unit includes:
   a voltage controlled oscillator of a plurality of stages in which a frequency range is determined by a coarse code;
   an internal coarse code generator receiving an output of the voltage controlled oscillator and the received serial data as inputs to provide the coarse code for controlling the voltage controlled oscillator to the voltage controlled oscillator;
   a frequency detector receiving a voltage controlled oscillator output in the
frequency range determined by the output of the coarse code generator and the received parallel data as inputs to output a signal for controlling a voltage applied to the voltage controlled oscillator for frequency synchronization;

a linear phase detector receiving the voltage controlled oscillator output and the received parallel data as inputs in a case where the frequency synchronization is performed by the frequency detector to output a signal for controlling the voltage applied to the voltage controlled oscillator for phase synchronization; and

a charge pump selectively receiving the output from the frequency detector and the linear phase detector to control the voltage applied to the voltage controlled oscillator.

10. A serial receiver which is connected to a transmitter that encodes and transmits parallel data as serial data, in order to receive the serial data, recovers a clock included in the serial data, converts and decodes the serial data into parallel data to output the received clock and the decoded parallel data, and comprises a clock recovery unit including a frequency detector for recovering a clock, wherein the frequency detector comprises:

a divider dividing signals among outputs of a voltage controlled oscillator of the plurality of stages according to a rate of the received data;

a serial data delay for delaying the serial data delayed by a delay time of the divider for dividing the output of the voltage controlled oscillator;

one or more synchronization detectors comparing an output of the delay to one of the outputs of the divider to detect synchronization and providing a result of the comparison as a synchronization signal; and

a frequency controller which outputs a frequency falling signal by using a periodic pulse signal due to one of the outputs of the divider and the output of the delay, in a case where a frequency difference occurs, and blocks the frequency falling signal in a case where the frequency is synchronized by the synchronization signal of the synchronization detector and the output of the delay.

11. A serial receiver which is connected to a transmitter that encodes and transmits parallel data as serial data, in order to receive the serial data, recovers a clock included in the serial data, converts and decodes the serial data into parallel data to output the received clock and the decoded parallel data, and comprises a
clock recovery unit including a linear phase detector for recovering a clock, wherein the linear phase detector comprises:

a delay for delaying initial stage and final stage output signals from among the outputs of the voltage controlled oscillator of the plurality of the stages and the received data;

a rising edge detector for detecting a rising edge of the serial data by sampling the serial received data according to the initial stage and the final stage output signals; and

a phase detector for receiving the received data delayed by the delay, an output of the rising edge detector, the initial stage and the final stage output of the voltage controlled oscillator delayed by the delay as inputs, and based on the rising edge of the delayed serial data, outputting a pulse between rising edges of the delayed final stage output and the initial stage output of the voltage controlled oscillator as a signal for adjusting a voltage to be applied to the voltage controlled oscillator.

12. A communication method used in a serial transceiver comprising:

a transmitting step of, in a case where a transmitter and a receiver are connected through a serial channel, dividing practical data into a plurality of uniform sizes to insert DC balancing information into every divided area, and inserting start and end information into the entire data to encode and perform serial transmission on practical transmission data having redundant information through the serial channel, by the transmitter; and

a receiving step of generating a clock signal corresponding to a data transmission rate through a frequency detection manner by using the practical transmission data received through the serial channel, recovering a clock by controlling a phase of the clock synchronized in a linear phase detection manner, acquiring data from the practical transmission data serially received, and decoding and outputting the data as original data without the redundant information, by the receiver.

13. The communication method of claim 12, wherein the receiving step comprises:

a frequency band determining step of sampling the practical transmission data
by using the output of the voltage controlled oscillator of the plurality of stages, receiving the sampled signal, the practical transmission data, and the output of the voltage controlled oscillator, and determining an operation frequency band of the voltage controlled oscillator of the plurality of stages;

a frequency synchronization step of detecting a frequency difference by using the received output of the voltage controlled oscillator of the plurality of stages operating at the maximum speed of a frequency band selected by the generated coarse code and the practical transmission data and decreasing a frequency of the voltage controlled oscillator of the plurality of stages until the frequency synchronization is completed; and

a phase synchronization step of adjusting a control voltage to be applied to the voltage controlled oscillator of the plurality of stages in order to synchronize the output of the voltage controlled oscillator of the plurality of stages with a linear phase of the practical transmission data, after the frequency synchronization step.

14. The communication method of claim 13, wherein the receiving step includes a data outputting step of parallelizing and outputting the practical transmission data according to the clock signal synchronized in the phase synchronization step and outputting a data enable signal representing usability of an output signal by detecting a start bit included in the synchronized signal.
Abstract of the Disclosure

A high speed transceiver without using an external clock signal and a communication method used by the high speed transceiver which applies a clock recovery circuit including a coarse code generator, a frequency detector, and a linear phase detector to the receiver so as to solve problems such as skew between a reference clock and data that may occur during data transmission and jitter of a recovered clock while an embedded clock method of applying clock information to data is used.
FIG. 1

FIG. 2

STOP BIT    START BIT           DC_A  DC_B           STOP BIT    START BIT
  0   1 | PRACTICAL DATA (A PORTION)  1   0 | PRACTICAL DATA (A PORTION)  0   1
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**New Applications Under 35 U.S.C. 111**
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Chulwoo KIM et al.

Application No.: 12/178,347
Filed: July 23, 2008
For: SERIAL TRANSCIEVER AND COMMUNICATION METHOD USED BY THE SERIAL TRANSCIEVER

Confirmation No.: 6126
Art Unit: N/A
Examiner: Not Yet Assigned

CLAIM FOR PRIORITY AND SUBMISSION OF DOCUMENTS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicants hereby claim priority under 35 U.S.C. 119 based on the following prior foreign application filed in the following foreign country on the date indicated:

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<td>Korea, Republic of</td>
<td>10-2007-0073815</td>
<td>July 24, 2007</td>
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</table>

In support of this claim, a certified copy of the said original foreign application is filed herewith.

Dated: July 23, 2008

Respectfully submitted,

By
Steven M. Rabin
Registration No.: 29,102
RABIN & BERDO, PC
Correspondence Customer Number: 23995
This is to certify that the following application annexed hereto is a true copy from the records of the Korean Intellectual Property Office.

출원번호: 10-2007-0073815
Application Number

출원년월일: 2007년 07월 24일
Filing Date

출원인: 고려대학교 산학협력단
Applicant(s)

Korea University Industrial & Academic Collaboration Foundation

2008년 07월 03일

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출원번호: 10-2007-0073815

【서지사항】

【서류명】 특허출원서
【참조번호】 0002
【출원구분】 특허출원
【출원인】
【명칭】 고려대학교 산학협력단
【출원인코드】 2-2004-017068-0
【대리인】
【성명】 전종학
【대리인코드】 9-2002-000417-2
【포괄위임등록번호】 2006-062980-9
【발명의 국문명칭】 직렬 송수신 장치 및 그 통신 방법
【발명의 영문명칭】 SERIAL TRANSMITTER AND RECEIVER, AND COMMUNICATION METHOD THEREOF

【발명자】

【성명】 김철우
【성명의 영문표기】 Kim, Chul Woo
【주민등록번호】 690919-1XXXXXX
【우편번호】 136-110
【주소】 서울 성북구 길음동 1283 길음뉴타운 605-1301호
【국적】 KR

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【성명】 정인화
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【주민등록번호】 811130-1XXXXXX
【우편번호】 136-071
출원번호: 10-2007-0073815

【주소】 서울 성북구 안양동 5가 103-34번지 201호
【국적】 KR
【심사청구】 청구
위와 같이 특허청장에게 제출합니다.

대리인

전중학  (인)

【수수료】
【출원료】 0  면  38,000 원
【가산출원료】 39  면  0 원
【우선권주정료】 0  건  0 원
【심사청구료】 20  항  749,000 원
【합계】  787,000 원
【감면사유】 학교
【감면후 수수료】 393,500 원
【첨부서류】 1. 고등교육법 제2조에 의한 학교임을 증명하는 서류 _1통
본 발명은 외부 클릭 신호를 사용하지 않는 고속 송수신 장치 및 그 통신 방법에 관한 것으로, 이를 위하여 적절 송수신 장치가 초기 동기화 과정을 거치도록 함과 아울러 내장 커스 코드 생성부와 선행 위상 검출부를 포함하는 클릭 복원부를 수신기에 적용함으로써, 데이터에 클릭 정보를 인가하는 임베디드 클릭 방식을 이용하면서도 데이터가 전달되는 동안 발생하는 기준 클릭과 데이터 사이의 스큐 문제 및 복원 클릭의 저터 문제를 제거할 수 있는 뛰어난 효과가 있다.

【대표도】

도 1

【설명서】

커스 코드, 송수신, 적절 통신, 동기화, 위상 동기, 선행 위상 검출기
출원번호: 10-2007-0073815

【명세서】

【발명의 명칭】
직렬 송수신 장치 및 그 통신 방법{SERIAL TRANSMITTER AND RECEIVER, AND COMMUNICATION METHOD THEREOF}

【발명의 상세한 설명】

【기술분야】
본 발명은 직렬 송수신 장치에 관한 것으로, 특히 외부 클럭 신호를 사용하지 않는 고속 송수신 장치 및 그 통신 방법에 관한 것이다.

【배경기술】

다양한 통신 방식의 급속한 확산과 발전은 멀티미디어에 대한 사용자 수요를 높이게되었으며, 그에 따라 더 높은 속도로 더 많은 데이터를 더 안정적으로 전송함과 이울리, 이러한 전송에 필요한 하드웨어 구성을 최소화하기 위한 연구가 활발해지고 있다.

일반적으로 데이터의 전송 속도를 높이기 위해서는 채널의 수를 늘려 여러 데이터를 동시에 전송하는 병렬 전송 방식과 하나의 채널을 통해 빠른 속도로 데이터를 전송하는 직렬 전송 방식 중 하나를 선택하여 그 기능을 극대화하는 것이 일반적이다. 여기서, 병렬 전송 방식은 경우 여러 전송 채널들 사이에 서로 다른 채널을 통해 전송되는 데이터 사이의 시간차를 의미하는 데이터 스케일을 존재할 수 있고, 채널의 수가 늘어날수록 하드웨어적인 비용이 많이 들기 때문에 최근에는 직렬
데이터 전송 방식이 고속 송수신기의 표준으로 채택되어 널리 사용되고 있으며, 이
러한 고속 직렬통신을 병렬로 구성하고자 하는 연구도 진행되고 있다. 이러한 직렬
데이터 송수신에서는 데이터가 오고 가는 속도가 매우 높기 때문에 잡음과 채널의
대역폭에 의한 데이터의 불확실성이 증가하는 문제가 있다. 이러한 데이터 전송의
불확실성을 줄이기 위해서 수신기는 입력 데이터를 샘플링하기 위해 가능한 지터
(gitter)가 작도록 클릭을 복원해야 하며, 비트 에러율이 최소가 되도록 복원된 클
릭과 입력 데이터의 위상 관계를 최적의 상태로 유지해야 한다. 따라서, 고속 직렬
통신에 있어 송신기로부터 클릭과 데이터를 입력받아 수신기가 입력 데이터를 샘플
링하기 위한 최적의 상태로 클릭 신호를 재조정하는 클릭 복원회로의 역할은 막중
하다 할 수 있다.

일반적인 고속 데이터 송수신기는 송신기에서 수신기로 데이터를 전송하기
위해 고속 송수신 데이터에 대한 동기 기준을 제공하기 위한 기준 클릭 신호를 함
께 전송하는 형태로 이루어져 있다. 하지만 이러한 방식은 수 미터에 이르는 긴 거
리까지 전송하는 경우 데이터와 기준 클릭 사이의 스케일문제로 인하여 수신기가 데
이터를 복원하는데 문제가 발생할 수 있다. 또한, 기준의 송수신기는 전송속도를
변화시키기 위해서 전송속도에 맞도록 수신기의 기준 클릭신호를 바꾸어 주거나,
수신기의 동작속도를 조절하기 위해 디지털 코드를 바꾸어 주어야하는 등의 번거로
움이 있다.

미국 공개특허 US 6,680,970호 "다중 속도 임베디드 클릭 직렬 수신기를 위
한 데이터를 검출에 적용되는 통계적 방법과 시스템(Statistical methods and

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출원번호: 10-2007-0073815

systems for data rate detection for multi-speed embedded clock serial receivers"에서는 이러한 문제를 해결하기 위해서 데이터의 경계(edge)를 검출하는 방식을 사용하는 방식을 제안하였으나, 이 경우 데이터의 경계 검출의 한계로 인하여 선형 위상 검출기를 사용하는 것에 비해 복잡되는 클럭 신호의 지터가 크기 때문에 속도에 제한이 발생하게 되며, 오류 가능성도 높아지게 된다.

다른 방법으로 미국 공개특허 US 5,838,749호 "디지털 데이터 신호로부터 임베디드 클럭을 추출하는 방법 및 장치(Method and apparatus for extracting an embedded clock from a digital data signal)"에서는 상기 문제의 해결을 위해서 클럭 복원회로 내부에 클럭 공급기를 탐재하는 방식을 사용하고 있으나, 이러한 클럭 공급기의 부가적인 탐재로 인한 면적 및 비용 증가와 전력 소모 증가 등의 문제점이 발생한다.

【발명의 내용】

【해결하고자 하는 과제】

본 발명 실험의 목적은 송신기에서 수신기로 데이터를 전달할 때, 초기 동기화 과정을 거치도록 함과 아울러 내장 커스 코드 생성부와 선형 위상 검출부를 포함하는 클럭 복원부를 수신기에 적용함으로써, 데이터에 클럭 정보를 인가하는 임베디드 클럭 방식을 이용하면서도 데이터가 전달되는 동안 발생하는 기존 클럭과 데이터 사이의 스케 문제 및 복원 클럭의 지터 문제를 제거할 수 있도록 한 직접 송수신 장치 및 그 통신 방법을 제공하는 것이다.
본 발명 실시예들의 다른 목적은 데이터를 전송시 기존 클릭을 함께 전송하지 않도록 하여 데이터와 기존 클릭 사이의 스を与え를 근본적으로 제거함과 아울러, 전송 채널의 수를 최소화하여 하드웨어적인 비용을 줄일 수 있도록 한 직렬 송수신 장치 및 그 통신 방법을 제공하는 것이다.

본 발명 실시예들의 또 다른 목적은 데이터를 전송시 기준 클릭을 함께 전송하지 않도록 하면서도 별도의 외부 송장을 없이 속도를 조절할 수 있으며, 선행 위상 검출 방식을 적용하여 복원되는 클릭 신호의 지에서 크게 감소시킬 수 있도록 한 직렬 송수신 장치 및 그 통신 방법을 제공하는 것이다.

본 발명 실시예들의 또 다른 목적은 수신기에 별도의 클릭 공급기가 없고, 주가적인 회로 없이도 클릭 신호를 복원할 수 있도록 한 직렬 송수신 장치 및 그 통신 방법을 제공하는 것이다.

【과제 해결 수단】

상기와 같은 목적을 달성하기 위하여, 본 발명의 실시예에 따른 직렬 송수신 장치는 전송할 병렬 데이터를 입력받아 직렬 평형 정보를 포함하는 송신 데이터로 인코딩함과 아울러 하기의 수신부로부터 제공되는 락 신호와 외부 제공 클릭 및 내부 위상 고정 루프의 통신 클릭을 근거로 복수 단계로 이루어진 초기 동기화를 위한 동기화 신호들을 직렬 통신 방식으로 출력하는 조정신호 생성부와, 상기 조정신호 생성부가 제공하는 초기 동기화 신호에 따른 동기 신호를 제공하거나 상
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기 통신 클릭에 따라 인코딩된 데이터를 직접 전송하는 직접 전송 수단을 포함하는 송신부와, 상기 송신부의 조정신호 생성부를 통한 동기 신호가 수신되면 위상 주파수 검출 방식을 통해 전압 제어 발진기를 제어하면서 동기화를 수행한 후 동기화되면 락 신호를 상기 송신부에 제공하고, 상기 송신부로부터 상기 인코딩된 데이터가 수신되면 해당 데이터와 상기 전압 제어 발진기 출력을 선행 위상 검출기를 통해 파악하여 클릭을 복원하는 클릭 복원부를 포함하며, 이를 통해 동기화 및 데이터 수신을 실시한 후 수신된 데이터의 디코딩을 통해 전송대상의 병렬 데이터를 출력하는 수신부를 포함하여 이루어진다.

상기 송신부는 복수의 병렬 데이터 신호를 입력받아 해당 병렬 데이터 신호를 두개 이상의 단위로 분할한 후, 상기 분할 위치에 적류 평형을 위한 정보를 삽입하고, 전체 데이터의 시작과 종료 부분에 각각 시작 정보와 종료 정보를 삽입하는 인코딩 수단을 포함할 수 있다.

상기 조정신호 생성부는 상기 수신부로부터 락 신호를 수신하지 못하는 경우 상기 수신부가 데이터 속도에 동기된 클릭 신호를 생성할 때까지 동기화 신호를 제공하며, 상기 수신부로부터 락 신호를 수신할 경우 상기 동기화 신호 대신 실제 전송할 인코딩 데이터 형태의 기 설정된 패턴을 가지는 시험 데이터를 기 설정된 시간동안 전송한다.

상기 수신부의 클릭 복원부는 상기 복수 스테이지와 가지는 전압제어 발진기와, 상기 전압제어 발진기의 출력과 수신되는 직렬 데이터를 근거로 상기 전압제어 발진기를 제어하는 내장 커스 코드(Coarse Code) 생성부와, 상기 조정신호 생성부
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통합된 메시지는 동기 신호를 근거로 상기 전압제어 발전기를 미세 조정하는 제 1동기화 수단과, 상기 수신 직렬 데이터와 상기 전압제어 발전기 출력을 입력으로 하는 선형 위상 검출기를 통해 얻어지는 정보로 상기 전압제어 발전기를 미세 조정하는 제 2동기화 수단과, 상기 제 1 또는 제 2동기화 수단에 의한 동기 여부를 검출하여 락 신호를 상기 통신부에 제공하는 락 검출 수단을 포함한다.

상기 내장 커스 코드 생성부는 상기 복수 스테이지의 전압 제어 발전기 출력을 지연시키는 복수의 제 1지연단과, 상기 수신되는 직렬 데이터를 지연시키는 복수의 제 2지연단과, 상기 제 1지연단의 출력에 따른 전압 제어 발전기의 출력 하강 모서리 위치를 검출하여 전압 제어 발전기의 주기를 파악하는 석별기와, 상기 석별기의 출력과 제 2지연단의 출력에 따른 수신 직렬 데이터의 위상을 비교하여 상기 전압 제어 발전기 출력과 수신 직렬 데이터의 신호를 파악하여 상기 전압 제어 발전기의 출력을 제어하는 신호를 출력하는 논리부를 포함하여 이루어진다.

또한, 본 발명 다른 실시예에 따른 직렬 송신 장치는 동기화에 따른 락 신호를 제공하는 직렬 수신 장치와 연결되어 병렬 데이터를 직렬 데이터로 전송하는 직렬 수신 장치에 관한 것으로, 전송할 병렬 데이터를 입력받아 직렬 통신 정보와 시작 및 종료 정보를 포함하는 송신 데이터로 인코딩하는 인코딩부와, 상기 직렬 수신 장치로부터 제공되는 락 신호와 외부 제공 클럭 및 내부 위상 고정 루프의 통신 클럭을 근거로 동기화 신호들을 직렬 통신 방식으로 제공하는 조정신호 생성부와, 상기 조정신호 생성부가 제공하는 동기화 신호에 따른 동기 신호를 제공하거나 상기 통신 클럭에 따라 인코딩된 데이터 중 하나를 선택하여 직렬 전송하는 직렬 전
본 발명 다른 실시예에 따른 직렬 수신 장치는 연결시 직렬 통신 방식으로 순차적인 초기 동기화 신호를 제공하고, 동기화에 끝나는 경우 실제 데이터를 전송하는 송신기와 연결되는 직렬 수신 장치에 관한 것으로, 상기 송신기가 제공하는 순차적인 동기화 신호로 직렬 통신 방식으로 수신하여 위상 주파수 검출 방식을 통해 통신용 동기를 맞추어 동기화가 끝났음을 알리는 띠 신호를 상기 송신기에 제공하고, 상기 송신기로부터 제공되는 상기 실제 데이터를 선행 위상 검출기를 통해 파악하여 클럭을 복원하는 클럭 복원부와, 상기 클럭 복원부를 통해 복원되는 클럭에 맞추어 실제 수신되는 데이터로부터 실제 데이터를 획득하며, 상기 획득된 실제 데이터를 디코딩하여 전송대상의 병렬 데이터를 출력하는 수신 신호 처리 수단을 포함할 수 있다.

본 발명 다른 실시예에 따른 직렬 송수신 장치를 이용한 통신 방법은, 송신기와 수신기가 직렬 채널을 통해 연결되는 경우 상기 송신기가 수신기에 동기화 클럭 정보를 직렬 채널을 통해 전송하는 초기 동기화 단계와, 상기 초기 동기화 단계를 통해 수신기가 동기되면 동기 완료 정보를 상기 송신기에 제공하고, 그에 따라 상기 송신기가 가 정의된 형태의 시험 데이터를 상기 직렬 채널을 통해 일정 시간 전송하는 전송 준비 단계와, 상기 송신기가 실제 데이터를 균일한 복수의 크기로 구분하여 직렬 평형 정보를 구분 영역마다 포함시키고, 전체 데이터에 시작 및 종료 정보를 포함시켜 양이 정보를 가지는 실제 전송 데이터로 인코딩하여 상기 직렬 채널을 통해 직렬 전송하는 단계와, 상기 수신기는 상기 직렬 채널을 통해 수신되
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본 발명의 실시예에 따른 직렬 송수신 장치 및 그 통신 방법은 초기 동기화 과정을 거쳐도록 함과 아울러 내장 커스 코드 생성부와 선행 위상 검출부를 포함하는 클릭 복원부를 수신기에 적용함으로써, 데이터에 클릭 정보를 인가하는 임베디드 클릭 방식을 이용하면서도 데이터가 전달되는 동안 발생하는 기존 클릭과 데이터 사이의 스큐 문제 및 복원 클릭의 지터 문제가 제거할 수 있는 뛰어난 효과가 있다.

본 발명의 실시예에 따른 직렬 송수신 장치 및 그 통신 방법은 데이터를 전송할 경우 기존 클릭을 함께 전송하지 않도록 하여 데이터와 기존 클릭 사이의 스 큐문제를 근본적으로 제거함과 아울러, 전송 채널의 수를 최소화하여 하드웨어적인 비용을 줄일 수 있는 효과가 있다.

본 발명의 실시예에 따른 직렬 송수신 장치 및 그 통신 방법은 단일 채널을 이용하는 직렬 통신에서 별도의 외부 동작 없이 속도를 조절할 수 있으며, 선행 위상 검출 방식을 적용하여 복원되는 클릭 신호의 지터를 크게 감소시켜 최대 통신

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속도 및 안정성을 높일 수 있는 효과가 있다.

【발명의 실시를 위한 구체적인 내용】

상기한 바와 같은 본 발명을 점부된 도면들과 실시예들을 통해 상세히 설명하도록 한다.

도 1은 본 발명 일 실시예에 따른 송수신기 구조를 보인 블록도로서, 도시한 바와 같이 병렬 신호를 수신하여 직렬 신호로 송신하는 송신부(100)와 해당 직렬 신호를 수신하는 수신부(200)로 이루어진다. 도시된 실시예에서, 전송할 병렬 데이터는 24비트로 예로 들어 설명하며, 이는 액정 디스플레이 수단을 제어하기 위한 제어 신호 인터페이스에 사용되는 경우이다.

상기 송신부(100)는 24비트의 병렬 데이터와 기준 클럭 신호를 입력받아 도 1의 인코더(Encoder)(20)를 통해 소정의 프로토콜에 따른 직렬 신호로 만들 병렬 데이터를 생성한다. 상기 예에서는 24비트 데이터를 12비트씩 구분한 후 구분 영역에 2비트의 직류 평형 신호를 삽입하고, 전체 데이터의 시작과 끝을 알리기 위한 시작 비트와 정지 비트를 각각 삽입하도록 구성된 인코더(20)를 이용한다. 혹은 필요시 특정한 패턴의 신호를 생성할 수도 있도록 한다.

상기 인코딩된 신호는 직렬로 변환할 경우 도 2에 도시한 바와 같은 형태를 가질 수 있으며, 여기서 각각 1비트씩으로 구성되는 시작 비트와 정지 비트가 존재하며, 상기 전송할 병렬 데이터를 균일한 크기의 블록(도시된 경우에는 12비트 씩)
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2개 블록)으로 구분한 후 해당 구분에 삽입된 한양의 직류 평형 신호(DC₀, DC₀)가 포함되어 있음을 알 수 있다. 즉, 도시된 예에서, 변환된 28비트의 신호는 데이터에 주파수 정보를 인가하기 위해 삽입된 코드로서 데이터의 처음을 알리기 위해 항상 1의 값을 나타내는 시작(Start)비트와 데이터의 마지막을 알리기 위해 항상 0의 값을 나타내는 종료(Stop)비트를 가지고, 실제 데이터 24비트의 가운데에 직류평형(DC-balancing) 비트를 가진다. 시작비트와 정지 비트는 항상 1과 0의 값을 가지기 때문에, 수신단 첫 번째 비트 출력과 마지막 비트 출력이 항상 1과 0으로 출력되면 수신부(200)가 복원동작을 마친 것으로 판단하게 하는 역할을 하고, DC₀와 DC₀ 비트는 장거리 전송에 따른 데이터의 왜곡을 최소화하기 위한 직류평형의 역할을 한다.
조정신호 생성부(Training Signal Generator)(30)는 수신기에 주파수 정보를 제공하는 몇 가지의 신호 패턴을 형성하여 실제 데이터가 전송되기 전에 클릭 복원회로가 데이터의 속도에 맞는 클릭 신호를 생성하도록 돕는 역할을 한다. 즉, 초기 동기와 신호와 시험 데이터 신호를 순차적으로 제공하여 수신부(200)가 동기화 되도록 하는 역할을 하는 수단이다.

상기 조정신호 생성부(30)에 의해 수신부(200)가 동기화 되면, 상기 조정신호 생성부(30)의 출력 대신 인코더(20)의 출력이 먹스(50)에 의해 선택되어 직렬기(70) 및 CMOS등의 논리신호를 LVDS(low voltage differential signaling: 저전압 차동 시그널링) 신호로 변환하는 LVDS 변환부(70)를 통해 인코딩된 직렬 전송 데이터로서 직렬 통신 채널을 통해 전송된다.
도 3 내지 도 5는 동작 단계에 따른 조정신호 생성부(30)의 신호 패턴을 보여준다. 먼저, 송신부(100, 200)에 전원이 인가되면 조정신호 생성부(30)는 수신부(200)가 데이터 속도에 동기된 클릭 신호를 생성할 때까지 클릭 신호를 생성하여 수신기 내부의 위상 고정 루프(Phase Locked Loop)에 기준 클릭을 제공해 주는 역할을 한다. 수신부(200)가 첫 번째 조정신호에 동기화되어 데이터의 속도에 맞는 클릭을 생성하게 되면 수신부(200)는 락(Lock) 신호를 생성하여 송신부(100)에 다음 단계의 신호를 전송받을 준비가 되었음을 알려준다.

락 신호를 인가받은 조정신호 생성부(30)는 클릭 신호의 생성을 중단하고, 수신부(200)에 실제 전송 데이터(인코딩되어 잉여비트들이 포함된 형태)와 비슷한 기 설정된 패턴 데이터를 두번째로 공급해 줌으로써 수신부(200)가 실제 데이터를 수신하기 위한 최적의 상태가 되기를 기다린다. 즉, 일정 시간동안 패턴 데이터를 시험 데이터로 전송한다.

한편, 이때의 시험 패턴 데이터에 포함된 직류 평형 비트들(DCA, DCF)을 실제 데이터 전송 시(예를 들어 1과 0의 조합인 경우)와는 달리 각각 1과 0으로 설정함으로써 이 신호가 실제 전송 데이터가 아닌 조정용 시험 데이터임을 알려준다. 상기 수신부(200)가 최적의 상태가 되기에 충분한 시간이 지난 후 조정신호 생성부는 시작 비트와 정지 비트가 포함된 28비트의 실제 전송 데이터를 직렬 전송하게 되고, 이때 DCA와 DCF 비트를 각각 0과 1로 설정함으로써 실제 전송 데이터를 구분할 수 있도록 한다.
상기 수신부(200)는 적렬 채널을 통해 수신한 VLDS 신호를 다시 논리레벨 신호로 변환하는 CMOS 변환부(210)를 통해 변환되어 클릭 복원을 위한 클릭 복원부(230)와 데이터 리타이머(220)를 거쳐 복원된 클릭에 맞추어 구분된 데이터 블록 단위로 신호가 획득된 후 병렬기(250)를 통해 신호가 병렬화된다. 이후, 시작 비트 검출부를 통해 잉여 비트들로 미세 락(fine lock)을 검출하고, 디코더(260)를 통해 실제 신호인 24비트 신호를 획득하여 출력 버퍼(280)를 통해 원래 송신된 병렬 신호 형태의 데이터 및 수신 클릭과 락 신호가 출력된다. 상기 락 신호는 상기 송신부(100)의 입력으로 제공된다.

도 6은 본 발명 일 실시예에 따른 클릭 복원 회로의 블록도를 나타낸 것으로 블록 복원부(230)와 관련 주변부의 일부 구성이 포함된 것이다.

신호의 속도에 반비례하는 지터의 특성을 이용하여, 송신기가 5~65MHz의 클릭 신호에 28비트의 데이터 정보를 인가하여 신호를 전송한다면, 수신기는 10~130MHz의 클릭 신호마다 14비트의 데이터 정보를 추출해 내도록 설계함으로써 수신기 내부의 지터를 최소화하였다. 즉, 인코딩시 구분한 데이터 블록의 크기에 따라 데이터를 추출하도록 하는 것으로 수신기에서 지터 저감 동작이 이루어지게 된다.

클릭 복원부(230)를 포함하는 도시된 회로의 동작은 크게 커스(Coarse) 전압 생성 동작, 위상 고정 루프 동기화 동작, 데이터 정렬 동작의 세 단계로 나누어진다. 커스 전압 생성 동작은 광대역 송수신기의 저지터 특성과 관련이 있는 동작으로서 수신기 내부의 위상 고정 루프가 10~130MHz의 넓은 주파수 범위를 하나의 미
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세 조정 전압으로 제어하는 대신에 전체 주파수 범위를 복수(예를 들어, 세 개)의 주파수 범위로 나누어, 소정 비트(범위가 3개 이상인 경우 2비트)의 커스 전압에 해당하는 주파수 대역만큼 미세 조정 전압으로 제어하는 방식을 가능하게 함으로써, 전압 제어 발진기(232) 이득을 최소화하는 효과를 얻게 한다. 전압 제어 발진기(232)의 이득이 크면 작은 조정 전압 변화에도 주파수 변화가 크게 나타나기 때문에 외부 잡음에 매우 민감하게 반응하여 지터 특성을 떨어뜨린다는 단점이 있다. 이러한 이유 때문에 커스 전압 제어 방식은 기존의 회로에서도 널리 쓰이고 있는 방식이지만, 주파수 범위에 따라 그에 맞는 커스 전압을 외부에서 직접 인가해 주는 방식을 사용해 왔기 때문에, 별도의 외부 제어 신호가 필수적이었다. 하지만, 본 실시예에서는 수신부(200)의 내부에서 자체적으로 동작 속도에 맞는 커스 전압을 생성하는 커스 코드 생성부(231)를 구성하는 것으로 이러한 문제점을 해결하였다.

상기 커스 코드 생성부(231)에 따른 커스 전압 동작은 다음과 같이 이루어진다. 초기 송신신부에 처음 전원이 인가되면 가장 먼저 송신신 부 내부의 위상 고정 루프(40)를 기준 클럭 신호에 동기 시키는 동작을 하게 되는데, 위상 고정 루프가 동기 될 때까지 송신신 부(40)의 직렬 채널 출력은 0으로 고정되도록 한다. 그에 따라, 수신부(200)는 송신부(100)가 정상 동작을 할 때까지 0의 입력을 받아들이게 된다. 이때, 송신부(100) 내부의 직렬기(60)는 송신부 내부의 위상 고정 루프(40)가 진동하면서 발생시키는 클럭 신호로 직렬 데이터 신호를 샘플링하는데, 직렬 데이터 신호가 0으로 고정되어 있기 때문에, 샘플링 된 14비트의 신호도 모두 0으로 고정된
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다. 송신부(100) 내부의 위상 고정 루프(40)가 동기 동작을 마치게 되면, 앞서 설명한대로 초기 동기화를 위한 첫 번째 조정신호인 클럭 신호가 송신기의 출력, 즉 직렬 데이터가 되어 수신부(200)로 전송된다. 직렬 데이터가 0이 아닌 값을 가지게 되면, 상기 수신부(200)에 포함된 병렬기(243)는 24비트의 출력 중 적어도 하나의 출력을 1로 가지게 된다.

도 7은 클럭 복원부(230)에 포함된 개시회로(241)의 구성을 보인 것으로, 노어게이트, 네드게이트, 반전기 등의 간단한 회로(310)로 구성되어 14비트의 병렬기 출력이 모두 0일 때와 적어도 하나가 1일 때를 구분하여, 송신부(100)가 내부적인 동기 동작을 마치고 어떠한 신호를 제공하기 시작하였음을 수신부(200)에 알려주는 역할을 하는 회로이다. 시작회로 내부의 노어게이트, 네드게이트, 반전기로 구성된 판별회로(310)가 병렬기의 출력이 적어도 하나의 1을 가졌을 판별해내게 되면, 판별회로(310)의 최종단에 연결된 10단의 D-플립플롭 회로(320)가 8분주된 클럭 신호를 통해 80주기의 긴 펄스신호를 발생시킨다. 이 펄스 신호는 시작회로의 최종 출력인 커스 인에이블(Coarse Enable) 신호가 되어 전체 수신부(200)를 리셋시키고, 커스 전압 생성 동작을 시작하게 한다. 여기서, 80주기의 긴펄스를 생성하는 회로 및 방식은 수신부(200)의 초기 동기화를 위해 필요한 소정의 지연을 얻기 위한 것으로 그 구체적인 구성이나 지연 시간은 다르게 구성할 수 있다.

상기 커스 코드 생성 동작은 도 8의 커스 전압 생성기(440)에 의해 이루어진다. 커스 인에이블(Coarse Enable) 신호는 멕스(234, 235)에 연결되어 커스 인에이블 신호가 1의 값을 갖는 동안 전하펌프1(CP1)(236)의 입력 UP1과 DN1 신호를 각각
VDD, GND와 연결되도록 하여 전하펌프 1(236)이 전압 제어 발전기 (232)를 현재의 커스 코드에서 발전할 수 있는 최대의 속도로 발전하도록 설정한다. 앞서 시작회로 (241)의 동작에 의해 수신부 (200)의 모든 회로가 리셋 동작을 마친 상태이므로 처음 커스 코드는 00의 상태를 가지게 되고, 이때의 전압 제어 발전기 (232)는 현재의 커스 코드에 따라 가장 낮은 주파수 범위 대에서 나타낼 수 있는 최고 주파수로 발전하고 있는 상태이다. 커스 코드 생성부 (231)는 현재 커스 코드에서의 최대 주파수로 발전하는 전압 제어 발전기 (232)의 클릭 신호와 기준 클릭 신호의 형태로 인가되고 있는 직렬 데이터 신호를 입력받아 이를 반전기로 구성된 지연단 및 D-플립 플립단 (443)에 인가한다. 지연단에 연결된 D-플립플립단은 지연된 클릭 신호의 상승 모서리에서 입력 클릭 신호를 샘플링하여 지연된 클릭 신호가 입력 클릭 신호의 하강 모서리보다 앞선 위치를 갖는 경우에는 1, 하강 모서리보다 뒤처진 위치를 갖는 경우에는 0의 값을 출력하게 함으로써 입력 클릭 신호의 하강 모서리와 지연된 클릭의 상승 모서리가 비슷한 위치를 갖는 부분에서는 출력 값이 1에서 0으로 바뀌게 된다. 이는 클릭 신호의 하강 모서리가 몇 개의 지연셀을 거친 신호와 비슷한 위치를 갖게 되는지 찾아내는 역할을 한다. 식별기 (1-0 검출기 (Identifier)) (444)는 도 9의 회로가 연속적으로 배열되어 있는 블록으로서 입력 신호가 1에서 0으로 바뀌는 부분에서 1의 신호를 출력하는 회로이기 때문에, 클릭 신호의 하강 모서리의 위치에 해당하는 단에서 1의 신호를 발생시킨다. 위의 동작을 통해 식별기 (444)가 N번째 단에서 1의 신호를 출력하였다면 그 입력 신호의 주기는 2N과 비슷한 값을 갖는다는 것을 알 수 있기 때문에, 식별기 (444)가 몇 번째 단에서 1의 값을
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 출력하는 가를 비교함으로써 어떤 신호가 더 짧은 신호인지를 쉽게 검출해 낼 수 있다. 만약 이러한 동작을 통해 직렬 데이터 신호가 전압 제어 발진기(232)의 클릭 신호보다 빠르다고 판단이 되면 간단한 디지털 로직으로 구성된 로직부(445, 441)를 통해 코스 코드를 하나 증가시키고, 코스 코드가 증가함에 따라 한 단계 높은 범위 대에서 발진하는 전압 제어 발진기(232)의 클릭 신호를 직렬 데이터 신호와 비교하여 코스 코드를 하나 증가시키거나, 현재의 값을 유지하게 하는 동작을 한번 더 반복한다.

기준 클릭 신호의 80주기에 해당하는 시간이 지난 후 코스 인에이블 신호는 0의 값으로 바뀌게 된다. 코스 인에이블 신호가 0이 되면, 앞서 코스 코드 생성 동작을 위해 각각 VDD, GND를 출력으로 선택했던 다중 위상 선택기가 PFD_UP, PFD_DN 신호를 출력으로 선택하게 되고, 생성된 코스 코드는 그대로 유지된다. PFD_UP, PFD_DN 신호는 위상-주파수 검출기의 출력이기 때문에, 전체 클릭 복원 회로는 전압 제어 발진기(232), 위상-주파수 검출기(233), 전하펌프1(236), 투프틀레(저항 및 커파시터 구성)로 구성되는 일반적인 위상 고정 루프의 형태를 갖게 된다. 위상고정 루프 동기화 동작은 이 위상 고정 루프를 통해 기준 클릭 형태로 인가되는 직렬 데이터에 전압 제어 발진기(232)의 출력 클릭을 동기화시키는 동작이다. 직렬 데이터에 전압 제어 발진기(232)의 출력 클릭이 어느 정도 동기가 되면, 도 10의 동기 검출기(510, 520, 530)에 의해 주파수락(Freq.Lock) 신호가 검출된다. 동기 검출기는 위상 고정 루프 동기화 동작 동안 직렬 데이터와 전압 제어 발진기(232)의 출력 클릭을 입력받아 두 신호의 위상차가 D-플립플립 입력단의 버퍼셀의 지연
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시간보다 작을 때 두 신호가 동기되었다고 판단하여 락 신호를 1로 출력한다. 락
신호에 연결된 5개의 D-플립플롭(530)은 아래에 연결된 리셋회로(520)와 함께 동기
검출기의 오동작에 대비하여 락 신호가 5주기 이상 1로 출력될 때에만 최종 출력
(Freq. Lock)을 1로 출력하게 하는 역할을 한다.

주파수 락(Freq. Lock) 신호가 1을 출력하면 수신부(200)는 위상 고정 푸프
동기화 동작을 멈추고, 다음 위상 선택기(238)의 출력을 변경시켜 새로운 푸프를
구성하게 된다. 새로운 푸프는 전압 제어 발전기(232), 선행 위상 검출기(Linear
PD)(239), 전하평포2(CP2)(237)로 구성되고, 푸프를 통해 생성된 전압 제어 발전기
(232) 클럭과 정렬된 적절 데이터 신호가 병렬(243)에 연결된다. 이때, 송신부
(100)의 조정신호 생성부(30)는 수신부(200)에서 출력한 주파수 락(Freq. Lock) 신
호를 입력받아 수신부(200)가 데이터를 받을 준비가 되었음을 알고 앞서 설명한대
로 2번째와 3번째 패턴(도 4 및 도 5)의 조정신호를 전송한다.

새롭게 구성된 푸프는 데이터 정렬 동작을 담당하는 푸프로서 전압 제어 발
전기(232) 클럭의 상승 모서리가 실제 데이터 신호 각 비트의 정중앙에 위치하도록
정렬하는 역할을 한다. 기존의 고속 송수신기의 경우 주로 뱅-뱅(Bang-Bang) 위상
검출기를 사용하여 클럭 복원 회로를 구성하는데, 이는 복원되는 클럭 신호가 상대
적으로 큰 지터를 갖고, 이로 인해 비트 에러율(BER)이 높아질 수 있다는 단점이
있기 때문에, 본 시스템에서는 선행 위상 검출기(239)를 사용하여 상대적으로 작은
지터와 낮은 비트 에러율을 나타내도록 설계하였다.

상기 전압 제어 발전기(232)는 14개의 스테이지, 즉 14개의 상이한 위상을

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가지는 전압 제어 발전기를 이용하며, 이를 통해 14 비트의 데이터 블록(데이터 12
비트와 잉여 2비트)에 대한 발전 출력을 제공할 수 있다. 만일 입력 신호를 다른
크기의 데이터 블록으로 구분할 경우라면 상이한 스테이지가 필요하다.

도 11과 도 12는 상기 선행 위상 검출기(239)의 예제 회로도와 외장의 동작
파형을 나타낸 그림이다. 상기 선행 위상 검출기(239) 회로는 2개의 다중 위상 클러
릭 신호(CLK(n), CLK(n-1)), 2개의 병렬기 출력 신호(DES(n-1), DES(n)), 그리고
직렬 데이터 신호를 입력받아 병렬기 출력 신호가 차례로 0과 1의 값을 가질 때,
다시 말해서 직렬 데이터 신호가 상승 모서리를 가질 때, 세 개의 다중 위상 클릭
신호 중 가운데 신호와 직렬 데이터 신호의 위상 차이에 따라 그 위상 차이에 해당
하는 폄스 신호를 출력하는 동작을 한다. 예를 들어 14개의 다중 위상 중에서 1번
체, 2번째 다중 위상 클릭 신호를 사용한다고 가정하면, 1번째 클릭 신호에 의해
샘플링 된 직렬 데이터 신호와 2번째 클릭 신호에 의해 샘플링 된 직렬 데이터 신
호가 각각 0과 1이라면, 즉, 도 12에서와 같이 직렬 데이터 신호가 1번째 클릭과 2
번째 클릭 신호의 사이에서 상승 모서리를 가지게 된다면, 상기 선행 위상 검출기
(239)는 직렬 데이터의 상승 모서리와 2번째 클릭 신호의 상승 모서리의 위상차를
PD_DN 신호로, 직렬 데이터의 상승 모서리와 2번째 클릭 신호의 상승 모서리의 위
상차를 PD_UP 신호로 나타낸다. PD_DN과 PD_UP 신호는 다중 위상 클릭 신호와 직렬
데이터 신호의 위상차와 비례하는 폄스로 나타나게 되므로, PD_DN 신호가 PD_UP 신
호 보다 넓은 폄스로 나타날 경우에는 다중 클릭 신호가 더 느리지도록 전하펌프
2(237)에 신호를 보내고, 반대의 경우에는 다중 클릭 신호가 더 빨라지도록 전하펌프

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프2(237)에 신호를 보낸다. PD_DN 신호와 PD_UP 신호의 너비가 같은 경우에는 2번째 클릭이 직렬 데이터의 정중앙에 위치한 경우이므로 이 경우 전하펌프2(237)는 출력 전류를 일정하게 유지한다.

PD_DN 신호와 PD_UP 신호는 전하펌프의 입력이 되는 신호이므로 두 신호 사이의 위상차가 존재하면 전하펌프에 전류 오차를 발생시켜 고정 위상 오차를 발생시킬 수 있으므로, 항상 먼저 출력되는 PD_DN 신호는 지연셀 한단의 저연, 즉 다중 위상 클릭 신호 간 위상차의 절반의 위상이 지연된 상태로 출력되도록 설계하여 고정 위상 오차를 최소화하도록 하였다.

신형 위상 검출기(239)에 의한 데이터 정렬을 마치면, 병렬기(243)의 첫 번째 출력과 마지막 출력은 항상 시작비트와 정지 비트를 의미하는 1과 0으로 고정된다. 간단한 로직으로 첫 번째 출력과 마지막 출력이 1과 0으로 출력됨을 검출하는 회로인 시작비트 검출기(243)는 시작비트와 정지 비트가 1과 0으로 고정됨을 확인하면 미세 락(Fine Lock) 신호를 1로 고정시키어 병렬기(243)의 출력을 사용해도 좋다는 허가 신호를 제공한다. 최종적으로 수신부(200)는 병렬기(243)의 28비트 출력 신호 중 시작비트, 정지 비트, DC_A, DC_B를 제외한 실제 24비트의 출력과 데이터 속도에 동기된 클릭 신호를 출력한다.
【특허청구범위】

【청구항 1】

전송할 병렬 데이터를 입력받아 직류 평형 정보를 포함하는 송신 데이터로 인코딩함과 아울러 하기의 수신부로부터 제공되는 락 신호와 외부 제공 클럭 및 내부 위상 고정 루프의 통신 클럭을 근거로 복수 단계로 이루어진 초기 동기화를 위한 동기화 신호들을 직접 통신 방식으로 출력하는 조정신호 생성부와, 상기 조정신호 생성부가 제공하는 초기 동기화 신호에 따른 동기 신호를 제공하거나 상기 통신 클럭에 따라 인코딩된 데이터를 직접 전송하는 직렬 전송 수단을 포함하는 송신부와;

상기 송신부의 조정신호 생성부를 통한 동기 신호가 수신되면 위상 주파수 검출 방식을 통해 전압 제어 발전기를 제어하면서 동기화를 수행한 후 동기화되면 락 신호를 상기 송신부에 제공하고, 상기 송신부로부터 상기 인코딩된 데이터가 수신되면 해당 데이터와 상기 전압 제어 발전기 출력을 선행 위상 검출기를 통해 파악하여 클럭을 복원하는 클럭 복원부를 포함하며, 이를 통해 동기화 및 데이터 수신을 실시한 후 수신된 데이터의 디코딩을 통해 전송대상의 병렬 데이터를 출력하는 수신부를 포함하는 것을 특별적으로 하는 직렬 송수신 장치.

【청구항 2】

제 1항에 있어서, 상기 송신부는 복수의 병렬 데이터 신호를 입력받아 해당
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병렬 데이터 신호를 두개 이상의 단위로 분할한 후, 상기 분할 위치에 직류 평형을 위한 정보를 삽입하고, 전체 데이터의 시작과 종료 부분에 각각 시작 정보와 종료 정보를 삽입하는 인코딩 수단을 포함하는 것을 특징으로 하는 직렬 송수신 장치.

【청구항 3】

제 2항에 있어서, 상기 인코딩 수단은 복수의 병렬 데이터를 균일한 크기의 데이터 블록으로 분할하고, 상기 각 분할된 데이터 블록 사이에 직류 평형 및 신호 구분을 위한 한쌍의 비트를 삽입하며 시작 비트와 정지 비트를 전체 데이터의 앞과 뒤에 삽입한 전송용 데이터를 생성하는 것을 특징으로 하는 직렬 송수신 장치.

【청구항 4】

제 1항에 있어서, 상기 조정신호 생성부는 상기 수신부로부터 락 신호를 수신하지 못하는 경우 상기 수신부가 데이터 속도에 동기된 클럭 신호를 생성할 때까지 동기화 신호를 제공하며, 상기 수신부로부터 락 신호를 수신할 경우 상기 동기화 신호 대신 실제 전송할 인코딩 데이터 형태의 기 설정된 패턴을 가지는 시험 데이터를 기 설정된 시간동안 전송하는 것을 특징으로 하는 직렬 송수신 장치.

【청구항 5】

제 4항에 있어서, 상기 조정신호 생성부가 전송하는 기 설정된 패턴을 가진
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데이터는 상기 데이터에 포함된 직류 평형 신호의 값이 실제 인코딩된 데이터에 포함되는 직류 평형 신호의 값과 상이한 것을 특징으로 하여 직렬 송수신 장치.

【청구항 6】

제 1항에 있어서, 상기 수신부의 클럭 복원부는

상기 복수 스테이지를 가지는 전압제어 발전기와;

상기 전압제어 발전기의 출력과 수신되는 직렬 데이터를 근거로 상기 전압제어 발전기를 제어하는 내장 커스 코드 (Coarse Code) 생성부와;

상기 조정신호 생성부를 통해 제공되는 동기 신호를 근거로 상기 전압제어 발전기를 미세 조정하는 제 1 동기화 수단과;

상기 수신 직렬 데이터와 상기 전압제어 발전기 출력을 입력으로 하는 신형 위상 격출기를 통해 얻어지는 정보로 상기 전압제어 발전기를 미세 조정하는 제 2 동기화 수단과;

상기 제 1 또는 제 2 동기화 수단에 의한 동기 여부를 검출하여 락 신호를 상기 수신부에 제공하는 락 격출 수단을 포함하는 것을 특징으로 하는 직렬 송수신 장치.

【청구항 7】

제 6항에 있어서, 상기 클럭 복원부는 수신되는 직렬 데이터를 분석하여 신
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호가 없던 상태에서 신호가 포함되는 상태로 변경되는 경우 일정 시간동안 상기 제1동기화 수단을 동작시켜 동기화 과정을 수행하도록 하는 개시 회로부를 더 포함하는 것을 특정으로 하는 직렬 송수신 장치.

【청구항 8】

제 6항에 있어서, 상기 내장 커스 코드 생성부는

상기 복수 스테이지의 전압 제어 발진기 출력을 지연시키는 복수의 제 1지연단과;

상기 수신되는 직렬 데이터를 지연시키는 복수의 제 2지연단과;

상기 제 1지연단의 출력에 따른 전압 제어 발진기의 출력 하강 모서리 위치를 검출하여 전압 제어 발진기의 주기를 파악하는 식별기와;

상기 식별기의 출력과 제 2지연단의 출력에 따른 수신 직렬 데이터의 위상을 비교하여 상기 전압 제어 발진기 출력과 수신 직렬 데이터의 선후를 파악하여 상기 전압 제어 발진기의 출력을 제어하는 신호를 출력하는 논리부를 포함하는 것을 특정으로 하는 직렬 송수신 장치.

【청구항 9】

제 6항에 있어서, 상기 복수 스테이지의 전압 제어 발진기는 하나의 외부 클럭에 대해서 제공되는 직렬 신호들 중에서 상기 삽입된 직류 평형 정보에 의해 구
분리는 데이터 블록의 비트크기와 상기 삽입된 직류 평형 정보의 절반크기와 시작 또는 정지 비트의 크기를 더한 값과 동일한 크기의 스테이지지를 가지는 것을 특징으로 하는 직렬 송수신 장치.

【청구항 10】

동기화에 따른 락 신호를 제공하는 직렬 수신 장치와 연결되어 병렬 데이터를 직렬 데이터로 전송하는 직렬 송신 장치에 있어서,

전송할 병렬 데이터를 입력받아 직류 평형 정보와 시작 및 종료 정보를 포함하는 송신 데이터로 인코딩하는 인코딩부와;

상기 직렬 수신 장치로부터 제공되는 락 신호와 외부 제공 클럭 및 내부 위상 고정 루프의 통신 클럭을 근거로 동기화 신호들을 직렬 통신 방식으로 제공하는 조정신호 생성부와;

상기 조정신호 생성부가 제공하는 동기화 신호에 따른 동기 신호를 제공하거나 상기 통신 클럭에 따라 인코딩된 데이터 중 하나를 선택하여 직렬 전송하는 직렬 전송 수단을 포함하는 것을 특징으로 하는 직렬 송신 장치.

【청구항 11】

제 10항에 있어서, 상기 인코딩부는 복수의 병렬 데이터를 균일한 크기의 데이터 블록으로 분할하고, 상기 각 분할된 데이터 블록 사이에 직류 평형 및 신호
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구분을 위한 한쌍의 비트를 삽입하며 시작 비트와 정지 비트를 전체 데이터의 앞과
뒤에 삽입한 전송용 데이터를 생성하는 것을 특징으로 하는 직렬 송신 장치.

【청구항 12】

제 10항에 있어서, 상기 조정신호 생성부는 상기 수신 장치로부터 락 신호를
수신하지 못하는 경우 상기 수신 장치가 데이터 속도에 동기된 클럭 신호를 생성할
때까지 동기화 신호를 제공하며, 상기 수신 장치로부터 락 신호를 수신할 경우 상
기 동기 신호 대신 실제 전송할 인코딩 데이터 형태로 기 설정된 패턴을 가지는 시
험 데이터를 기 설정된 시간동안 전송하는 것을 특징으로 하는 직렬 송신 장치.

【청구항 13】

제 12항에 있어서, 상기 조정신호 생성부가 전송하는 기 설정된 패턴을 가진
데이터는 상기 데이터에 포함된 적류 평형 신호의 값이 실제 인코딩된 데이터에 포
함되는 적류 평형 신호의 값과 상이한 값을 특징으로 하는 직렬 송신 장치.

【청구항 14】

연결시 직렬 통신 방식으로 순차적인 초기 동기화 신호를 제공하고, 동기화
에 끝나는 경우 실제 데이터를 전송하는 송신기와 연결되는 직렬 수신 장치에 있어
서,
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상기 송신기가 제공하는 순차적인 동기화 신호를 직접 통신 방식으로 수신하여 위상 주파수 검출 방식을 통해 통신용 동기를 맞추어 동기화가 끝났음을 알리는 락 신호를 상기 송신기에 제공하고, 상기 송신기로부터 제공되는 상기 실제 데이터를 선형 위상 검출기를 통해 파악하여 클럭을 복원하는 클럭 복원부와;

상기 클럭 복원부를 통해 복원되는 클럭에 맞추어 실제 수신되는 데이터로부터 실제 데이터를 획득하며, 상기 획득된 실제 데이터를 디코딩하여 전송대상의 병렬 데이터를 출력하는 수신 신호 처리 수단을 포함하는 것을 특징으로 하는 직접 수신 장치.

【참조항 15】

제 14항에 있어서, 상기 클럭 복원부는

복수 스테이지를 가지는 전압제어 발진기와;

상기 전압제어 발진기의 출력과 수신되는 직렬 데이터를 근거로 상기 전압제어 발진기를 제어하는 내장 코스 코드(Coarse Code) 생성부와;

상기 조정신호 생성부를 통해 제공되는 동기 신호를 근거로 상기 전압제어 발진기를 미세 조정하는 제 1동기화 수단과;

상기 수신 직렬 데이터와 상기 전압제어 발진기 출력을 입력으로 하는 선형 위상 검출기를 통해 얻어지는 정보로 상기 전압제어 발진기를 미세 조정하는 제 2 동기화 수단과;
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상기 제 1 또는 제 2동기화 수단에 의한 동기 여부를 검출하여 락 신호를 상기 송신부에 제공하는 락 검출 수단을 포함하는 것을 특징으로 하는 직렬 수신 장치.

【청구항 16】

제 15항에 있어서, 상기 내장 커스 코드 생성부는

상기 복수 스테이지의 전압 제어 발진기 출력을 지연시키는 복수의 제 1지연단과;

상기 수신되는 직렬 데이터를 지연시키는 복수의 제 2지연단과;

상기 제 1지연단의 출력에 따른 전압 제어 발진기의 출력 하강 모서리 위치를 검출하여 전압 제어 발진기의 주기를 파악하는 식별기와;

상기 식별기의 출력과 제 2지연단의 출력에 따른 수신 직렬 데이터의 위상을 비교하여 상기 전압 제어 발진기 출력과 수신 직렬 데이터의 신호를 파악하여 상기 전압 제어 발진기의 출력을 제어하는 신호를 출력하는 논리부를 포함하는 것을 특징으로 하는 직렬 수신 장치.

【청구항 17】

제 15항에 있어서, 상기 복수 스테이지의 전압 제어 발진기의 하나의 외부 클럭에 대해서 제공되는 직렬 신호들 중에서 상기 삽입된 직류 평형 정보에 의해
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구분되는 데이터 블록의 비트 크기와 상기 삽입된 적류 평형 정보의 절반 크기와 시작 또는 정지 비트의 크기를 더한 값과 동일한 크기의 스테이지를 가지는 것을 특징으로 하는 적렬 수신 장치.

【청구항 18】

송신기와 수신기가 직렬 채널을 통해 연결되는 경우 상기 송신기가 수신기에 동기화 클럭 정보를 직렬 채널을 통해 전송하는 초기 동기화 단계와;

상기 초기 동기화 단계를 통해 수신기가 동기되면 동기 완료 정보를 상기 송신기에 제공하고, 그에 따라 상기 송신기가 기 설정된 형태의 시험 데이터를 상기 직렬 채널을 통해 일정 시간 전송하는 전송 준비 단계와;

상기 송신기가 실제 데이터를 균일한 복수의 크기로 구분하여 적류 평형 정보를 구분 영역마다 포함시키고, 전체 데이터에 시작 및 종료 정보를 포함시켜 양여 정보를 가지는 실제 전송 데이터로 인코딩하여 상기 직렬 채널을 통해 직렬 전송하는 단계와;

상기 수신기는 상기 직렬 채널을 통해 수신되는 실제 전송 데이터를 선형 위상 검출 방식을 통해 동기된 클럭 주파수와 비교하여 클럭의 지터를 보정하면서 직렬 수신된 상기 실제 전송 데이터로부터 데이터를 획득하여 상기 양여 정보를 제거한 원래의 데이터로 디코딩하여 출력하는 단계를 포함하는 것을 특징으로 하는 직렬 송수신 장치의 통신 방법.
【청구항 19】

제 18항에 있어서, 상기 초기 동기화 단계는 상기 수신기가 수신되는 동기화 신호와 상기 수신기에 내장된 전압 제어 발진기의 출력을 입력들로 하여 동작하는 커스 코드 생성부의 출력에 의해 상기 전압 제어 발진기가 제어되는 방식으로 동기화가 이루어지는 단계와;

상기 전압 제어 발진기의 출력과 수신되는 동기화 신호를 위상 주파수 검출 수단을 통해 비교하여 상기 전압 제어 발진기를 미세 제어하는 단계를 포함하는 것을 특징으로 하는 직렬 송수신 장치의 통신 방법.

【청구항 20】

제 18항에 있어서, 상기 전송 준비 단계는 상기 송신기가 임의 정보를 가지는 실제 전송 데이터의 형태이면서 상기 직류 평형 정보의 값을 실제 전송 데이터와 상이하도록 한 시험 데이터를 일정 시간 전송하는 단계를 포함하는 것을 특징으로 하는 직렬 송수신 장치의 통신 방법.

【도면의 간단한 설명】

<44> 도 1은 기존 클럭을 사용하지 않는 고속 송수신기의 구성을 도시한 블록도.

<45> 도 2는 고속 송수신기의 신호 전송 형태를 나타낸 도면.

<46> 도 3은 조정 신호 발생기의 초기 동기화 신호 전송 형태를 나타낸 도면.
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47> 도 4는 조정 신호 발생기의 시험 데이터 전송 형태를 나타낸 도면.

48> 도 5는 조정 신호 발생기의 실제 데이터 전송 형태를 나타낸 도면.

49> 도 6은 클릭 복원 회로의 구성을 도시한 블록도.

50> 도 7은 시작 회로의 구성을 도시한 블록도.

51> 도 8은 커스 전압 생성기의 구성을 도시한 블록도.

52> 도 9는 커스 전압 생성기에 포함된 1-0 검출기의 구성을 도시한 블록도.

53> 도 10은 동기 검출기 회로의 구성을 도시한 블록도.

54> 도 11은 선행 위상 검출기 회로의 구성을 도시한 블록도.

55> 도 12는 선행 위상 검출기에 의해서 위상 차이가 검출되는 경우를 도시한 도면.

56> ** 도면의 주요 부분에 대한 부호의 설명 **

57> 10: 입력 버퍼 20: 인코더

58> 30: 조정신호 생성부 40: 위상 고정 루프

59> 50: 믹스 60: 적렬기

60> 70: LVDS 변환부 100: 송신부

61> 200: 수신부 210: CMOS 변환부

62> 220: 데이터 리타이머 230: 클릭 복원부

63> 250: 병렬기 260: 디코더

64> 270: 시작비트 검출부 280: 출력 버퍼
【도면】

【도 1】

【도 2】

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출원번호: 10-2007-0073815

【도 4】

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【도 5】

정지비트 시작비트 DC4 DC6 정지비트 시작비트
0 1 1 1 0 1 0

【도 6】

상세 도면과 함께 설명을 제공할 수 있습니다.
**PATENT APPLICATION FEE DETERMINATION RECORD**  
Substitute for Form PTO-875

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<th>APPLICATION AS FILED – PART I</th>
<th>SMALL ENTITY</th>
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<td>INDEPENDENT CLAIMS (37 CFR 1.16(h))</td>
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<td>If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($130 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(a).</td>
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**MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))**

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**APPLICATION AS AMENDED – PART II**

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**AMENDMENT B**

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*If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

**If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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