**APPLICATION NO.** | **ISSUE DATE** | **PATENT NO.** | **ATTORNEY DOCKET NO.** | **CONFIRMATION NO.**
---|---|---|---|---
12/641,432 | 02/07/2012 | 8110461 | SUN.DH.627 | 1608

23557 | 7590 | 01/18/2012

SALIWANCHIK, LLOYD & EISENCHENK
A PROFESSIONAL ASSOCIATION
PO Box 142950
GAINESVILLE, FL 32614

**ISSUE NOTIFICATION**

The projected patent number and issue date are specified above.

**Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)**

(application filed on or after May 29, 2000)

The Patent Term Adjustment is 143 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Young Jun Kwon, Chungbuk, KOREA, REPUBLIC OF;
PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail
Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571) 273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note Use Block 1 for any change of address)

25557 7590 10/1/2011
SALIWANCHIK, LLOYD & EISENSCHEINK
A PROFESSIONAL ASSOCIATION
PO Box 142950
GAINESVILLE, FL 32614

Phone: (352) 375-8100 Fax: (352) 372-5800

APPLICATION NO. 12/641,432 FILING DATE 12/18/2009 FIRST NAMED INVENTOR Young Jun Kwon ATTORNEY DOCKET NO. SUNDH.627 CONFIRMATION NO. 1508
TITLE OF INVENTION: FLASH MEMORY DEVICE AND MANUFACTURING METHOD OF THE SAME

<table>
<thead>
<tr>
<th>APPLN. TYPE</th>
<th>SMALL ENTITY</th>
<th>ISSUE FEE DUE</th>
<th>PUBLICATION FEE DUE</th>
<th>PREV. PAID ISSUE FEE</th>
<th>TOTAL FEES DUE</th>
<th>DATE DUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>nonprovisional</td>
<td>NO</td>
<td>$1740</td>
<td>$300</td>
<td>$0</td>
<td>$2040</td>
<td>01/11/2012</td>
</tr>
</tbody>
</table>

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
   - Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
   - Fee Address indication (or "Fee Address" Indication form PTOSB247; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list:
   - (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
   - (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

   Saliwanchik, Lloyd & Eisenbench

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)
   PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 1.11. Completion of this form is NOT a substitute for filing an assignment.

   (A) NAME OF ASSIGNEE
   DONGBU HITEK CO., LTD.
   SEOUL, KOREA

   (B) RESIDENCE: (CITY AND STATE OR COUNTRY)

   Please check the appropriate assignee category or categories (will not be printed on the patent):
   □ Individual
   □ Corporation or other private group entity
   □ Government

4a. The following fee(s) are submitted:
   □ Issue Fee
   □ Application Fee (No small entity discount permitted)
   □ Advance Order - # of Copies

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)
   □ A check is enclosed.
   □ Payment by credit card. Form PTO-2038 is attached.
   □ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number ___________________________ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)
   a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
   b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

   NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

   Authorized Signature
   Jeff Lloyd
   Typed or printed name

   Date January 3, 2012
   Registration No. 35,589

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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PTO/SB-40 (Rev. 02/11) Approved for use through 08/31/2013.
OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Electronic Patent Application Fee Transmittal

<table>
<thead>
<tr>
<th>Application Number:</th>
<th>12641432</th>
</tr>
</thead>
<tbody>
<tr>
<td>Filing Date:</td>
<td>18-Dec-2009</td>
</tr>
<tr>
<td>Title of Invention:</td>
<td>FLASH MEMORY DEVICE AND MANUFACTURING METHOD OF THE SAME</td>
</tr>
<tr>
<td>First Named Inventor/Applicant Name:</td>
<td>Young Jun Kwon</td>
</tr>
<tr>
<td>Filer:</td>
<td>Jeff Lloyd/Jennifer R. Ruppert</td>
</tr>
<tr>
<td>Attorney Docket Number:</td>
<td>SUN.DH.627</td>
</tr>
</tbody>
</table>

Filed as Large Entity

**Utility under 35 USC 111(a) Filing Fees**

<table>
<thead>
<tr>
<th>Description</th>
<th>Fee Code</th>
<th>Quantity</th>
<th>Amount</th>
<th>Sub-Total in USD($)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Basic Filing:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pages:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Claims:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Miscellaneous-Filing:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Petition:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Patent-Appeals-and-Interference:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Post-Allowance-and-Post-Issuance:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Utility Appl issue fee</td>
<td>1501</td>
<td>1</td>
<td>1740</td>
<td>1740</td>
</tr>
<tr>
<td>Publ. Fee- early, voluntary, or normal</td>
<td>1504</td>
<td>1</td>
<td>300</td>
<td>300</td>
</tr>
<tr>
<td>Description</td>
<td>Fee Code</td>
<td>Quantity</td>
<td>Amount</td>
<td>Sub-Total in USD($)</td>
</tr>
<tr>
<td>-------------------</td>
<td>----------</td>
<td>----------</td>
<td>--------</td>
<td>---------------------</td>
</tr>
<tr>
<td>Extension-of-Time</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Miscellaneous</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Total in USD ($)</strong></td>
<td></td>
<td></td>
<td>2040</td>
<td></td>
</tr>
<tr>
<td>Electronic Acknowledgement Receipt</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>------------------------------------</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>EFS ID:</strong></td>
<td>11745302</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Application Number:</strong></td>
<td>12641432</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>International Application Number:</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Confirmation Number:</strong></td>
<td>1608</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Title of Invention:</strong></td>
<td>FLASH MEMORY DEVICE AND MANUFACTURING METHOD OF THE SAME</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>First Named Inventor/Applicant Name:</strong></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Customer Number:</strong></td>
<td>23557</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Filer:</strong></td>
<td>Jeff Lloyd/Jennifer R. Ruppert</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Filer Authorized By:</strong></td>
<td>Jeff Lloyd</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Attorney Docket Number:</strong></td>
<td>SUN.DH.627</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Receipt Date:</strong></td>
<td>03-JAN-2012</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Filing Date:</strong></td>
<td>18-DEC-2009</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Time Stamp:</strong></td>
<td>13:32:39</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Application Type:</strong></td>
<td>Utility under 35 USC 111(a)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Payment information:**

<table>
<thead>
<tr>
<th>Submitted with Payment</th>
<th>yes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Payment Type</td>
<td>Credit Card</td>
</tr>
<tr>
<td>Payment was successfully received in RAM</td>
<td>$2040</td>
</tr>
<tr>
<td>RAM confirmation Number</td>
<td>10100</td>
</tr>
<tr>
<td>Deposit Account</td>
<td>190065</td>
</tr>
<tr>
<td>Authorized User</td>
<td>LLOYD, JEFF</td>
</tr>
</tbody>
</table>

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

- Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)
- Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.
NOTICE OF ALLOWANCE AND FEE(S) DUE

EXAMINER
EXAMINEE

PHAM, HOAI V

ART UNIT
PAPER NUMBER

2892

DATE MAILED: 10/11/2011

APPLICATION NO. 12/641,432
FILING DATE 12/18/2009
FIRST NAMED INVENTOR Young Jun Kwon
ATTORNEY DOCKET NO. SUN.DH.627
CONFIRMATION NO. 1608

TITLE OF INVENTION: FLASH MEMORY DEVICE AND MANUFACTURING METHOD OF THE SAME

<table>
<thead>
<tr>
<th>APPLN. TYPE</th>
<th>SMALL ENTITY</th>
<th>ISSUE FEE DUE</th>
<th>PUBLICATION FEE DUE</th>
<th>PREV. PAID ISSUE FEE</th>
<th>TOTAL FEE(S) DUE</th>
<th>DATE DUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>nonprovisional</td>
<td>NO</td>
<td>$1740</td>
<td>$300</td>
<td>$0</td>
<td>$2040</td>
<td>01/11/2012</td>
</tr>
</tbody>
</table>

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:
A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.
B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:
A. Pay TOTAL FEE(S) DUE shown above, or
B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.
**PART B - FEE(S) TRANSMITTAL**

Complete and send this form, together with applicable fee(s), to: Mail

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

or Fax
(571)-273-2885

**APPLICATION NO.** | **FILING DATE** | **FIRST NAMED INVENTOR** | **ATTORNEY DOCKET NO.** | **CONFIRMATION NO.**
--- | --- | --- | --- | ---
12/641,432 | 12/18/2009 | Young Jun Kwon | SUN.DH.627 | 1608

**TITLE OF INVENTION:** FLASH MEMORY DEVICE AND MANUFACTURING METHOD OF THE SAME

**APPLN. TYPE** | **SMALL ENTITY** | **ISSUE FEE DUE** | **PUBLICATION FEE DUE** | **PREV. PAID ISSUE FEE** | **TOTAL FEE(S) DUE** | **DATE DUE**
--- | --- | --- | --- | --- | --- | ---
nonprovisional | NO | $1740 | $300 | $0 | $2040 | 01/11/2012

**EXAMINER** | **ART UNIT** | **CLASS-SUBCLASS**
--- | --- | ---
PHAM, HOAI V | 2892 | 257-315000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.307).

- Change of correspondence address (or Change of Correspondence Address form PT/0SB/122) attached.

- "Fee Address" indication (or "Fee Address" Indication form PT/0SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

**PLEASE NOTE:** Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

A. NAME OF ASSIGNEE

B. RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent):

- Individual
- Corporation or other private group entity
- Government

4a. The following fee(s) are submitted:

- Issue Fee
- Publication Fee (No small entity discount permitted)
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Date ________________________________

Typed or printed name ________________________________

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Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 143 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 143 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

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Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.
Notice of Allowability

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. □ This communication is responsive to 8/10/2011.

2. □ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. □ The allowed claim(s) is/are 5 and 7-11.

4. □ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) □ All   b) □ Some*   c) □ None of the:
      1. □ Certified copies of the priority documents have been received.
      2. □ Certified copies of the priority documents have been received in Application No. ______.
      3. □ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: ______.

Applicant has THREE MONTHS FROM THE MAILING DATE of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. □ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. □ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) □ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached 1) □ hereto or 2) □ to Paper No./Mail Date ______.
   (b) □ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ______.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. □ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)
3. □ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date ______
   Paper No./Mail Date ______
4. □ Examiner's Comment Regarding Requirement for Deposit of Biological Material 7. □ Examiner's Amendment/Comment
   8. □ Examiner's Statement of Reasons for Allowance
   9. □ Other ______.

/HOAI V PHAM/
Primary Examiner, Art Unit 2892

U.S. Patent and Trademark Office
PTOL-37 (Rev. 03-11) Notice of Allowability Part of Paper No./Mail Date 20110925
DETAILED ACTION

Election/Restrictions

1. Applicant’s election without traverse of claims 5-12 in the reply filed on 08/10/2011 is acknowledged.

Examiner’s amendment

2. An examiner’s amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. This application is in condition for allowance except for the presence of claims 1-4 non-elected without traverse. Accordingly, claims 1-4 have been cancelled.

4. The application has been amended as follows:

In the claims:

Cancel claims 1-4.

Allowable Subject Matter

5. Claims 5 and 7-11 are allowed.

6. The following is an examiner’s statement of reasons for allowance: the prior of record fails to show forming a source LDD region in the substrate between the first and second memory gates through an ion implantation process; forming a second polysilicon layer on an entire surface of the substrate formed with the oxide layer;
etching the second polysilicon layer to form a floating poly on inner sidewalls of the first and second memory gates, respectively, and first and second select gate on respective outer sidewalls of the first and second memory gates while having the characteristics as recited in claim 5.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HOAI V. PHAM whose telephone number is (571)272-1715. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Thao Xuan Le can be reached on 571-272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.
**Notice of References Cited**

<table>
<thead>
<tr>
<th>*</th>
<th>Document Number</th>
<th>Date MM-YYYY</th>
<th>Name</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>US-7,718,488</td>
<td>05-2010</td>
<td>Chen et al.</td>
<td>438/257</td>
</tr>
<tr>
<td>B</td>
<td>US-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C</td>
<td>US-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>US-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>US-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F</td>
<td>US-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>G</td>
<td>US-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>US-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I</td>
<td>US-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>J</td>
<td>US-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>K</td>
<td>US-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>US-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M</td>
<td>US-</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**FOREIGN PATENT DOCUMENTS**

<table>
<thead>
<tr>
<th>*</th>
<th>Document Number</th>
<th>Date MM-YYYY</th>
<th>Country</th>
<th>Name</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>O</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>P</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Q</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NON-PATENT DOCUMENTS**

<table>
<thead>
<tr>
<th>*</th>
<th>Document Number</th>
<th>Date MM-YYYY</th>
<th>Country Code-Number-Kind Code</th>
<th>Name</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>U</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>W</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.*

U.S. Patent and Trademark Office
PTO-892 (Rev. 01-2001)
**Issue Classification**

<table>
<thead>
<tr>
<th>Application/Control No.</th>
<th>Applicant(s)/Patent Under Reexamination</th>
</tr>
</thead>
<tbody>
<tr>
<td>12641432</td>
<td>KWON, YOUNG JUN</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Examiner</th>
<th>Art Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>HOAI V PHAM</td>
<td>2892</td>
</tr>
</tbody>
</table>

**ORIGINAL**

<table>
<thead>
<tr>
<th>CLASS</th>
<th>SUBCLASS</th>
</tr>
</thead>
<tbody>
<tr>
<td>438</td>
<td>201</td>
</tr>
</tbody>
</table>

**INTERNATIONAL CLASSIFICATION**

<table>
<thead>
<tr>
<th>CLAIMED</th>
<th>NON-CLAIMED</th>
</tr>
</thead>
<tbody>
<tr>
<td>H 0 1 L</td>
<td>21 / 0220 (2006.01.01)</td>
</tr>
</tbody>
</table>

**CROSS REFERENCE(S)**

<table>
<thead>
<tr>
<th>CLASS</th>
<th>SUBCLASS (ONE SUBCLASS PER BLOCK)</th>
</tr>
</thead>
<tbody>
<tr>
<td>438</td>
<td>211 257</td>
</tr>
<tr>
<td>257</td>
<td>E21179</td>
</tr>
</tbody>
</table>

**Claims renumbered in the same order as presented by applicant**

- Final
- Original

<table>
<thead>
<tr>
<th>1</th>
<th>5</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>7</td>
</tr>
<tr>
<td>3</td>
<td>8</td>
</tr>
<tr>
<td>4</td>
<td>9</td>
</tr>
<tr>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>6</td>
<td>11</td>
</tr>
</tbody>
</table>

**NONE**

<table>
<thead>
<tr>
<th>(Assistant Examiner)</th>
<th>(Date)</th>
<th>Total Claims Allowed:</th>
</tr>
</thead>
<tbody>
<tr>
<td>/HOAI V PHAM/ Primary Examiner. Art Unit 2892</td>
<td>09/25/2011</td>
<td>6</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>(Primary Examiner)</th>
<th>(Date)</th>
<th>O.G. Print Claim(s)</th>
<th>O.G. Print Figure</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>2</td>
</tr>
</tbody>
</table>

U.S. Patent and Trademark Office

Part of Paper No. 20110225
BIB DATA SHEET

CONFIRMATION NO. 1608

<table>
<thead>
<tr>
<th>SERIAL NUMBER</th>
<th>FILING or 371(c) RULE</th>
<th>CLASS</th>
<th>GROUP ART UNIT</th>
<th>ATTORNEY DOCKET NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>12/641,432</td>
<td>12/18/2009</td>
<td>257</td>
<td>2892</td>
<td>SUN.DH.627</td>
</tr>
</tbody>
</table>

APPLICANTS
Young Jun Kwon, Chungbuk, KOREA, REPUBLIC OF;

** CONTINUING DATA ***********************

** FOREIGN APPLICATIONS ***********************
REPUBLIC OF KOREA 10-2008-0138887 12/31/2008

** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **
12/31/2009

Foreign Priority claimed: Yes No
35 USC 119(a-d) conditions met: Yes No
Met after Allowance: Yes No

STATE OR COUNTRY: KOREA, REPUBLIC OF
SHEETS: 14
DRAWINGS: 12
TOTAL CLAIMS: 2
INDEPENDENT CLAIMS: 2

ADDRESS
SALIWANCHIK, LLOYD & EISENSCHENK
A PROFESSIONAL ASSOCIATION
PO Box 142950
GAINESVILLE, FL 32614
UNITED STATES

TITLE
FLASH MEMORY DEVICE AND MANUFACTURING METHOD OF THE SAME

FILING FEE RECEIVED
1090

FEES: Authority has been given in Paper No.__________ to charge/credit DEPOSIT ACCOUNT No.__________ for following:

- [ ] All Fees
- [ ] 1.16 Fees (Filing)
- [ ] 1.17 Fees (Processing Ext. of time)
- [ ] 1.18 Fees (Issue)
- [ ] Other __________
- [ ] Credit
**Search Notes**

<table>
<thead>
<tr>
<th>Application/Control No.</th>
<th>Applicant(s)/Patent Under Reexamination</th>
</tr>
</thead>
<tbody>
<tr>
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</tr>
</tbody>
</table>

<table>
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<tr>
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<th>Art Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>HOAI V PHAM</td>
<td>2892</td>
</tr>
</tbody>
</table>

**SEARCHED**

<table>
<thead>
<tr>
<th>Class</th>
<th>Subclass</th>
<th>Date</th>
<th>Examiner</th>
</tr>
</thead>
<tbody>
<tr>
<td>438</td>
<td>201,211,257,593</td>
<td>09/23/2011</td>
<td>HP</td>
</tr>
</tbody>
</table>

**SEARCH NOTES**

<table>
<thead>
<tr>
<th>Search Notes</th>
<th>Date</th>
<th>Examiner</th>
</tr>
</thead>
</table>

**INTERFERENCE SEARCH**

<table>
<thead>
<tr>
<th>Class</th>
<th>Subclass</th>
<th>Date</th>
<th>Examiner</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>interference searched printout history</td>
<td>09/23/2011</td>
<td>HP</td>
</tr>
</tbody>
</table>
## Index of Claims

<table>
<thead>
<tr>
<th>Application/Control No.</th>
<th>Applicant(s)/Patent Under Reexamination</th>
</tr>
</thead>
<tbody>
<tr>
<td>12641432</td>
<td>KWON, YOUNG JUN</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Examiner</th>
<th>Art Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>HOAI V PHAM</td>
<td>2892</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>✓</th>
<th>Rejected</th>
</tr>
</thead>
<tbody>
<tr>
<td>=</td>
<td>Allowed</td>
</tr>
<tr>
<td>-</td>
<td>Cancelled</td>
</tr>
<tr>
<td>÷</td>
<td>Restricted</td>
</tr>
<tr>
<td>N</td>
<td>Non-Elected</td>
</tr>
<tr>
<td>I</td>
<td>Interference</td>
</tr>
<tr>
<td>A</td>
<td>Appeal</td>
</tr>
<tr>
<td>O</td>
<td>Objected</td>
</tr>
</tbody>
</table>

☐ Claims renumbered in the same order as presented by applicant

<table>
<thead>
<tr>
<th>CLAIM</th>
<th>DATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Final</td>
<td>Original</td>
</tr>
<tr>
<td>1</td>
<td>+</td>
</tr>
<tr>
<td>2</td>
<td>+</td>
</tr>
<tr>
<td>3</td>
<td>+</td>
</tr>
<tr>
<td>4</td>
<td>+</td>
</tr>
<tr>
<td>5</td>
<td>+</td>
</tr>
<tr>
<td>6</td>
<td>+</td>
</tr>
<tr>
<td>7</td>
<td>+</td>
</tr>
<tr>
<td>8</td>
<td>+</td>
</tr>
<tr>
<td>9</td>
<td>+</td>
</tr>
<tr>
<td>10</td>
<td>+</td>
</tr>
<tr>
<td>11</td>
<td>+</td>
</tr>
<tr>
<td>12</td>
<td>+</td>
</tr>
</tbody>
</table>
### EAST Search History

**EAST Search History (Interference)**

<table>
<thead>
<tr>
<th>Ref #</th>
<th>Hits</th>
<th>Search Query</th>
<th>DBs</th>
<th>Default Operator</th>
<th>Plurals</th>
<th>Time Stamp</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1</td>
<td>2389</td>
<td>select adjgate.clm.</td>
<td>US-PGPUB; USPAT; UPAD</td>
<td>OR</td>
<td>ON</td>
<td>2011/09/23 13:45</td>
</tr>
<tr>
<td>L2</td>
<td>1101</td>
<td>floating.clm. and 1</td>
<td>US-PGPUB; USPAT; UPAD</td>
<td>OR</td>
<td>ON</td>
<td>2011/09/23 13:46</td>
</tr>
<tr>
<td>L3</td>
<td>830</td>
<td>source.clm. and 2</td>
<td>US-PGPUB; USPAT; UPAD</td>
<td>OR</td>
<td>ON</td>
<td>2011/09/23 13:46</td>
</tr>
<tr>
<td>L4</td>
<td>690</td>
<td>drain.clm. and 3</td>
<td>US-PGPUB; USPAT; UPAD</td>
<td>OR</td>
<td>ON</td>
<td>2011/09/23 13:47</td>
</tr>
<tr>
<td>L5</td>
<td>524</td>
<td>substrate.clm. and 4</td>
<td>US-PGPUB; USPAT; UPAD</td>
<td>OR</td>
<td>ON</td>
<td>2011/09/23 13:47</td>
</tr>
<tr>
<td>L6</td>
<td>180</td>
<td>polysilicon.clm. and 5</td>
<td>US-PGPUB; USPAT; UPAD</td>
<td>OR</td>
<td>ON</td>
<td>2011/09/23 13:47</td>
</tr>
<tr>
<td>L7</td>
<td>54</td>
<td>metal.clm. and 6</td>
<td>US-PGPUB; USPAT; UPAD</td>
<td>OR</td>
<td>ON</td>
<td>2011/09/23 13:48</td>
</tr>
</tbody>
</table>

9/23/2011 1:48:56 PM
C: \ Users\ hpham4\ Documents\ EAST\ Workspaces\ Default EAST Workspace
1600x1200.wsp
I hereby certify that this correspondence is being electronically transmitted via EFS to the United States Patent and Trademark Office on August 10, 2011.

Jeff Lloyd, Patent Attorney, Reg. No. 35,589

ELECTION UNDER 37 C.F.R. § 121 AND PRELIMINARY AMENDMENT
Examining Group 2892
Patent Application
Docket No. SUN.DH.627
Serial No. 12/641,432

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Examiner : Hoai V. Pham
Art Unit : 2892
Applicants : Young Jun Kwon
Serial No. : 12/641,432
Filed : December 18, 2009
Conf. No. : 1608
For : Flash Memory Device and Manufacturing Method of the Same

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

ELECTION UNDER 35 USC §121 AND PRELIMINARY AMENDMENT

Sir:

In response to the written Restriction Requirement dated July 11, 2011 in the patent application identified above, Applicants hereby elect to prosecute the invention of Group II (claims 5-12) without traverse.

Prior to examination, Applicants respectfully request that the subject application be amended as follows:

J:\SUN\D1\627\Amnd\Election-PreAmnd.doc\jrr
In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Withdrawn) A flash memory device comprising:
   first and second memory gates adjacently disposed on a substrate;
   a floating poly between the first and second memory gates;
   first and second select gates at respective outer sides of the first and second memory gates;
   an oxide layer between the first memory gate and the first select gate and between the second memory gate and the second select gate;
   a drain region in the substrate at outer sides of the first and second select gates;
   a source region in the substrate between the first and second memory gates; and
   a metal contact on each of the drain region and the source region.

2. (Withdrawn) The flash memory device of claim 1, wherein the oxide layer is further disposed between the first and second select gates and the substrate.

3. (Withdrawn) The flash memory device of claim 1, wherein the oxide layer serves as a gate oxide layer for the first and second select gates.

4. (Withdrawn) The flash memory device of claim 1, further comprising a halo ion implantation region and an LDD ion implantation region in the substrate between the first and second memory gates.

5. (Currently Amended) A method for manufacturing a flash memory device, the method comprising:
   forming first and second memory gates on a substrate;
   forming a third oxide layer on an entire surface of the substrate formed with the first and second memory gates;
forming a source LDD region in the substrate between the first and second memory gates through an ion implantation process;

forming a second polysilicon layer on an entire surface of the substrate formed with the oxide layer;

etching the second polysilicon layer to form a floating poly on inner sidewalls of the first and second memory gates, respectively, and first and second select gates on respective outer sidewalls of the first and second memory gates;

forming a floating poly between the first and second memory gates;

forming first and second select gates at respective outer sides of the first and second memory gates;

forming a drain region in the substrate at outer sides of the first and second select gates;

forming a source region in the substrate between the first and second memory gates; and

forming a metal contact on each of the drain region and the source region.

6. (Canceled)

7. (Currently Amended) The method of claim 6 claim 5, wherein the forming of the floating poly and the forming of the first and second select gates are simultaneously achieved by the etching of the second polysilicon layer.

8. (Original) The method of claim 7, wherein the etching of the second polysilicon layer forms the floating poly and the first and second select gates through a self-align scheme.

9. (Original) The method of claim 7, further comprising forming a peripheral gate poly simultaneously with the forming of the floating poly and the forming of the first and second select gates.
10. (Original) The method of claim 5, further comprising forming a source and drain of a transistor in a peripheral region simultaneously with an ion implantation process for forming the drain region at the outer sides of the first and second select gates.

11. (Original) The method of claim 5, wherein the forming of the first and second memory gates on the substrate includes:
   sequentially forming a first oxide layer, a first nitride layer, a second oxide layer and a first polysilicon layer on the substrate; and
   pattern the first oxide layer, the first nitride layer, the second oxide layer and the first polysilicon layer to form the first and second memory gates adjacently disposed on the substrate.

12. (Canceled)
Remarks

Claims 1-12 are pending in the subject application. Claims 5 and 7 are amended; claims 6 and 12 are canceled. No new matter is introduced by these amendments. Upon entry of these amendments, claims 5 and 7-11 will be before the Examiner for consideration; claims 1-4 are withdrawn. Favorable consideration of the pending claims is respectfully requested.

Applicants invite the Examiner to call the undersigned if clarification is needed on any of this response, or if the Examiner believes a telephonic interview would expedite the prosecution of the subject application to completion.

The Commissioner is hereby authorized to charge any fees under 37 CFR §§1.16 or 1.17 as required by this paper to Deposit Account No. 19-0065.

Respectfully submitted,

Jeff Lloyd
Patent Attorney
Registration No. 35,589
Phone No.: 352-375-8100
Fax No.: 352-372-5800
Address: Saliwanchik, Lloyd & Eisenschenk
A Professional Association
P.O. Box 142950
Gainesville, FL 32614-2950

JL/jrr
<table>
<thead>
<tr>
<th>Document Number</th>
<th>Document Description</th>
<th>File Name</th>
<th>File Size(Bytes)/Message Digest</th>
<th>Multi Part/.zip</th>
<th>Pages (if appl.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Election-PreAmnd.pdf</td>
<td>295716</td>
<td>yes</td>
<td>5</td>
<td></td>
</tr>
</tbody>
</table>
### Multipart Description/PDF files in .zip description

<table>
<thead>
<tr>
<th>Document Description</th>
<th>Start</th>
<th>End</th>
</tr>
</thead>
<tbody>
<tr>
<td>Response to Election / Restriction Filed</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Claims</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>Applicant Arguments/Remarks Made in an Amendment</td>
<td>5</td>
<td>5</td>
</tr>
</tbody>
</table>

**Warnings:**

**Information:**

| Total Files Size (in bytes) | 295716 |

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/OE/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.
### PATENT APPLICATION FEE DETERMINATION RECORD

**APPLICATION AS FILED – PART I**

<table>
<thead>
<tr>
<th>(Column 1)</th>
<th>(Column 2)</th>
<th>SMALL ENTITY [ ] OR OTHER THAN SMALL ENTITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>FOR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BASIC FEE</td>
<td>NUMBER Filed</td>
<td>NUMBER EXTRA</td>
</tr>
<tr>
<td>Search Fee</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Search Fee</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Examination Fee</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Total Claims</td>
<td></td>
<td>*</td>
</tr>
<tr>
<td>Independent Claims</td>
<td></td>
<td>*</td>
</tr>
<tr>
<td>Application Size Fee</td>
<td></td>
<td>*</td>
</tr>
</tbody>
</table>

* If the difference in column 1 is less than zero, enter "0" in column 2.

### APPLICATION AS AMENDED – PART II

<table>
<thead>
<tr>
<th>AMENDMENT</th>
<th>(Column 1)</th>
<th>(Column 2)</th>
<th>(Column 3)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>08/10/2011</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Claims Remaining After Amendment</td>
<td>HIGHEST NUMBER PREVIOUSLY PAID FOR</td>
<td>PRESENT EXTRA</td>
<td></td>
</tr>
<tr>
<td>Total (37 CFR 1.16(k))</td>
<td>Minus</td>
<td>** 20</td>
<td>* 0</td>
</tr>
<tr>
<td>Independent (37 CFR 1.16(n))</td>
<td>Minus</td>
<td>** 3</td>
<td>* 0</td>
</tr>
</tbody>
</table>

**Application Size Fee (37 CFR 1.16(s))**

**First Presentation of Multiple Dependent Claim (37 CFR 1.16(j))**

### AMENDMENT

<table>
<thead>
<tr>
<th>(Column 1)</th>
<th>(Column 2)</th>
<th>(Column 3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Claims Remaining After Amendment</td>
<td>HIGHEST NUMBER PREVIOUSLY PAID FOR</td>
<td>PRESENT EXTRA</td>
</tr>
<tr>
<td>Total (37 CFR 1.16(k))</td>
<td>Minus</td>
<td>**</td>
</tr>
<tr>
<td>Independent (37 CFR 1.16(n))</td>
<td>Minus</td>
<td>**</td>
</tr>
</tbody>
</table>

**Application Size Fee (37 CFR 1.16(s))**

**First Presentation of Multiple Dependent Claim (37 CFR 1.16(j))**

---

Legal Instrument Examiner: JULIET MCMILLAN/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22314-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22314-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.
Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

euspto@slepatents.com
**Office Action Summary**

<table>
<thead>
<tr>
<th>Application No.</th>
<th>Applicant(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>12/641,432</td>
<td>KWON, YOUNG JUN</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Examiner</th>
<th>Art Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>HOAI V. PHAM</td>
<td>2892</td>
</tr>
</tbody>
</table>

---

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) [ ] Responsive to communication(s) filed on **18 December 2009**

2a) [ ] This action is FINAL.  
2b) [ ] This action is non-final.

3) [ ] Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) [ ] Claim(s) **1-12** is/are pending in the application.

4a) Of the above claim(s) ______ is/are withdrawn from consideration.

5) [ ] Claim(s) ______ is/are allowed.

6) [ ] Claim(s) ______ is/are rejected.

7) [ ] Claim(s) ______ is/are objected to.

8) [ ] Claim(s) **1-12** are subject to restriction and/or election requirement.

**Application Papers**

9) [ ] The specification is objected to by the Examiner.

10) [ ] The drawing(s) filed on ______ is/are:  
     a) [ ] accepted or b) [ ] objected to by the Examiner.
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) [ ] The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12) [ ] Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a) [ ] All  
   b) [ ] Some *  
   c) [ ] None of:

   1. [ ] Certified copies of the priority documents have been received.
   2. [ ] Certified copies of the priority documents have been received in Application No. ______.
   3. [ ] Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) [ ] Notice of References Cited (PTO-892)

2) [ ] Notice of Draftsman’s Patent Drawing Review (PTO-948)

3) [ ] Information Disclosure Statement(s) (PTO/SB/08)  
   Paper No(s)/Mail Date ______.

4) [ ] Interview Summary (PTO-413)  
   Paper No(s)/Mail Date ______.

5) [ ] Notice of Informal Patent Application

6) [ ] Other: _____.

U.S. Patent and Trademark Office  
PTOL-326 (Rev. 08-06)  
Office Action Summary  
Part of Paper No./Mail Date 20110702
DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:
   I. Claims 1-4, drawn to a semiconductor device, classified in class 257, subclass 315.
   II. Claims 5-12, drawn to a method of making a semiconductor device, classified in class 438, subclass 201.

2. The inventions are distinct, each from the other because of the following reasons:

   Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the product as claimed can be made by another and materially different process such as forming a drain region in the substrate before forming the first and second select gates.

3. Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and examination burden if restriction were not required because one or more of the following reasons apply:

   (a) the inventions have acquired a separate status in the art in view of their different classification;
(b) the inventions have acquired a separate status in the art due to their recognized divergent subject matter;

(c) the inventions require a different field of search (for example, searching different classes/subclasses or electronic resources, or employing different search queries);

(d) the prior art applicable to one invention would not likely be applicable to another invention;

(e) the inventions are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a invention to be examined even though the requirement may be traversed (37 CFR 1.143) and (ii) identification of the claims encompassing the elected invention.

4. The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected invention.
5. If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

6. Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

7. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

8. The examiner has required restriction between product and process claims. Where applicant elects claims directed to the product, and the product claims are subsequently found allowable, withdrawn process claims that depend from or otherwise require all the limitations of the allowable product claim will be considered for rejoinder. All claims directed to a nonelected process invention must require all the limitations of an allowable product claim for that process invention to be rejoined.

9. In the event of rejoinder, the requirement for restriction between the product claims and the rejoined process claims will be withdrawn, and the rejoined process claims will be fully examined for patentability in accordance with 37 CFR 1.104. Thus, to
be allowable, the rejoined claims must meet all criteria for patentability including the requirements of 35 U.S.C. 101, 102, 103 and 112. Until all claims to the elected product are found allowable, an otherwise proper restriction requirement between product claims and process claims may be maintained. Withdrawn process claims that are not commensurate in scope with an allowable product claim will not be rejoined. See MPEP § 821.04(b). Additionally, in order to retain the right to rejoinder in accordance with the above policy, applicant is advised that the process claims should be amended during prosecution to require the limitations of the product claims. **Failure to do so may result in a loss of the right to rejoinder.** Further, note that the prohibition against double patenting rejections of 35 U.S.C. 121 does not apply where the restriction requirement is withdrawn by the examiner before the patent issues. See MPEP § 804.01.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai v. Pham whose telephone number is 571-272-1715. The examiner can normally be reached on M-F.

11. If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Thao Xuan Le can be reached on 571-272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either PrivatePAIR or PublicPAIR. Status information for unpublished applications is available through PrivatePAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should
you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hoai v Pham/
Primary Examiner, Art Unit 2892
### Index of Claims

| ✓ | Rejected | - | Cancelled | N | Non-Elected | A | Appeal | □ | Claims renumbered in the same order as presented by applicant | ☐ | CPA | ☐ | T.D. | ☐ | R.1.47 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| = | Allowed | + | Restricted | I | Interference | O | Objected | | | | | | | | | | |

<table>
<thead>
<tr>
<th>CLAIM</th>
<th>DATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Final</td>
<td>Original</td>
</tr>
<tr>
<td>1</td>
<td>+</td>
</tr>
<tr>
<td>2</td>
<td>+</td>
</tr>
<tr>
<td>3</td>
<td>+</td>
</tr>
<tr>
<td>4</td>
<td>+</td>
</tr>
<tr>
<td>5</td>
<td>+</td>
</tr>
<tr>
<td>6</td>
<td>+</td>
</tr>
<tr>
<td>7</td>
<td>+</td>
</tr>
<tr>
<td>8</td>
<td>+</td>
</tr>
<tr>
<td>9</td>
<td>+</td>
</tr>
<tr>
<td>10</td>
<td>+</td>
</tr>
<tr>
<td>11</td>
<td>+</td>
</tr>
<tr>
<td>12</td>
<td>+</td>
</tr>
</tbody>
</table>
TITLE: FLASH MEMORY DEVICE AND MANUFACTURING METHOD OF THE SAME

Publication No: US-2010-0163966-A1
Publication Date: 07/01/2010

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publicly available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101
This is to certify that the following application annexed hereto is a true copy from the records of the Korean Intellectual Property Office.

Application Number: 10-2008-0138887

Filing Date: DEC. 31, 2008

Applicant(s): Dongbu HiTek Co., Ltd.
제출 일자 : 2008-12-31

【서지사항】
【서류명】 특허출원서
【참조번호】 2449
【출원구분】 특허출원
【출원인】
【명칭】 주식회사 동부하이텍
【출원인코드】 1-1998-000857-5
【대리인】
【성명】 허용록
【대리인코드】 9-1998-000616-9
【포괄위임등록번호】 2007-040671-5
【발명의 국문명칭】 플래시메모리 소자 및 그 제조 방법
【발명의 영문명칭】 Flash memory device and manufacturing method the same
【발명자】
【성명】 권영준
【성명의 영문표기】 KWON, YOUNG JUN
【주민등록번호】 800926-1XXXXXX
【우편번호】 369-854
【주소】 충청북도 음성군 감곡면 오항리 818-2 영하이초힐라
102-502
【국적】 KR
위와 같이 특허청장에게 제출합니다.

대리인
허용록 (인)

【수수료】
【출원료】 0 면 38,000 원
제출 일자 : 2008-12-31

【가산출원료】 27 면 0 원
【우선권추천료】 0 건 0 원
【상사청구료】 0 항 0 원
【합계】 38,000 원
【요약】

실시에는 플래시메모리 소자 및 그 제조 방법에 관한 것이다.

실시에 따른 플래시메모리 소자는 기판 상에 형성된 제1 메모리 케이트, 제2 메모리 케이트; 상기 제1, 제2 메모리 케이트 내측면에 형성된 플로팅 폴리; 상기 제1, 제2 메모리 케이트 외측면에 각각 형성된 제1, 제2 선택 케이트; 상기 제1, 제2 메모리 케이트와 상기 제1, 제2 선택 케이트 사이에 형성된 제3 산화막; 상기 제1, 제2 선택 케이트 외측의 상기 기판에 형성된 드레인영역, 상기 제1, 제2 메모리 케이트 내측의 상기 기판에 형성된 소스영역 및 상기 드레인영역과 상기 소스영역 상에 형성된 메탈컨텍;을 포함한다.

【대표도】

도 2

【색인어】

비휘발성 메모리 소자, SONOS(Silicon-Oxide-Nitride-Oxide-Silicon)
[영상서]

[발명의 명칭]
플래시메모리 소자 및 그 제조 방법(Flash memory device and manufacturing method the same)

[발명의 상세한 설명]

[기술분야]

<1> 실시에는 플래시메모리 소자 및 그 제조 방법에 관한 것이다.

[배경기술]

<2> 플래시메모리 소자는 전원이 커지더라도 저장된 데이터가 손상되지 않는 비휘발성 기억매체이면서도 데이터의 기록, 읽기, 삭제 등의 처리 속도가 비교적 높다는 장점이 있다.

<3> 이에 따라, 플래시메모리 소자는 PC의 Bios용, 셋탑 박스, 프린터 및 네트워크 서버 등의 데이터 저장용으로 널리 사용되고 있으며 최근에는 디지털 카메라와 휴대폰 등에서도 많이 이용되고 있다.

<4> 플래시메모리 소자에 있어서, SONOS(Silicon-Oxide-Nitride-Oxide-Silicon) 구조를 이용한 반도체 소자가 사용되고 있다.

<5> SONOS 메모리소자는 게이트전압에 의해 설리콘 위의 얇은 산화막을 전하가 터널링하여 평행의 다결정 설리콘을 사용한 부유게이트(Floating Gate) 대신 설리콘 결화막내의 트랩에 주입 또는 트랩으로부터 이환되는 에너지층을 이용하는 전하
트랩형 소자이다.

도 1a 뒷지 도 1c는 종래기술에 의한 플레시메모리 소자의 공정단면도이다.

도 1a와 같이 포토 및 식각(Photo and etch)을 이용하여 스플릿 선택게이트
(split select gate)를 디파인(define)하는 경우, 포토공정의 오버레이 미스알라인
(overlay misalign) 때문에 서로 다른 선택게이트 길이(select gate length)(L1≠
L2)를 가질수록 좌측셀(A cell)과 우측셀(B cell)이 서로 다른 특성을 나타내는
문제가 있다.

또한, 도 1b와 같이 로컬니트라이드(Local nitride)을 메모리사이트(Memory
site)로 이용하는 경우, 포토 및 식각을 이용하여 디파인하는 경우 포토(photo)의
CD 베리에이션(variation) 및 오버레이 미스알라인에 의한 서로 다른 절화막 길이
(nitride length)(L3≠L4) 및 선택게이트 길이(L1≠L2)를 가지게 되고, 이로 인하
여 좌측셀(A cell)과 우측셀(B cell)의 특성 베리에이션(variation)이 커지게 되는
문제가 있다.

또한, 종래기술은 도 1c와 같이 소스영역의 폴리(디미지)를 액티브와 메모리
게이트 폴리에 데미지(damage) 없이 제거함에 어려움이 있다.

【발명의 내용】

【해결하고자 하는 과제】

실시에선 자기 정렬형 SONOS(Silicon-Oxide-Nitride-Oxide-Silicon)구조의
플레시메모리 소자에 관한 것으로서, 기존의 포토 및 식각을 이용한 셀(Cell) 형성
방법을 사용하는 대신 자기 정렬 더블 스페이서(self-align double spacer)공정을 이용함으로써 기존의 SONOS 공정(Process)이 갖는 CD, 오버레이(Overlay) 문제에 기인한 셀의 균일성(cell uniformity) 문제가 특성저하를 극복할 수 있는 폴라세미
모러 소자 및 그 제조 방법을 제공하고자 한다.

또한, 설계에는 소스 사이드(Source side)의 면적을 늘리고, 소스(Source) 이온주입 후 스페이서 폴리Spacer Poly) 형성공정을 진행하여 소스 사이드(Source side)의 액티브 데미지(Active damage) 없이 텅질 폴리(gap-fill poly)를 제거하기 위한 노력을 덜 수 있다. 그리고 이와 같이 공정이 진행하게 되면 LDD Length를 폴리(Poly) 형성 두께에 따라 자연스럽게 증가되게 되고, 이것은 프로그램(Program) 및 제거(Erase) 등작 시 소스(Source)와 드레인(Drain) 간의 전치(Punch) BV를 높일 수 있는 폴라세미모러 소자 및 그 제조 방법을 제공하고자 한다.

【결과 해결 수단】

설계에 따른 폴라세미모러 소자는 기판 상에 형성된 제1 메모리 게이트, 제2 메모리 게이트; 상기 제1, 제2 메모리 게이트 외측면에 형성된 폴리형 폴리; 상기 제1, 제2 메모리 게이트 외측면에 각각 형성된 제1, 제2 선택 게이트; 상기 제1, 제2 메모리 게이트와 상기 제1, 제2 선택 게이트 사이에 형성된 제3 산화막; 상기 제1, 제2 선택 게이트 외측의 상기 기판에 형성된 드레인 영역, 상기 제1, 제2 메모리 게이트 외측의 상기 기판에 형성된 소스 영역; 및 상기 드레인 영역과 상기
소스영역 상에 형성된 메탈컨택을 포함한다.

실험에 따른 플래시에모리 소자의 제조 방법은 기판 상에 제1 메모리 게이트, 제2 메모리 게이트를 형성하는 단계; 상기 제1, 제2 메모리 게이트가 형성된 기판의 전면에 제3 산화막을 형성하는 단계; 상기 제1, 제2 메모리 게이트 내측면에 폴리형 풀리층을 형성하는 단계; 상기 제1, 제2 메모리 게이트 외측면에 각각 제1, 제2 선택 게이트를 형성하는 단계; 상기 제1, 제2 선택 게이트 외측의 상기 기판에 드레인영역을 형성하고, 상기 제1, 제2 메모리 게이트 내측의 상기 기판에 소스영역을 형성하는 단계; 및 상기 드레인영역과 상기 소스영역에 메탈컨택을 형성하는 단계를 포함한다.

【효과】

실험에 따른 플래시에모리 소자 및 그 제조 방법은, 소스(Source) 이온주입공정을 선행하고, 폴리(Poly)형성 및 식각공정을 진행함으로써, 소스(Source) 쪽의 폴리(Poly)는 제거하지 않아도 되므로 소스(Source) 영역의 폴리(Poly)를 태너지(Damage)없이 제거하기 위한 노력과 시간을 덜 수 있으며, 그 공정이 간단하고, 공정 시간(time)을 줄일 수 있어 공정비용을 절감할 수 있다.

또한, 실험에는 셀(Cell)의 소스(Source)에는 Program/Erase 동작 시 High bias가 걸리게 되는데, 위 공정을 진행하게 되면, N+ 전형시 폴리(Poly)가 N+을 풀락킹(blocking)하여 Cell의 소스(Source) 영역의 LDD drift 영역이 넓어지게 되어, Source와 Drain 간의 Punch BV(Breakdown Voltage)도 항상 시킬 수 있다. 즉, Cell
의 Program/Erase 동작 시 High Bias가 인가되는 Source 쪽의 Punch BV가 개선되므로, Cell의 Length를 증가시키지 않고도 Source Drain 간의 Punch BV를 개선할 수 있다.

아래, 실시에는 질화막(Nitride)과 선택게이트(select gate)의 length에 따라 cell 특성의 민감하게 바뀌는데, 기존의 기술들은 질화막과 선택게이트의 length를 포토 및 식각(Photo and etch)에 의하여 컨트롤(control) 하지만 실시에는 자기 정렬형 공정을 이용하여 기존 기술이 갖는 CD, 오버레이 베리에이션(overlay variation)에 기인한 문제를 해결할 수 있으면서 cell 특성의 균일성(uniformity) 측면에서 더 좋은 특성을 얻을 수 있다.

【발명의 실시를 위한 구체적인 내용】

이하, 실시예를 참조하여 설명하기로 한다.

본 발명에 따른 실시 예의 설명에 있어서, 각 중(목), 영역, 패턴 또는 구조물들이 기판, 각 중(목), 영역, 패드 또는 패턴들의 "상/위(on)" 또는 "아래(under)"에 형성되는 것으로 기재되는 경우에 있어, "상/위(on)"와 "아래(under)"는 "직접(directly)" 또는 "다른 중을 개제하여 (indirectly)" 형성하는 것을 모두 포함한다. 또한 각 중의 상/위 또는 아래에 대한 기준은 도면을 기준으로 설명한다.

도면에서 각층의 두께나 크기는 설명의 편의 및 명확성을 위하여 과장되거나 생략되거나 또는 전략적으로 도시되었다. 또한 각 구성요소의 크기는 설계크기를
전적으로 반영하는 것은 아니다.

(실시예)

도 2는 실시예에 따른 플래시메모리 소자의 단면도이다.

실시예에 따른 플래시메모리 소자는 기판(10) 상에 형성된 제1 메모리 케이트(20a), 제2 메모리 케이트(20b); 상기 제1, 제2 메모리 케이트(20a, 20b) 내측면에 형성된 플로팅 폴리(29a, 29b); 상기 제1, 제2 메모리 케이트(20a, 20b) 외측면에 각각 형성된 제1, 제2 선택 케이트(30a, 30b); 상기 제1, 제2 메모리 케이트(20a, 20b)와 상기 제1, 제2 선택 케이트(30a, 30b) 사이에 형성된 제3 산화막(25); 상기 제1, 제2 선택 케이트(30a, 30b) 외측의 상기 기판(10)에 형성된 드레인영역, 상기 제1, 제2 메모리 케이트(20a, 20b) 내측의 상기 기판에 형성된 소스 영역 및 상기 드레인영역과 상기 소스영역 상에 형성된 메탈연결(36);을 포함한다. 도 1에서 미설명된 도면부호는 이하 제조방법에서 설명하기로 한다.

실시예에 따른 플래시메모리 소자 및 그 제조 방법은, 소스(Source) 이온주입공정을 선 진행하고, 폴리(Poly)형성 및 시각공정을 진행함으로써, 소스(Source) 측의 폴리(Poly)는 제거하지 않아도 되므로 소스(Source) 영역의 폴리(Poly)를 테라지(Damage)없이 제거하기 위한 노력과 시간을 할 수 있으며, 그 공정이 간단하고, 공정 시간(time)을 줄일 수 있어 공정비용을 절감할 수 있다.

또한, 실시예는 셀(Cell)의 소스(Source)에는 Program/Erase 동작 시 High bias가 걸리게 되는데, 위 공정을 진행하게 되면, N+ 전행시 폴리(Poly)가 N+을 볼
락킹(blocking)하여 Cell의 소스(Source) 영역의 LDD drift 영역이 넓어지게 되어, Source와 Drain 간의 Punch BV도 항상 시킬 수 있다. 즉, Cell의 Program/Erase 동작 시 High Bias가 인가되는 Source 쪽의 Punch BV가 개설되므로, Cell의 Length를 증가시키지 않고서도 Source Drain 간의 Punch BV를 개선할 수 있다.

또한, 실시에는 질화막(Nitride)과 선택제이트(select gate)의 length에 따라 cell 특성이 미란하게 바뀌는데, 기존의 기술들은 질화막과 선택제이트의 length를 포토 및 식각(Photo and etch)에 의하여 컨트롤(control) 하지만 실시에는 자기 정렬형 공정을 이용하여 기존 기술이 갖는 CD, 오버레이 시리지선(overlay variation)에 기인한 문제를 해결할 수 있도록 cell 특성의 균일성(uniformity) 측면에서 더 좋은 특성을 얻을 수 있다.

이하, 도 3 내지 도 14를 참조하여 실시에 따른 플레이업모티 소자의 제조 방법을 설명한다.

우선, 도 3과 같이, 기판(10)에 소자분리막(12)을 형성하여 활성영역(active area)(11)을 정해한다. 이때, 활성영역(11)에는 페트 산화막(15)이 형성될 수 있다.

다음으로 도 4와 같이, 기판(10)에 제1 이온주입공정을 진행하여 웨(well) 영역(13)을 형성할 수 있다. 예를 들어, 기판(10)이 P형인 경우, N형 이온주입에 의해 N형 웨를 형성할 수 있다. 실시에는 웨 영역(13)이 형성된 기판(10)에 문턱전압(threshold voltage) 조절을 위한 제2 이온주입 영역(미도시)을 진행할 수 있다.
다음으로 도 5와 같이, 폴리산화막(15)을 제거하고 기판(10) 상에 제1 산화막(21), 제1 질화막(22), 제2 산화막(23) 및 제1 폴리실리콘층(24)을 순차적으로 형성한다.

예를 들어, 제1 산화막(21)은 탄널산화막의 기능을 할 수 있으며, 기판(10)에 열처리 공정을 진행하여 약 20~80Å 두께의 SiO₂로 형성되거나, Al₂O₃ 같은 High-K 물질을 CVD(Chemical Vapor Deposition) 또는 ALD(Atomic Layer Deposition) 방식으로 중착시킬 수 있다.

제1 질화막(22)은 전하트램증 역할을 할 수 있으며, CVD 방식으로 약 70~100Å 두께의 Si₃N₄(x,y는 자연수)로 형성될 수 있다.

제2 산화막(23)은 탑옥사이드층(top oxide)으로서 기능할 수 있으며, CVD 방식의 실리콘산화막(SiO₂)으로 형성될 수 있으나 이에 한정되는 것은 아니다.

이후, 제2 산화막(23) 상에 제1 폴리실리콘층(24)을 중착 등의 방법으로 형성한다.

다음으로 도 6과 같이, 제1 산화막(21), 제1 질화막(22), 제2 산화막(23) 및 제1 폴리실리콘층(24)을 캐터링하여 제1 메모리 게이트(20a), 제2 메모리 게이트(20b)를 포함하는 메모리 게이트(20)를 형성한다. 이에 따라 메모리 게이트(20)는 SONOS(Silicon-Oxide-Nitride-Oxide-Silicon)구조를 이룰 수 있다.

예를 들어, 제1 폴리실리콘층(24) 상에 제1 토토레지스트 패턴(미도시)을 이용하여 메모리 게이트가 형성될 부분만 오픈(open)하고 식각공정을 통하여 메모리
게이트(20)를 디바인(define)할 수 있다. 이때 식각 공정은 제1 폴리실리콘층(24)부터 제1 절화막(22)까지 한 번에 식각할 수도 있으며, 제2 산화막(23) 전까지 식각하고, 나머지층은 식각하는 두 단계 식각방식으로 진행할 수도 있다. 후자의 경우 첫 번째 식각 공정에서 제2 산화막(23)에 스탑(stop)하고, 두 번째 식각 공정에서 제2 산화막(23)과 제1 절화막(22)을 식각한다. 두 번째 식각 방식은 건식(Dry) 또는 습식(Wet) 식각 방식을 모두 이용할 수 있다.

다음으로, 7과 같이 제1, 제2 메모리 게이트(20a, 20b)가 형성된 기판(10)의 전면에 제3 산화막(25)을 형성한다.

예를 들어, 메모리 게이트(20)의 영역에 남아있던 터널 산화막인 제1 산화막(21)을 제거한 후 두엽게이트 산화(Dual gate oxide)공정으로 제3 산화막(25)을 열산화 방식으로 형성할 수 있다.

예를 들어, 제3 산화막(25)은 두꺼운 게이트 옥사이드(thick gate oxide)와 얇은 게이트 옥사이드(thin gate oxide)가 합쳐진 산화막이거나, 얇은 게이트 옥사이드(thin gate oxide)가 겔체일 수 있다.

이때, 이후 형성되는 선택게이트(Select Gate oxide)(30a, 30b)는 제3 산화막(25)을 선택 게이트 옥사이드로 공유할 수 있다.

다음으로, 8과 같이 제1 포토레지스트 패턴(41)을 마스크로 제1 메모리 게이트(20a)와 제2 메모리 게이트(20b) 사이의 기판(10)에 HCI(hot carrier injection) 효율을 증가하기 위해 Halo 이온주입영역(Halo Implant Region)(27b)과
소스 LDD(Lightly Doped Drain) 영역(27a)을 형성할 수 있다.

다음으로, 도 9와 같이 제1 포토레지스트 패턴(41)을 제거하고, 소스 LDD 영역(27a)이 형성된 기판(10)의 전면에 제2 폴리실리콘층(28)을 형성한다.

예를 들어, 제1 포토레지스터 패턴(41)을 제거 후 바로 제2 폴리실리콘층(28)을 증착한다.

다음으로, 도 10과 같이 제2 폴리실리콘층(28)을 식각하여 제1, 제2 에모리 게이트(20a, 20b) 내측면에 플로팅 폴리(Floating Poly)(29a, 29b)를 형성하고, 제1, 제2 에모리 게이트(20a, 20b) 외측면에 각각 제1, 제2 선택 게이트(30a, 30b)를 형성한다. 상기 플로팅 폴리는 제1 플로팅 폴리(29a), 제2 플로팅 폴리(29b)를 포함할 수 있다.

예를 들어, 폴리실리콘(Poly silicon) 식각공정을 이용하여, Cell 영역을 전면 식각한다. 이렇게 하면, 제2 폴리실리콘층(28)의 두께에 따라 선택게이트(Select gate)의 Length가 결정되게 된다. 실제로는 종래기술에서 Cell의 미스알라인(mis-aligne) 문제를 자기정렬 방식을 이용하여로써 해결할 수 있다.

또한, 실제로는 플로팅 폴리(29a, 29b)는 미리 source 영역에 대한 LDD 영역 등의 이온주입공정을 진행하였기 때문에 제거되지 않아도 된다. 이렇게 되면 소스 폴리(29a, 29b)를 태미지(Damage)없이 제거하기 위한 노력과 시간을 덜 수 있으며, 드레인(Drain)과 소스(source)간의 Punch BV를 향상시킨다.

이때, 실제로는 선택 게이트 폴리 디바인(Select Gate Poly Define) 시 포
토레지스터(MOS)를 이용하여 패턴링(Patterning)한 후 식각하여 주변영역 게이트 폴리(Peri Gate Poly)를 다이파인(Define)할 수 있다. 또한, 식각공정 시 환성영역에 대미지(Damage)가 발생한 것으로 판명될 때에는 세(S selv)의 선택게이트 폴리 다이파인(Select Gate Poly Define)하기 위한 포토 스텝(Photo step)과 식각공정, 주변영역 게이트 폴리(Peri region Gate Poly)를 다이파인(Define)하기 위한 포토스템(Photo step)과 식각공정을 따로 진행할 수 있다.

다음으로, 도 11과 같이 감광막 패턴(42)을 마스크로 제1, 제2 선택 게이트 (30a, 30b) 외측에 할로 이온주입영역(Halo Implant Region)(32)과 LDD 이온주입영역(31)을 형성한다.

실시에서 LDD 이온주입영역(31)은 주변영역(peri area) 트랜지스터(Transistor)의 LDD 이온주입공정과 동시에 진행할 수 있다.

다음으로, 도 12와 같이 상기 감광막 패턴(42)을 제거하고, 이온주입에 의해 제1, 제2 선택 게이트 (30a, 30b) 외측의 기관(10)에 드레인영역(34)을 형성하고, 제1, 제2 메모리 게이트(20a, 20b) 내측의 기관(10)에 소스영역(25)을 형성한다.

예를 들어, 스페이서(Spacer)(33)를 형성한 후 고농도 N+ 이온주입공장인 소스(Source), 드레인(Drain) 이온주입공정을 진행하여 소스영역(26), 드레인영역(34)을 형성한다. 스페이서(33)은 ONO(Oxide-Nitride-Oxide) 또는 ON(oxid-Nitride)의 구조로 형성될 수 있다.

이때 실시에는 드레인, 소스 이온주입공장을 주변영역(peri area) 트랜지스
터(Transistor)의 소스(Source)와 드레인(Drain) 이온주입공정과 함께 진행할 수 있다.

설시에는 소스영역의 플로팅 폴리(Floating Poly)가 소스, 드레인(Source, Drain) 이온주입 공정 시 블리킹(Blocking) 역할을 하므로 LDD drift 영역(D)이 넓어지게 되는데, 이것은 Source와 Drain 간의 BV를 향상시킨다.

다음으로, 도 13과 같이 살리사이드(35) 공정을 진행한다. 예를 들어, 소스 영역(26), 드레인영역(34), 메모리레이트(20), 플로팅 폴리(29a, 29b) 상의 제3 산화막(25)을 제거 후 기판 전면에 코발트(Co) 동 금속층을 형성하고 열처리를 통해 소스영역(26), 드레인영역(34), 선택체이트(30a, 30b), 메모리레이트(20), 플로팅 폴리(29a, 29b) 상에 살리사이드(35)를 형성할 수 있다.

다음으로, 도 14와 같이 소스영역(26), 드레인영역(34)에 메탈간택(36)과 배선(37)을 형성하는 후공정(Back End Process)을 진행한다.

설시에 따른 플레시메모리 소자 및 그 제조 방법은, 소스(Source) 이온주입공정을 선 진행하고, 폴리(Poly) 형성 및 시각공정을 진행함으로써, 소스(Source) 쪽의 폴리(Poly)는 제거하지 않아도 되므로 소스(Source) 영역의 폴리(Poly)를 내비치(Damage)없이 제거하기 위한 노력과 시간을 들 수 있으며, 그 공정이 간단하고, 공정 시간(time)을 줄일 수 있어 공정비용을 절감할 수 있다.

또한, 설시에는 셀(Cell)의 소스(Source)에는 Program/Erase 동작 시 High bias가 걸리게 되는데, 위 공정을 진행하게 되면, N+ 전형시 폴리(Poly)가 N+을 붙
라김(blocking)하여 Cell의 소스(Source) 영역의 LDD drift 영역이 넓어지게 되어, Source와 Drain 간의 Punch BV도 항상 시킬 수 있다. 즉, Cell의 Program/Erase 동작 시 High Bias가 인가되면 Source 쪽의 Punch BV가 개설되므로, Cell의 Length를 증가시키지 않고서도 Source Drain 간의 Punch BV를 개선할 수 있다.

또한, 실시에는 절화막(Nitride)과 선택게이트(select gate)의 length에 따라 cell 특성이 민감하게 바뀌는데, 기존의 기술들은 절화막과 선택게이트의 length를 포토 및 식각(Photo and etch)에 의하여 컨트롤(control) 하지만 실시에는 자기 정렬형 공정을 이용하여 기존 기술이 갖는 CD. 오버레이 베리에이션(overlay variation)에 기인한 문제를 해결할 수 있으므로 cell 특성의 균일성(uniformity) 측면에서 더 좋은 특성을 얻을 수 있다.

이상에서 설명한 실시에 따른 플래시메모리 소자는 다음과 같이 동작될 수 있으나 이에 한정되는 것은 아니다.

실시에 따른 플래시메모리 소자의 프로그램(program) 동작은 혼 캐리어인 전자(electron)를 발생시키기 위한 바이어스를 인가시키 동작할 수 있다.

그러고, 소거(erase) 동작은 BTBT(Band to Band tunneling)를 형성할 수 있는 조건으로 바이어스를 인가하여, EHP(Electron-Hole Pair)을 형성하여 동작될 수 있다. 이때, 소거 동작은 워드라인(W/L) 단위로 하기 때문에, 선택된(Selected) 셀과 같은 워드라인(W/L)은 모두 소거된다.

즉, 선택되지 않은(Un-selected) 셀이라도 동일한 워드라인(W/L)에 위치하게
되며, 해당 셀은 소기(erase)된다. 또한, 읽기(read) 중간은 드레인 영역에 인가하는 바이어스에 따라 전류(current)가 촉발되는데, 프로그램 상태와 소기 상태의 전류량이 다르므로, 프로그램 상태인지 소거 상태인지 알 수 있게 된다.

이상에서 실시예를 중심으로 설명하였으나 이는 단지 예시일 뿐 본 발명을 한정하는 것이 아니며, 본 발명이 속하는 분야의 통상의 지식을 가진 자라면 본 실시예의 본질적인 특성을 얻어나지 않는 범위에서 이상에 예시되지 않은 여러 가지의 변형과 응용이 가능함을 알 수 있을 것이다. 예를 들면, 실시예에 구체적으로 나타난 각 구성 요소는 변형하여 실시할 수 있는 것이다. 그리고 이러한 변형과 응용에 관계된 차이점들은 참부른 청구 범위에서 규정하는 본 발명의 범위에 포함되는 것으로 해석되어야 할 것이다.
【복합정구범위】

【청구항 1】

기관 상에 형성된 제1 메모리 카이트, 제2 메모리 카이트;
상기 제1, 제2 메모리 카이트 내측면에 형성된 플로팅 폴리;
상기 제1, 제2 메모리 카이트 외측면에 각각 형성된 제1, 제2 선택 카이트;
상기 제1, 제2 메모리 카이트와 상기 제1, 제2 선택 카이트 사이에 형성된 제3 산화막;
상기 제1, 제2 선택 카이트 외측의 상기 기판에 형성된 드레인영역, 상기 제1, 제2 메모리 카이트 내측의 상기 기판에 형성된 소스영역; 및
상기 드레인영역과 상기 소스영역 상에 형성된 베탈진맥;을 포함하는 플래시 메모리 소자.

【청구항 2】

제1 항에 있어서,
상기 제3 산화막은
상기 제1, 제2 선택 카이트와 상기 기판 사이에도 형성된 것을 특징으로 하는 플래시 메모리 소자.

【청구항 3】

제1 항에 있어서,
상기 제3 산화막은
제1, 제2 선택 게이트 옥사이드 기능을 하는 것을 특정으로 하는 플레시메모리 소자.

【참기항 4】

제1 항에 있어서,

상기 제1, 제2 메모리 게이트 사이의 상기 기판에 형성된 할로 이온주입영역과 LDD 이온주입영역을 더 포함하는 것을 특정으로 하는 플레시메모리 소자.

【참기항 5】

기판 상에 제1 메모리 게이트, 제2 메모리 게이트를 형성하는 단계;

상기 제1, 제2 메모리 게이트가 형성된 기판의 전면에 제3 산화막을 형성하는 단계;

상기 제1, 제2 메모리 게이트 내측면에 폴로딩 풀리지를 형성하는 단계;

상기 제1, 제2 메모리 게이트 외측면에 각각 제1, 제2 선택 게이트를 형성하는 단계;

상기 제1, 제2 선택 게이트 외측의 상기 기판에 드레인영역을 형성하고, 상기 제1, 제2 메모리 게이트 내측의 상기 기판에 소스영역을 형성하는 단계; 및 상기 드레인영역과 상기 소스영역에 메탈콘택을 형성하는 단계;를 포함하는 플레시메모리 소자의 제조방법.

【참기항 6】

제5 항에 있어서,
상기 제1, 제2 메모리 게이트 내측면에 플로팅 폴리를 형성하는 단계는,

상기 제3 산화막이 형성된 기판의 전면에 제2 폴리실리콘층을 형성하는 단계:

상기 제2 폴리실리콘층을 식각하여 상기 제1, 제2 메모리 게이트 내측면에
플로팅 폴리를 형성하는 단계;를 포함하는 것을 특징으로 하는 플래시메모리 소자의
의 제조방법.

【청구항 7】

제6 항에 있어서,

상기 플로팅 폴리를 형성하는 단계와 상기 각 제1, 제2 선택 게이트를 형성
하는 단계는 상기 제2 폴리실리콘층을 식각하여 동시에 진행되는 것을 특징으로 하
는 플래시메모리 소자의 제조방법.

【청구항 8】

제7 항에 있어서,

상기 플로팅 폴리를 형성하는 단계와 상기 제1, 제2 선택 게이트를 형성하는
단계는 상기 폴리실리콘층을 식각하여 자기경련 방식으로 형성하는 것을 특징으로 하
는 플래시메모리 소자의 제조방법.

【청구항 9】

제7 항에 있어서,

상기 플로팅 폴리를 형성하는 단계와 상기 제1, 제2 선택 게이트를 형성하는
단계는,

주변영역 게이트 폴리(Peri Gate Poly)를 함께 형성하는 것을 특징으로 하는 플래시메모리 소자의 제조방법.

【참고항 10】

제5 항에 있어서.

장기 제1, 제2 선택 게이트 외측에 드레인영역을 형성하는 단계는

주변영역(peri area) 트랜지스터(Transistor)의 소스(Source)와 드레인(Drain) 이온주입공정과 함께 진행하는 것을 특징으로 하는 플래시메모리 소자의 제조방법.

【참고항 11】

제5 항에 있어서.

장기 기판 상에 제1 메모리 게이트, 제2 메모리 게이트를 형성하는 단계는,

기판 상에 제1 산화막, 제1 절화막, 제2 산화막 및 제1 폴리실리콘층을 순차적으로 형성하는 단계; 및

장기 제1 산화막, 장기 제1 절화막, 장기 제2 산화막 및 장기 제1 폴리실리콘층을 패터닝하여 제1 메모리 게이트, 제2 메모리 게이트를 형성하는 단계;를 포 함하는 것을 특징으로 하는 플래시메모리 소자의 제조방법.

【참고항 12】

제5 항에 있어서.
상기 제1 메모리 게이트와 상기 제2 메모리 게이트 사이의 기판에 이온주입에 의해 소스 LDD 영역을 형성하는 단계를 더 포함하는 것을 특징으로 하는 플래시 메모리 소자의 제조방법.

【도면의 간단한 설명】

<63> 도 1a 내지 도 1c는 종래기술에 의한 플래시메모리 소자의 공정단면도.

<64> 도 2는 실시예에 따른 플래시메모리 소자의 단면도.

<65> 도 3 내지 도 14는 실시예에 따른 플래시메모리 소자의 공정 단면도.
<table>
<thead>
<tr>
<th>APPLICATION NUMBER</th>
<th>FILING or 371(c) DATE</th>
<th>GRP ART UNIT</th>
<th>FIL FEE RECD</th>
<th>ATTY DOCKET NO</th>
<th>TOTAL CLAIMS</th>
<th>IND CLAIMS</th>
</tr>
</thead>
<tbody>
<tr>
<td>12/641,432</td>
<td>12/18/2009</td>
<td>2827</td>
<td>1090</td>
<td>SUN.DH.627</td>
<td>12</td>
<td>2</td>
</tr>
</tbody>
</table>

CONFIRMATION NO. 1608

FILING RECEIPT

23557
SALIWANCHIK LLOYD & SALIWANCHIK
A PROFESSIONAL ASSOCIATION
PO Box 142950
GAINESVILLE, FL 32614

Date Mailed: 01/06/2010

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a “Notice to File Missing Parts” for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections.

Applicant(s)
Young Jun Kwon, Chungbuk, KOREA, REPUBLIC OF;

Power of Attorney: The patent practitioners associated with Customer Number 23557

Domestic Priority data as claimed by applicant

Foreign Applications
REPUBLIC OF KOREA 10-2008-0138887 12/31/2008

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper Request to Retrieve Electronic Priority Application(s) (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 12/31/2009

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is US 12/641,432

Projected Publication Date: 07/01/2010

Non-Publication Request: No

Early Publication Request: No
PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process simplifies the filing of patent applications on the same invention in member countries, but does not result in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED
The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as
set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

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The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

**NOT GRANTED**

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).
The undersigned hereby requests the USPTO retrieve an electronic copy of each of the following foreign applications for which benefit has been claimed under 35 U.S.C. 119(a)-(d) from a foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement:

Please retrieve (check all that apply)

☑ The following applications originally filed in participating offices (only list the Participating Office and the Participating Office Application Number (columns 1 and 2 below)):

☐ The following applications originally filed in non-participating offices (must list the information for all three columns below):

<table>
<thead>
<tr>
<th>1. Participating Office with which the Priority Application, or the Copy, was filed (e.g., EPO)</th>
<th>2. Participating Office Application Number in which the Priority Application, or a Copy, was filed (e.g., 03104132)</th>
<th>3. Non-Participating Office Application Number (Priority Application), if applicable</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1. KR</td>
<td>10-2008-0138887</td>
<td></td>
</tr>
<tr>
<td>2.</td>
<td>12/31/2008</td>
<td></td>
</tr>
<tr>
<td>3.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

This Request to Retrieve Electronic Priority Application(s) (Request) should be filed within the later of four months from the date of filing the above-identified application claiming foreign priority, or sixteen months from the filing date of the foreign application to which priority is claimed.

This Request should be submitted concurrently with the claim for priority, or thereafter. The USPTO will not attempt to retrieve the identified priority application(s) until applicant identifies the indicated priority application(s) on the oath or declaration or an application data sheet in compliance with 37 CFR 1.53(c).

Applicants are advised to consult Private PAIR (accessed through www.uspto.gov) to assure that the retrieval has been successful. The applicant remains ultimately responsible for the submission of the certified copy of the foreign application(s) within the period set forth in 37 CFR 1.55(a) (before the U.S. application issues as a patent) if the USPTO does not timely retrieve the identified priority application(s).

I hereby declare that I have the authority to grant access to the above-identified applications.

[Signature]

Jeff Lloyd

Printed or Typed Name

Patent Attorney

Title

December 18, 2009

Date

352-375-8100

Telephone Number

35,589

Registration Number, if applicable
## Electronic Patent Application Fee Transmittal

<table>
<thead>
<tr>
<th>Application Number:</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Filing Date:</td>
<td></td>
</tr>
<tr>
<td><strong>Title of Invention:</strong></td>
<td>FLASH MEMORY DEVICE AND MANUFACTURING METHOD OF THE SAME</td>
</tr>
<tr>
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</tr>
<tr>
<td>Filer:</td>
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</tr>
<tr>
<td>Attorney Docket Number:</td>
<td>SUN.DH.627</td>
</tr>
</tbody>
</table>

**Filed as Large Entity**

### Utility under 35 USC 111(a) Filing Fees

<table>
<thead>
<tr>
<th>Description</th>
<th>Fee Code</th>
<th>Quantity</th>
<th>Amount</th>
<th>Sub-Total in USD($)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Basic Filing:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Utility application filing</td>
<td>1011</td>
<td>1</td>
<td>330</td>
<td>330</td>
</tr>
<tr>
<td>Utility Search Fee</td>
<td>1111</td>
<td>1</td>
<td>540</td>
<td>540</td>
</tr>
<tr>
<td>Utility Examination Fee</td>
<td>1311</td>
<td>1</td>
<td>220</td>
<td>220</td>
</tr>
</tbody>
</table>

**Pages:**

**Claims:**

**Miscellaneous-Filing:**

**Petition:**

**Patent-Appeals-and-Interference:**
<table>
<thead>
<tr>
<th>Description</th>
<th>Fee Code</th>
<th>Quantity</th>
<th>Amount</th>
<th>Sub-Total in USD($)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Post-Allowance-and-Post-Issuance:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Extension-of-Time:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Miscellaneous:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Total in USD ($)</strong></td>
<td></td>
<td></td>
<td>1090</td>
<td></td>
</tr>
</tbody>
</table>
# Electronic Acknowledgement Receipt

<table>
<thead>
<tr>
<th>EFS ID:</th>
<th>6665428</th>
</tr>
</thead>
<tbody>
<tr>
<td>Application Number:</td>
<td>12641432</td>
</tr>
<tr>
<td>International Application Number:</td>
<td></td>
</tr>
<tr>
<td>Confirmation Number:</td>
<td>1608</td>
</tr>
<tr>
<td>Title of Invention:</td>
<td>FLASH MEMORY DEVICE AND MANUFACTURING METHOD OF THE SAME</td>
</tr>
<tr>
<td>First Named Inventor/Applicant Name:</td>
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</tr>
<tr>
<td>Customer Number:</td>
<td>23557</td>
</tr>
<tr>
<td>Filer:</td>
<td>Jeff Lloyd/JESSICA AYERS</td>
</tr>
<tr>
<td>Filer Authorized By:</td>
<td>Jeff Lloyd</td>
</tr>
<tr>
<td>Attorney Docket Number:</td>
<td>SUN.DH.627</td>
</tr>
<tr>
<td>Receipt Date:</td>
<td>18-DEC-2009</td>
</tr>
<tr>
<td>Filing Date:</td>
<td></td>
</tr>
<tr>
<td>Time Stamp:</td>
<td>10:49:54</td>
</tr>
<tr>
<td>Application Type:</td>
<td>Utility under 35 USC 111(a)</td>
</tr>
</tbody>
</table>

## Payment information:

<table>
<thead>
<tr>
<th>Submitted with Payment</th>
<th>yes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Payment Type</td>
<td>Credit Card</td>
</tr>
<tr>
<td>Payment was successfully received in RAM</td>
<td>$1090</td>
</tr>
<tr>
<td>RAM confirmation Number</td>
<td>8572</td>
</tr>
<tr>
<td>Deposit Account</td>
<td>190065</td>
</tr>
<tr>
<td>Authorized User</td>
<td>LLOYD, JEFF</td>
</tr>
</tbody>
</table>

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

- Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)
- Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)
Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)
Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)
Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

<table>
<thead>
<tr>
<th>Document Number</th>
<th>Document Description</th>
<th>File Name</th>
<th>File Size(Bytes)/Message Digest</th>
<th>Multi Part./.zip</th>
<th>Pages (if appl.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>as-filed.pdf</td>
<td>1036175</td>
<td>yes</td>
<td>21</td>
<td></td>
</tr>
</tbody>
</table>

**Multipart Description/PDF files in .zip description**

<table>
<thead>
<tr>
<th>Document Description</th>
<th>Start</th>
<th>End</th>
</tr>
</thead>
<tbody>
<tr>
<td>Specification</td>
<td>1</td>
<td>10</td>
</tr>
<tr>
<td>Claims</td>
<td>11</td>
<td>13</td>
</tr>
<tr>
<td>Abstract</td>
<td>14</td>
<td>14</td>
</tr>
<tr>
<td>Drawings-only black and white line drawings</td>
<td>15</td>
<td>21</td>
</tr>
</tbody>
</table>

**Warnings:**

<table>
<thead>
<tr>
<th>Information:</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
</tr>
<tr>
<td>Oath or Declaration filed</td>
</tr>
</tbody>
</table>

**Warnings:**

<table>
<thead>
<tr>
<th>Information:</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
</tr>
<tr>
<td>Request for USPTO to retrieve priority docs</td>
</tr>
</tbody>
</table>

**Warnings:**

<table>
<thead>
<tr>
<th>Information:</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
</tr>
<tr>
<td>Fee Worksheet (PTO-875)</td>
</tr>
</tbody>
</table>

**Warnings:**

<table>
<thead>
<tr>
<th>Information:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Files Size (in bytes):</td>
</tr>
</tbody>
</table>
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
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National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.
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<table>
<thead>
<tr>
<th><strong>EFS ID:</strong></th>
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</tr>
</thead>
<tbody>
<tr>
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</tr>
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</tr>
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</tr>
<tr>
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<td>SUN.DH.627</td>
</tr>
<tr>
<td><strong>Receipt Date:</strong></td>
<td>18-DEC-2009</td>
</tr>
<tr>
<td><strong>Filing Date:</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Time Stamp:</strong></td>
<td>10:49:54</td>
</tr>
<tr>
<td><strong>Application Type:</strong></td>
<td>Utility under 35 USC 111(a)</td>
</tr>
</tbody>
</table>

## Payment information:

<table>
<thead>
<tr>
<th>Submitted with Payment</th>
<th>yes</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Payment Type</strong></td>
<td>Credit Card</td>
</tr>
<tr>
<td><strong>Payment was successfully received in RAM</strong></td>
<td>$1090</td>
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<tr>
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<table>
<thead>
<tr>
<th>Document Number</th>
<th>Document Description</th>
<th>File Name</th>
<th>File Size(Bytes)</th>
<th>Multi Part / .zip</th>
<th>Pages if appl.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Specification</td>
<td>as-filed.pdf</td>
<td>1036175</td>
<td>yes</td>
<td>21</td>
</tr>
<tr>
<td></td>
<td>Claims</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Abstract</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Drawings-only black and white line drawings</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Multipart Description/PDF files in .zip description**

<table>
<thead>
<tr>
<th>Document Description</th>
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<th>End</th>
</tr>
</thead>
<tbody>
<tr>
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</tr>
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<td>11</td>
<td>13</td>
</tr>
<tr>
<td>Abstract</td>
<td>14</td>
<td>14</td>
</tr>
<tr>
<td>Drawings-only black and white line drawings</td>
<td>15</td>
<td>21</td>
</tr>
</tbody>
</table>

**Warnings:**

**Information:**

| 2               | Oath or Declaration filed      | Executed-Dec-POA.pdf | 135498    | no     | 3              |

**Warnings:**

**Information:**

| 3               | Request for USPTO to retrieve priority docs | Request-to-Retrieve.pdf | 124129    | no     | 1              |

**Warnings:**

**Information:**

| 4               | Fee Worksheet (PTO-875)         | fee-info.pdf          | 33006     | no     | 2              |

**Warnings:**

**Information:**

Total Files Size (in bytes): 1328808
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FLASH MEMORY DEVICE AND MANUFACTURING METHOD OF THE SAME

CROSS-REFERENCE TO RELATED APPLICATION


BACKGROUND

A flash memory device is a nonvolatile memory device that does not lose data stored therein even if power is turned off. In addition, the flash memory can record, read, and delete data at a relatively high speed.

Accordingly, the flash memory device is widely used for the Bios of a personal computer (PC), a set-top box, a printer, and a network server in order to store data. Recently, the flash memory device is extensively used for digital cameras and portable phones.

In such a flash memory device, a semiconductor device having a SONOS (Silicon-Oxide-Nitride-Oxide-Silicon) structure is often used.

Different from a flash memory device having a floating gate including polycrystalline silicon, the SONOS memory device is a charge-trap type device, in which gate voltage is applied so that charges (electrons) pass through a thin oxide layer formed on silicon to become injected into or released from a charge trap formed in a silicon nitride layer.

FIGS. 1A to 1C are sectional views showing the procedure for manufacturing flash memory devices according to related art.

As shown in FIG. 1A, when a split select gate is defined by a photo and etch process, select gate lengths of cells may be different from each other (L1≠L2) due to an overlay misalign in the photo process, so one cell (A-Cell shown on the left) may have characteristics different from characteristics of the other cell (B-Cell shown in the right).

In addition, as shown in FIG. 1B, when the split select gate is defined by the photo and etch process in a state in which a local nitride layer is used as a memory site, the cells may have various nitride lengths (L3≠L4) and select gate lengths (L1≠L2) due to the critical dimension CD
variation and overlay misalign in the photo process, so that characteristic variation of the left cell
(A-Cell) and the right cell (B-Cell) may be increased.

Further, referring to FIG. 1C, it can be difficult to remove polysilicon covering a source region between adjacent cells without damage when forming an active gate poly and a memory gate poly.

BRIEF SUMMARY

An embodiment provides a flash memory device having a self-align SONOS structure and a method for manufacturing the same, in which a self-align double spacer process is used instead of the photo and etch process to form a cell. According to embodiments, problems related to the CD and overlay variation can be minimized, thereby achieving cell uniformity while inhibiting degradation of characteristics.

In addition, an embodiment provides a flash memory device and a method for manufacturing the same, in which an area of a source side can be enlarged and a spacer poly forming process is performed after implanting source ions, so that time and labor force required for removing a gap-fill poly without active damage can be saved. In this case, the LDD length can be increased proportionally to the thickness of polysilicon used for the spacer poly, so that punch-through breakdown voltage (BV) between the source and the drain may rise during the program and erase operations.

A flash memory device according to an embodiment includes first and second memory gates on a substrate; a floating poly between the first and second memory gates; first and second select gates at respective outer sides of the first and second memory gates; an oxide layer between the first memory gate and the first select gate and between the second memory gate and the second select gate; a drain region in the substrate at outer sides of the first and second select gates; a source region in the substrate between the first and second memory gates; and a metal contact on each of the drain region and the source region.

A method for manufacturing a flash memory device according to an embodiment includes forming first and second memory gates on a substrate; forming an oxide layer on an entire surface of the substrate formed with the first and second memory gates; forming a floating poly between the first and second memory gates; forming first and second select gates at outer
sides of the first and second memory gates; forming a drain region in the substrate at outer sides of the first and second select gates; forming a source region in the substrate between the first and second memory gates; and forming a metal contact on each of the drain region and the source region.

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BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A to 1C are cross-sectional views showing the procedure for manufacturing a flash memory device according to related art;

FIG. 2 is a cross-sectional view of a flash memory device according to an embodiment;

and

FIGS. 3 to 14 are cross-sectional views showing the procedure for manufacturing a flash memory device according to the embodiment.

DETAILED DESCRIPTION

Hereinafter, embodiments of a flash memory device and a method for manufacturing the same will be described with reference to accompanying drawings.

In the description of embodiments, it will be understood that when a layer (or film) is referred to as being ‘on’ another layer or substrate, it can be directly on another layer or substrate, or intervening layers may also be present. Further, it will be understood that when a layer is referred to as being ‘under’ another layer, it can be directly under another layer, or one or more intervening layers may also be present. In addition, it will also be understood that when a layer is referred to as being ‘between’ two layers, it can be the only layer between the two layers, or one or more intervening layers may also be present.

FIG. 2 is a cross-sectional view of a flash memory device according to an embodiment.

Referring to FIG. 2, flash memory device according to an embodiment includes first and second memory gates 20a and 20b on a substrate 10; floating polys 29a and 29b between the first and second memory gates 20a and 20b; first and second select gates 30a and 30b at outer sides of the first and second memory gates 20a and 20b, respectively; a third oxide layer 25 between the first memory gate 20a and the first select gate 30a and between the second memory gate 20b and the second select gate 30b; a drain region formed on the substrate 10 at outer sides
of the first and second select gates 30a and 30b; a source region formed on the substrate 10 between the first and second memory gates 20a and 20b; and a metal contact 36 on each of the drain region and the source region. Reference numerals shown in FIG. 2, but not described, will be explained when a manufacturing method for the flash memory device is described.

According to the flash memory device and the method for manufacturing the same of an embodiment, a polysilicon forming process and an etching process of the polysilicon are performed after implanting source ions. Therefore, there is no need to remove polysilicon covering a source region in order to form the source region, and time and labor force required for removing the poly of the source region without damage can be saved. In addition, the manufacturing process is simplified and the manufacturing time is shortened, so that the manufacturing cost can be reduced.

According to an embodiment, a high bias is applied to the source of a selected cell during program and erase operations. By utilizing the poly and source region formation processes according to an embodiment, the polysilicon is used to block N+ ions when the N+ ion implantation process is performed, so that an LDD drift area of the source region of the cell is enlarged, thereby improving the punch-through BV between the source and the drain. Accordingly, when the program and erase operations of the cell are performed, the punch-through BV of the source receiving high bias is improved, so that the punch-through BV between the source and the drain can be improved without increasing the length of the cell.

Further, the memory cells of SONOS structures show characteristics sensitive to lengths of the nitride layer and the select gate. In a related art, photo and etch processes are performed to control the lengths of the nitride layer and the select gate. In contrast, embodiments of the invention can address the problems related to the CD and overlay variation found in the related art by employing a self-align scheme, resulting in superior characteristics in terms of uniformity of cell characteristics.

Hereinafter, a method for manufacturing the flash memory device according to an embodiment will be described with reference to FIGS. 3 to 14.

First, as shown in FIG. 3, an isolation layer 12 is formed on a substrate 10 to define an active area 11. At this time, a pad oxide layer 15 can be formed on the active area.
Then, as shown in FIG. 4, a first ion implantation process is performed on the substrate 10 to form a well area 13. For the memory cell area, well area 13 can be P type where the memory gates are to be formed. In an embodiment, if the substrate 10 is a P type substrate, N type ions are implanted to form an N type well, and the regions where the memory gates are formed can be formed without a well 13 therebelow or be formed with a more highly P type region 13. According to an embodiment, a second ion implantation process is performed on the substrate 10 having the well area 13 to adjust threshold voltage.

Next, as shown in FIG. 5, the pad oxide layer 15 is removed and a first oxide layer 21, a nitride layer 22, a second oxide layer 23, and a first polysilicon layer 24 are sequentially formed on the substrate 10.

For instance, the first oxide layer 21 may serve as a tunnel oxide layer. The first oxide layer 21 can include SiO₂, and can be formed on the substrate 10 at thickness of about 20 to 80 Å by performing the heat treatment process with respect to the substrate 10. In another embodiment, the first oxide layer 21 can include high-K material, such as Al₂O₃, and can be deposited on the substrate 10 through CVD (chemical vapor deposition) or ALD (atomic layer deposition).

The first nitride layer 22 may serve as a charge trap layer. The first nitride layer 22 can include SiₓNᵧ (where x and y are natural numbers), and can be deposited on the first oxide layer 21 at thickness of about 70 to 100 Å through CVD.

The second oxide layer 23 may serve as a top oxide layer. The second oxide layer can include SiO₂, and can be deposited on the first nitride layer 22 through CVD, but the embodiment is not limited thereto.

The first polysilicon layer 24 can be deposited on the second oxide layer 23.

Then, as shown in FIG. 6, the first oxide layer 21, the first nitride layer 22, the second oxide layer 23, and the first polysilicon layer 24 are patterned to form a memory gate 20 including a first memory gate 20a and a second memory gate 20b. Thus, the memory gate 20 may have the SONOS structure.

For instance, after forming a first photoresist pattern (not shown) on the first polysilicon layer 24 such that parts of the first polysilicon layer 24 for the memory gate 20 are covered, the first polysilicon layer 24 is etched to define the memory gate 20. At this time, the etching process
can be performed for a time to etch from the first polysilicon layer 24 to the first nitride layer 22. Otherwise, the etching process can be performed in two steps, in which the first polysilicon layer 24 is etched in the first step and the remaining layers are etched in the second step. In the case of the two-step etching process, the second oxide layer 23 serves as an etch stop layer in the first step, and the second oxide layer 23 and the first nitride layer 22 are etched in the second step. The second step can be performed through dry etching or wet etching.

Then, as shown in FIG. 7, a third oxide layer 25 is formed over the entire surface of the substrate 10 formed with the first and second memory gates 20a and 20b.

In one embodiment, the first oxide layer 21 is removed from regions other than below the memory gates 20, and a thermal oxidation process, such as a dual gate oxidation process, is performed to form the third oxide layer 25.

The third oxide layer 25 may be an oxide layer including a thick gate oxide layer and a thin gate oxide layer, or may be a thin gate oxide layer itself.

Select gates 30a and 30b, which will be formed later, may use the third oxide layer 25 as the select gate oxide.

Then, as shown in FIG. 8, a halo ion implantation region 27b and a source LDD (lightly doped drain) ion implantation region 27a can be formed in the substrate 10 between the first and second memory gates 20a and 20b by using a first photoresist pattern 41 as a mask to improve HCl (hot carrier injection) efficiency.

Next, as shown in FIG. 9, the first photoresist pattern 41 is removed, and a second polysilicon layer 28 is formed over the entire surface of the substrate 10 formed with a source LDD region 27a.

In one embodiment, the second polysilicon layer 28 is deposited just after the first photoresist pattern 41 has been removed.

Then, as shown in FIG. 10, the second polysilicon layer 28 is etched to form first and second floating polys 29a and 29b between the first and second memory gates 20a and 20b, and to form first and second select gates 30a and 30b at outer sides of the first and second memory gates 20a and 20b. The floating polys and select gates can have a spacer shape.

In an embodiment, the entire surface of the cell area is subject to the polysilicon etching process. That is, an etch back process without an etch mask on the cell area can be performed.
In this case, the length of the select gates 30a and 30b can be determined according to thickness of the second polysilicon layer 28. Therefore, the misalign problem of structures in the cell area can be minimized by forming the select gates through the self-align scheme.

In addition, according to an embodiment, since the ion implantation process has been already performed with respect to the source region and the LDD region, there is no need to remove the floating polys 29a and 29b in order to implant ions into the source region. Thus, the time and labor force required to remove the floating polys 29a and 29b without damage can be saved and the punch-through BV between the drain and the source can be improved.

According to an embodiment, when the select gate poly is defined, patterning and etching processes can be performed by using a photoresist pattern in the peripheral region (not shown), thereby defining the peripheral gate poly. In addition, if the active area is damaged during the etching process, the photo and etching process to define the select gate poly of the cell can be performed separately from the photo and etching process to define the peripheral gate poly.

Referring to FIG. 11, a drain halo ion implantation region 32 and a drain LDD ion implantation region 31 are formed at the outer sides of the first and second select gates 30a and 30b by using a second photoresist layer pattern 42 as a mask.

According to an embodiment, the drain LDD ion implantation region 31 can be formed when the LDD ion implantation process is performed for a transistor provided in the peripheral region.

Then, as shown in FIG. 12, after removing the second photoresist layer pattern 42, a drain region 34 is formed on the substrate 10 at the outer sides of the first and second select gates 30a and 30b and a source region 26 is formed on the substrate 10 between the first and second memory gates 20a and 20b through an ion implantation process.

In an embodiment, a spacer 33 is formed, and an ion implantation process is performed using N+ ions at high concentration to form a source region 26 and a drain region 34. The spacer 33 may have an ONO (Oxide-Nitride-Oxide) structure or an ON (Oxide-Nitride) structure.

According to an embodiment, the ion implantation process for the drain region and the source region can be performed simultaneously with the ion implantation process for the source and the drain of the transistor provided in the peripheral region.
According to an embodiment, the floating poly of the source region may block the N+ ions when the ion implantation process is performed for the source and the drain, so that the LDD drift area D can be enlarged, thereby improving the punch-through BV between the source and the drain.

Then, as shown in FIG. 13, a salicide process is performed. For example, after removing the third oxide layer 25 from exposed surfaces of the source region 26, the drain region 34, the memory gate 20, and the floating polys 29a and 29b, a metal layer, such as a cobalt (Co) layer, is formed on the entire surface of the substrate 10. Then, salicide layers 35 are formed on the source region 26, the drain region 34, the select gates 30a and 30b, the memory gate 20, and the floating polys 29a and 29b through a heat treatment process with respect to the metal layer.

Next, as shown in FIG. 14, a back end process is performed to form metal contacts 36 and metal lines 37 on the source region 26 and the drain region 34.

According to the flash memory device and the method for manufacturing the same of an embodiment, since the poly forming process and the etching process are performed after implanting source ions, there is no need to remove poly disposed on the source region, so time and labor force required for removing the poly on the source region without damage can be saved. In addition, the manufacturing process is simplified and the manufacturing time is shortened, so that the manufacturing cost can be reduced.

In addition, a high bias can be applied to the source of the cell during the program and erase operations. According to an embodiment, the poly on the source region blocks N+ ions when the N+ ion implantation process for forming the source and drain regions is performed, so that an LDD drift area of the source region of the cell is enlarged, thereby improving the punch-through BV between the source and the drain. Accordingly, when the program and erase operations of the cell are performed, the punch-through BV of the source receiving high bias is improved, so that the punch-through BV between the source and the drain can be improved without increasing the length of the cell.

Further, the memory cells show characteristics sensitive to lengths of the nitride layer and the select gate. According to the related art, a photo and etch process is performed to control the lengths of the nitride layer and the select gate. In contrast, an embodiment can solve the
problems related to the CD and overlay variation of the related art by employing a self-align scheme, resulting in superior characteristics in terms of uniformity of cell characteristics.

The flash memory device described above can be operated as follows, but the embodiment is not limited thereto.

The program operation of the flash memory device according to one embodiment can be achieved by applying bias for generating hot carrier electrons.

In addition, the erase operation can be achieved by forming EHP (electron-hole pair) while applying a bias that enables formation of band-to-band tunneling (BTBT). At this time, since the erase operation is performed in a unit of W/L (word line), cells aligned in the same word line of a selected cell are completely erased.

That is, the cells aligned in the same word line of the selected cell are erased even if the cells are unselected cells. In the read operation, current is applied according to bias applied to a drain region. Since the current applied during the program operation is different from the current applied during the erase operation, the program operation can be distinguished from the erase operation based on the current.

Any reference in this specification to “one embodiment,” “an embodiment,” “example embodiment,” etc., means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of such phrases in various places in the specification are not necessarily all referring to the same embodiment. Further, when a particular feature, structure, or characteristic is described in connection with any embodiment, it is submitted that it is within the purview of one skilled in the art to effect such feature, structure, or characteristic in connection with other ones of the embodiments.

Although embodiments have been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the spirit and scope of the principles of this disclosure. More particularly, various variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the disclosure, the drawings and the appended claims. In addition to
variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.
CLAIMS

What is claimed is:

1. A flash memory device comprising:
   first and second memory gates adjacentl disposed on a substrate;
   a floating poly between the first and second memory gates;
   first and second select gates at respective outer sides of the first and second memory gates;
   an oxide layer between the first memory gate and the first select gate and between the second memory gate and the second select gate;
   a drain region in the substrate at outer sides of the first and second select gates;
   a source region in the substrate between the first and second memory gates; and
   a metal contact on each of the drain region and the source region.

2. The flash memory device of claim 1, wherein the oxide layer is further disposed between the first and second select gates and the substrate.

3. The flash memory device of claim 1, wherein the oxide layer serves as a gate oxide layer for the first and second select gates.

4. The flash memory device of claim 1, further comprising a halo ion implantation region and an LDD ion implantation region in the substrate between the first and second memory gates.

5. A method for manufacturing a flash memory device, the method comprising:
   forming first and second memory gates on a substrate;
   forming a third oxide layer on an entire surface of the substrate formed with the first and second memory gates;
   forming a floating poly between the first and second memory gates;
   forming first and second select gates at respective outer sides of the first and second memory gates;
forming a drain region in the substrate at outer sides of the first and second select gates; and
forming a source region in the substrate between the first and second memory gates; and
forming a metal contact on each of the drain region and the source region.

6. The method of claim 5, wherein the forming of the floating poly between the first and second memory gates comprises:

forming a second polysilicon layer on an entire surface of the substrate formed with the oxide layer; and

etching the second polysilicon layer, wherein the etching of the second polysilicon layer forms the floating poly at inner sidewalls of the first and second memory gates.

7. The method of claim 6, wherein the forming of the floating poly and the forming of the first and second select gates are simultaneously achieved by the etching of the second polysilicon layer.

8. The method of claim 7, wherein the etching of the second polysilicon layer forms the floating poly and the first and second select gates through a self-align scheme.

9. The method of claim 7, further comprising forming a peripheral gate poly simultaneously with the forming of the floating poly and the forming of the first and second select gates.

10. The method of claim 5, further comprising forming a source and drain of a transistor in a peripheral region simultaneously with an ion implantation process for forming the drain region at the outer sides of the first and second select gates.

11. The method of claim 5, wherein the forming of the first and second memory gates on the substrate includes:

sequentially forming a first oxide layer, a first nitride layer, a second oxide layer and a first polysilicon layer on the substrate; and
patterning the first oxide layer, the first nitride layer, the second oxide layer and the first polysilicon layer to form the first and second memory gates adjacently disposed on the substrate.

12. The method of claim 5, further comprising forming a source LDD region in the substrate between the first and second memory gates through an ion implantation process before forming the floating poly.
ABSTRACT

Disclosed are a flash memory device and a method for manufacturing the same. The flash memory device includes first and second memory gates on a substrate; a floating poly between the first and second memory gates; first and second select gates at respective outer sides of the first and second memory gates; an oxide layer between the first memory gate and the first select gate and between the second memory gate and the second select gate; a drain region in the substrate at outer sides of the first and second select gates; a source region in the substrate between the first and second memory gates; and a metal contact on each of the drain region and the source region.
DECLARATION (37 C.F.R. § 1.63) AND POWER OF ATTORNEY

As a below-named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name; and

I believe that I am the original, first, and sole inventor (if only one name is listed below), or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled FLASH MEMORY DEVICE AND MANUFACTURING METHOD OF THE SAME, specification for which

☑ is attached hereto.
☐ was filed ________________ Serial No. ________________

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code §119 and/or §365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

<table>
<thead>
<tr>
<th>Application Serial No.</th>
<th>Country</th>
<th>Filing Date</th>
<th>Priority Claimed</th>
</tr>
</thead>
<tbody>
<tr>
<td>10-2008-0138887</td>
<td>Korea</td>
<td>December 31, 2008</td>
<td>Yes</td>
</tr>
</tbody>
</table>

I hereby claim priority benefits under Title 35, United States Code §119 of any provisional application(s) for patent listed below:

<table>
<thead>
<tr>
<th>Application Serial No.</th>
<th>Filing Date</th>
<th>Priority Claimed</th>
</tr>
</thead>
</table>

I hereby claim the benefit under Title 35, United States Code, §120 and/or §365 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application(s) in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

<table>
<thead>
<tr>
<th>Application Serial No.</th>
<th>Filing Date</th>
<th>Status (Patented, Pending, Abandoned)</th>
</tr>
</thead>
</table>
I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint all persons registered to practice before the Patent and Trademark Office associated with Customer Number 23557 as my attorneys with full power of substitution and revocation to prosecute this application and all divisions and continuations thereof and to transact all business in the Patent and Trademark Office connected therewith.
Name of First or Sole Inventor: Young Jun KWON

Residence: Chungbuk, Republic of Korea

Citizenship: Republic of Korea

Post Office Address: 102-502, Yeong Heights Villa, Ohyang-ri, Gangok-myeon, Bumseong-gun, Chungbuk, Republic of Korea

Signature of First or Sole Inventor: [Signature]

Date: December 16, 2004

Name of Second Joint Inventor:

Residence: 

Citizenship: 

Post Office Address: 

Signature of Second Joint Inventor: [Signature]

Date: 

Name of Third Joint Inventor:

Residence: 

Citizenship: 

Post Office Address: 

Signature of Third Joint Inventor: [Signature]

Date: 

Name of Fourth Joint Inventor:

Residence: 

Citizenship: 

Post Office Address: 

Signature of Fourth Joint Inventor: [Signature]

Date: 

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# PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

<table>
<thead>
<tr>
<th>APPLICATION AS FILED – PART I</th>
<th>SMALL ENTITY</th>
<th>OTHER THAN SMALL ENTITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>FOR</td>
<td>(Column 1)</td>
<td>(Column 2)</td>
</tr>
<tr>
<td>BASIC FEE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(37 CFR 1.18(a), (b), or (c))</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>SEARCH FEE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(37 CFR 1.18(k), (l), or (m))</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>EXAMINATION FEE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(37 CFR 1.18(o), (p), or (q))</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>TOTAL CLAIMS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(37 CFR 1.19(i))</td>
<td>12</td>
<td>x$26</td>
</tr>
<tr>
<td>INDEPENDENT CLAIMS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(37 CFR 1.18(h))</td>
<td>2</td>
<td>x$110</td>
</tr>
<tr>
<td>APPLICATION SIZE FEE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(37 CFR 1.16(c))</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TOTAL</td>
<td>195</td>
<td>390</td>
</tr>
</tbody>
</table>

* If the difference in column 1 is less than zero, enter "0" in column 2.

# APPLICATION AS AMENDED – PART II

<table>
<thead>
<tr>
<th>AMENDMENT A</th>
<th>SMALL ENTITY</th>
<th>OTHER THAN SMALL ENTITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLAIMS REMAINING AFTER AMENDMENT</td>
<td>HIGHEST NUMBER PREVIOUSLY PAID FOR</td>
<td>PRESENT EXTRA</td>
</tr>
<tr>
<td>Total (37 CFR 1.16(i))</td>
<td>*</td>
<td>Minus</td>
</tr>
<tr>
<td>Independent (37 CFR 1.16(h))</td>
<td>*</td>
<td>Minus</td>
</tr>
<tr>
<td>Application Size Fee (37 CFR 1.16(g))</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>TOTAL ADD’T FEE</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>AMENDMENT B</th>
<th>SMALL ENTITY</th>
<th>OTHER THAN SMALL ENTITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLAIMS REMAINING AFTER AMENDMENT</td>
<td>HIGHEST NUMBER PREVIOUSLY PAID FOR</td>
<td>PRESENT EXTRA</td>
</tr>
<tr>
<td>Total (37 CFR 1.16(i))</td>
<td>*</td>
<td>Minus</td>
</tr>
<tr>
<td>Independent (37 CFR 1.16(h))</td>
<td>*</td>
<td>Minus</td>
</tr>
<tr>
<td>Application Size Fee (37 CFR 1.16(g))</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>TOTAL ADD’T FEE</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" is less than 20, enter "0".
*** If the "Highest Number Previously Paid For" is less than 3, enter "1".

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