ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

**Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)**

(application filed on or after May 29, 2000)

The Patent Term Adjustment is 273 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Hyun-Ju Lim, Mapo-gu, KOREA, REPUBLIC OF;
PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

or Fax (571)-273-885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60803 7590 10/28/2010
Sherr & Vaughn, PLLC
620 Herndon Parkway
Suite 320
Herndon, VA 20170

APPLICATION NO. 12/46,486 FILING DATE 06/29/2008 FIRST NAMED INVENTOR Hyun-Ju Lim ATTORNEY DOCKET NO. 604-0170 CONFIRMATION NO. 5212

TITLE OF INVENTION: METHOD OF MANUFACTURING FLASH MEMORY DEVICE

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EXAMINER SLUTSKER, JULIA

ART UNIT 2891 CLASS-SUBCLASS 438-199000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
   - Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
   - "Fee Address" indication (or "Fee Address" Indication form PTO/SB/471, Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list:
   - (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
   - (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

   Sherr & Vaughn, PLLC

3. ASSIGNEE NAME AND ADDRESS DATA TO BE PRINTED ON THE PATENT (print or type)

   (A) NAME OF ASSIGNEE: Dongbu HiTek Co., Ltd.
   (B) RESIDENCE: (CITY AND STATE OR COUNTRY) Seoul, Republic of Korea

   Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
   ☐ Issue Fee
   ☐ Publication Fee (No small entity discount permitted)
   ☐ Advance Order - # of Copies

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)
   ☐ A check is enclosed
   ☐ A check is enclosed (enclose a copy of this form)
   ☐ Payment by credit card. Form PTO-2038 is attached.
   ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number ____________ (enclose a extra copy of this form).

5. Change in Entity Status (from status indicated above)
   ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.128.
   ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.127(g)(2).

NOTE: The Issue Fee and/or Maintenance Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature ________________
Typed or printed name Todd A. Vaughn

Date 10/06/2010
Registration No. 52,319

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.
OMB 0651-0033 U.S. Patent and Trademark Office; U.S. Department of Commerce
# Electronic Patent Application Fee Transmittal

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## Utility under 35 USC 111(a) Filing Fees

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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.
NOTICE OF ALLOWANCE AND FEE(S) DUE

60803 7590 10/28/2010

SHERR & VAUGHN, PLLC
620 HERNDON PARKWAY
SUITE 320
HERNDON, VA 20170

EXAMINER
SLUTSKER, JULIA
ART UNIT 2891
PAPER NUMBER

DATE MAILED: 10/28/2010

APPLICATION NO. 12/146,486
FILING DATE 06/26/2008
FIRST NAMED INVENTOR Hyun-Ju Lim
ATTORNEY DOCKET NO. 604-0170
CONFIRMATION NO. 5212

TITLE OF INVENTION: METHOD OF MANUFACTURING FLASH MEMORY DEVICE

APPL. TYPE nonprovisional
SMALL ENTITY NO
ISSUE FEE DUE $1510
PUBLICATION FEE DUE $300
PREV. PAID ISSUE FEE $0
TOTAL FEE(S) DUE $1810
DATE DUE 01/28/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.
PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail

Mail Stop ISSUE FEE
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P.O. Box 1450
Alexandria, Virginia 22313-1450

or Fax

(571)-273-2885

SHERR & VAUGHN, PLLC
620 HERNDON PARKWAY
SUITE 320
HERNDON, VA 20170

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CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60803
7590
10/28/2010

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Depositor’s name

Signature

(Date)

APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO.
--- | --- | --- | --- | ---
12/146,486 | 06/26/2008 | Hyun-Ju Lim | 604-0170 | 5212

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EXAMINER | ART UNIT | CLASS-SUBCLASS |
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SLUTSKER, JULIA | 2891 | 438-199000 |

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   (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

   PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

   (A) NAME OF ASSIGNEE
   (B) RESIDENCE: (CITY and STATE OR COUNTRY)

   Please check the appropriate assignee category or categories (will not be printed on the patent):

   - Individual
   - Corporation or other private group entity
   - Government

4. The following fee(s) are submitted:

   - Issue Fee
   - Publication Fee (No small entity discount permitted)
   - Advance Order - # of Copies

   4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

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   - a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
   - b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

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Typed or printed name

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PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 273 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 273 day(s).

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**Notice of Allowability**

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<td>JULIA SLUTSKER</td>
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**The MAILING DATE of this communication appears on the cover sheet with the correspondence address**—

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to **08/17/2010**.

2. ☒ The allowed claim(s) is/are **1-7, 9-14 and 16-20**.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All   b) ☐ Some*  c) ☐ None  of the:
   1. ☒ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. ______.
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
   * Certified copies not received: ______.

   Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

   **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date ______.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ______.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

---

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
3. ☐ Information Disclosure Statements (PTO/SD/08), Paper No./Mail Date ______
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date ______.
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other ______

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U.S. Patent and Trademark Office
PTOL-37 (Rev. 08-06)  Notice of Allowability  Part of Paper No./Mail Date 20101014
DETAILED ACTION

Allowable Subject Matter

1. Claims 1-7, 9-14, and 16-20 allowed.

2. The following is an examiner’s statement of reasons for allowance: the search of the prior art does not disclose or reasonably suggest removing the entire fourth dielectric film as required by amended independent claims 1, 12 and 20.

   Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JULIA SLUTSKER whose telephone number is (571)270-3849. The examiner can normally be reached on Monday-Friday, 8 a.m.-5 p.m. EST.

   If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Keisha Bryant can be reached on (571)-272-1844. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.
4. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JS
October 14, 2010

/Asok K. Sarkar/
Primary Examiner, Art Unit 2891
October 22, 2010
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### Issue Classification

**Application/Control No.**
12146486

**Applicant(s)/Patent Under Reexamination**
LIM, HYUN-JU

**Examiner**
JULIA SLUTSKER

**Art Unit**
2891

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**JULIA SLUTSKER**
Examiner.Art Unit 2891

(Asst Examiner)

**Total Claims Allowed:**
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**10/14/2010**

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**Asok K Sarkar**
Primary Examiner.Art Unit 2891

(Primary Examiner)

**10/22/2010**

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** APPLICANTS **

Hyun-Ju Lim, Mapo-gu, KOREA, REPUBLIC OF;

** CONTINUING DATA ***********************

** FOREIGN APPLICATIONS ***********************


** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **

07/09/2008

Foreign Priority claimed: Yes No
35 USC 119(a-d) conditions met: Yes No

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** ADDRESS **

SHERR & VAUGHN, PLLC
620 HERNDON PARKWAY
SUITE 320
HERNDON, VA 20170
UNITED STATES

** TITLE **

METHOD OF MANUFACTURING FLASH MEMORY DEVICE

** FILING FEE RECEIVED **

1030

FEES: Authority has been given in Paper No. ________ to charge/credit DEPOSIT ACCOUNT No. ________ for following:

- All Fees
- 1.16 Fees (Filing)
- 1.17 Fees (Processing Ext. of time)
- 1.18 Fees (Issue)
- Other __________________
- Credit

BIB (Rev. 05/07).
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Hyun-Ju Lim
Application No.: 12/146,486
Filed: June 26, 2008

Docket No.: 604-0170
Confirmation No.: 5212
Group Art Unit: 2891
Examiner: SLUTSKER, JULIA

For: METHOD OF MANUFACTURING FLASH MEMORY DEVICE

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. BOX 1450
Alexandria, VA 22313-1450

REPLY AND AMENDMENT UNDER 37 C.F.R. § 1.111

Sir:

In response to the Non-Final Office Action mailed May 26, 2010, Applicant respectfully requests reconsideration of the application in view of the following Amendments and Remarks.

Amendments to the Claims are reflected in the listing of claims which begins on page 2.

Remarks begin on page 8.

Applicant believes that no extensions of time are required at this time. However, if extensions of time are necessary to prevent abandonment of this application, such extensions of time are hereby petitioned for under 37 C.F.R. §1.136(a).
AMENDMENTS TO THE CLAIMS

Please CANCEL claims 8 and 15 without prejudice or disclaimer to the subject matter recited therein.

Please AMEND claims 1, 12, and 20 as shown below.

The following is a complete list of all claims in this application.

1. (Currently Amended) A method comprising:
   forming a gate on a semiconductor substrate; and then
   sequentially stacking a first dielectric film and a second dielectric film on the semiconductor substrate; and then
   forming a first spacer comprising a first dielectric film pattern and a second dielectric film pattern on sidewalls of the gate by performing a first etching process; and then
   forming source and drain areas in the semiconductor substrate; and then
   removing the second dielectric film; and then
   sequentially stacking a third dielectric film and a fourth dielectric film on the semiconductor substrate; and then
   forming a second spacer comprising the first dielectric pattern and a third dielectric pattern on the sidewalls of the gate by performing a second etching process, wherein forming the second spacer comprises performing the second etching process removing a portion of the third dielectric film and the entire fourth dielectric film; and
then

forming an interlayer dielectric film on the semiconductor substrate including the
gate and the first spacer.

2. (Original) The method of claim 1, wherein removing the second dielectric
pattern comprises:

removing the second dielectric film pattern by performing a wet etching process.

3. (Original) The method of claim 2, wherein the wet etching process is
performed using phosphoric acid (H₃PO₄) as an etching solution.

4. (Original) The method of claim 1, wherein the first and fourth dielectric
films comprise an oxide film and the second and third dielectric films comprise a nitride
film.

5. (Original) The method of claim 4, wherein the oxide film comprises TEOS
and the nitride film comprises SiN.

6. (Original) The method of claim 1, wherein sequentially stacking the first
dielectric film and the second dielectric film comprises:

sequentially forming the first dielectric film having a thickness in a range between
100 to 300Å and the second dielectric film having a thickness in a range between 500 to
800Å.
7. (Original) The method of claim 1, wherein sequentially stacking the third dielectric film and the fourth dielectric film comprises:

forming the third dielectric film having a thickness in a range between 70 to 200Å and the fourth dielectric film having a thickness in a range between 360 to 440Å.

8. (Cancelled)

9. (Original) The method of claim 1, wherein forming the gate includes sequentially stacking a gate oxide film, a floating gate, a dielectric film and a control gate on the semiconductor substrate.

10. (Original) The method of claim 1, further comprising, after forming the second spacer and before forming the interlayer dielectric film:

forming a metal layer on the semiconductor substrate including the gate and the second spacer; and then

forming a silicide layer on the gate and the source/drain area by performing an annealing process on the semiconductor substrate.

11. (Original) The method of claim 10, wherein the metal layer comprises cobalt.

12. (Currently Amended) A method comprising:
forming a plurality of gates in a cell area of a semiconductor substrate and a gate electrode in a peripheral area of the semiconductor substrate; and then

forming first spacers comprising a first dielectric layer and a second dielectric layer on sidewalls of the gates and the gate electrode; and then

forming source/drain areas in the semiconductor substrate; and then

removing the second dielectric layer to expose the first dielectric layer; and then

forming second spacers comprising the first dielectric layer and a third dielectric layer on the sidewalls of the gate and the gate electrode, wherein performing the second etching process comprises removing a portion of the third dielectric film and the entire fourth dielectric film.

13. (Original) The method of claim 12, wherein forming the first spacers comprises:

forming the first dielectric film against sidewalls of the gate and the gate electrode and on the uppermost surface of the semiconductor substrate; and then

forming the second dielectric film on the first dielectric film; and then

performing a first etching process on the first dielectric film and the second dielectric film.

14. (Original) The method of claim 12, wherein forming the second spacers comprises:

forming the third dielectric film on the first dielectric film; and then

forming a fourth dielectric film on the third dielectric film; and then
performing a second etching process on the third dielectric film and the fourth dielectric film.

15. (Cancelled)

16. (Original) The method of claim 12, further comprising, after forming the second spacers:

forming silicide layers on the gates, the gate electrodes and the source/drain areas; and then

forming an interlayer dielectric film on the semiconductor substrate including the gates, the gate electrode, the silicide layers and the second spacers; and then

forming a contact plug extending through the interlayer dielectric film and electrically connected to the gates, the gate electrode and the source/drain areas.

17. (Original) The method of claim 16, wherein forming the silicide layer comprises:

forming a first metal layer on the semiconductor substrate including the gates, the gate electrode and the second spacers; and then

performing an annealing process on the semiconductor substrate.

18. (Original) The method of claim 17, wherein forming the contact plugs comprises:

forming via holes in the interlayer dielectric film exposing the silicide layers; and
then

forming a second metal layer in the via holes.

19. (Original) The method of claim 18, wherein the first metal layer comprises cobalt and the second metal layer comprises tungsten.

20. (Currently Amended) A method comprising:

forming gates spaced apart on a semiconductor substrate; and then

forming first spacers comprising a first oxide layer and a first nitride layer on sidewalls of the gates; and then

forming source/drain areas in the semiconductor substrate; and then

removing the first nitride layer to expose the first oxide layer; and then

forming second spacers comprising the first oxide layer and a second nitride layer on the sidewalls of the gate, wherein performing the second etching process comprises removing a portion of the third dielectric film and the entire fourth dielectric film; and then

forming silicide layers on the gates and the source/drain areas; and then

forming an interlayer dielectric film on the semiconductor substrate including the gates, the silicide layers and the second spacers; and then

forming a contact plug extending through the interlayer dielectric film and electrically connected to the gates, the gate electrode and the source/drain areas.
REMARKS

Claims 1-7, 9-14, and 16-20 are pending in the above-referenced patent application. By this amendment, claims 8 and 15 are cancelled without prejudice or disclaimer to the subject matter recited therein, and claims 1, 12, and 20 are amended. No new matter has been added.

In the Non-Final Office Action: Claims 1-7, 9-11, and 20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Kwon (U.S. 2006/0079060) in view of Yan (U.S. 2008/0090350). Claims 12-14 and 16-19 were rejected under 35 U.S.C. §103(a) as being unpatentable over Kwon in view of Kwak (U.S. 2008/0280442) and Yan. Claims 8 and 15 were objected to as being dependent upon a rejected base claim, but indicated as allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In reply to the rejection of claims 1-7, 9-11, and 20 under 35 U.S.C. §103(a) as being unpatentable over Kwon in view of Yan, and in reply to the rejection of claims 12-14 and 16-19 under 35 U.S.C. §103(a) as being unpatentable over Kwon in view of Kwak and Yan, the Applicant respectfully requests reconsideration. By this amendment, claim 1 is amended to incorporate the allowable subject matter of claim 8, and claims 12 and 20 are amended to incorporate the allowable subject matter of claim 15. Accordingly, the Applicant respectfully requests withdrawal of the rejection of claims 1-7, 9-14, and 16-20 under 35 U.S.C. §103(a).
CONCLUSION

Applicant believes that a full and complete response has been made to the Office Action and respectfully submits that all of the stated objections and grounds for rejection have been overcome or rendered moot. Accordingly, Applicant respectfully submits that all pending claims are allowable and that the application is in condition for allowance.

Should the Examiner feel that there are any issues outstanding after consideration of this response, the Examiner is invited to contact the Applicant’s undersigned representative at the number below to expedite prosecution.

Prompt and favorable consideration of this Reply is respectfully requested.

Respectfully Submitted,

[Signature]

Todd A. Vaughn
Reg. No. 52,319

Sherr & Vaughn, PLLC
620 Herndon Parkway
Suite 320
Herndon, Virginia 20170
Tel: 571-313-7556
Fax: 703-935-8473

TAV/SWL
## Electronic Acknowledgement Receipt

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**Warnings:**

**Information:**
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.
**PATENT APPLICATION FEE DETERMINATION RECORD**

For: Application or Docket Number: 12/146,486
Filing Date: 08/26/2008

**APPLICATION AS FILED – PART I**

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**APPLICATION SIZE FEE (37 CFR 1.16(e))**

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(e).

**MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))**

* If the difference in column 1 is less than zero, enter “0” in column 2.

**APPLICATION AS AMENDED – PART II**

**AMENDMENT 08/17/2010**

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Legal Instrument Examiner: ROSS W. BROWN

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.
Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.
Office Action Summary

Application No. 12/146,486
Applicant(s) LIM, HYUN-JU

Examiner JULIA SLUTSKER
Art Unit 2891

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) [x] Responsive to communication(s) filed on 07 December 2009.

2a) [ ] This action is FINAL.

2b) [x] This action is non-final.

3) [ ] Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) [x] Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) [ ] Claim(s) _____ is/are allowed.

6) [x] Claim(s) 1-7,9-14 and 16-20 is/are rejected.

7) [x] Claim(s) 8 and 15 is/are objected to.

8) [ ] Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) [ ] The specification is objected to by the Examiner.

10) [x] The drawing(s) filed on 26 June 2008 is/are: a) [x] accepted or b) [ ] objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) [ ] The oath or declaration is objected to by the Examiner. Note the attached Office action or form PTO-152.

Priority under 35 U.S.C. § 119

12) [x] Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) [x] All  b) [ ] Some * c) [ ] None of:

1. [x] Certified copies of the priority documents have been received.

2. [ ] Certified copies of the priority documents have been received in Application No. _____.

3. [ ] Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) [x] Notice of References Cited (PTO-892)

2) [ ] Notice of Draftsman’s Patent Drawing Review (PTO-948)

3) [x] Information Disclosure Statement(s) (PTO/SB/08)

4) [ ] Interview Summary (PTO-413)

5) [ ] Notice of Informal Patent Application

6) [ ] Other: _____

U.S. Patent and Trademark Office
PTOL-326 (Rev. 08-06) Office Action Summary Part of Paper No./Mail Date 20100514
DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7, 9-11, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon (US 2006/0079060) in view of Yan (US 2008/0090350).

   Regarding claim 1, Kwon discloses a method comprising: forming a gate (Fig.13, numeral 306 a, 306 b) on a semiconductor substrate (Fig.13, numeral 300); and then sequentially stacking a first dielectric film (Fig.14, numeral 314) and a second dielectric film (Fig.14, numeral 318) on the semiconductor substrate (Fig.14, numeral 300); and then forming a first spacer comprising a first dielectric film patter (Fig.15, numeral 316a) and a second dielectric film pattern (Fig.15, numeral 318a) on sidewalls of the gate (Fig.15, numerals 306a, 306b) by performing a first etching process ([0052]) ; and then forming source and drain areas in the semiconductor substrate (Fig. 16, numeral 326); and removing the second dielectric film ([0053]); and then sequentially stacking a third dielectric film (Fig.17, numeral 332) and a fourth dielectric film (Fig. 17, numeral 334) on the semiconductor substrate (Fig.17, numeral 300); and then forming a second spacer comprising the first dielectric pattern (Fig.18, numeral 316a) and a third dielectric pattern on the sidewalls of the gate (Fig.18, numerals 332a) by performing a second
etching process ([0056]); and then forming an interlayer dielectric film on the semiconductor substrate including the gate and the first spacer ([0044]).

Kwon does not disclose that removing the second dielectric film is performed after forming source and drain areas in the semiconductor substrate.

Kwon however discloses that the source/drain areas can be formed before forming of the silicon epitaxial layer (324) which is formed after removing the second dielectric film (318a) ([0053], [0054]). And Yan discloses removing the second dielectric film (Fig.2D, numeral 193) after forming source and drain areas in the semiconductor substrate (Fig.2D, numeral 192).

It would have been therefore obvious to one of ordinary skill in the art at the time the invention was made to modify Kwon with Yan to remove the second dielectric film after forming source and drain areas in the semiconductor substrate for the purpose of formation of deep heavily doped diffusion layers (Kwon, [0054]).

Regarding claim 2, Kwon discloses removing the second dielectric film pattern by performing a wet etching process ([0053]).

Regarding claim 3, Kwon discloses that the wet etching process is performed using phosphoric acid as an etching solution ([0053]).

Regarding claim 4, Kwon discloses that the first dielectric film comprises and oxide film and the second dielectric films comprise a nitride film ([0036]).

Kwon does not disclose that the fourth dielectric film comprises an oxide films and the third dielectric film comprises a nitride film.
Kwon however discloses that the materials of the dielectric films can be chosen taking into account an etch selectivity with respect to each other.

It would have been therefore obvious to one of ordinary skill in the art at the time the invention was made to have the fourth dielectric film comprises an oxide film and the third dielectric film comprises a nitride film as an alternative of materials disclosed in Kwon ([0055])

**Regarding claim 5,** Kwon discloses that the nitride film comprises SiN ([0055]) and the oxide films comprises silicon oxide ([0055]).

Kwon does not disclose that the oxide film comprises TEOS.

It would have been however obvious to one of ordinary skill in the art at the time the invention was made to have the oxide film comprising TEOS since it is well-known method for forming silicon oxide films.

**Regarding claim 6,** Kwon discloses sequentially forming the first dielectric film having a thickness in a range between 100 to 300Å ([0036]).

Kwon does not that the second dielectric film having a thickness in a range between 500 to 800Å.

It would have been however obvious to one of ordinary skill in the art at the time the invention was made to adjust the thickness of the second dielectric film to be in the claimed range for the purpose of optimization of the etching and barrier properties.

**Regarding claim 7,** Kwon discloses forming the third dielectric film having a thickness of 100 Å ([0055]).
Kwon does not discloses that the fourth dielectric thickness in a range between 360 to 440 Å.

It would have been however obvious to one of ordinary skill in the art at the time the invention was made to adjust the thickness of the second dielectric film to be in the claimed range for the purpose of optimization of the etching and barrier properties.

**Regarding claim 9**, Yan discloses sequentially stacking a gated oxide film (Fig.1a, numeral 106), a floating gate (Fig.1a, numeral 108), a dielectric film (Fig. 1a, numeral 110) and a control gate (Fig.1A, numeral 112) on the semiconductor substrate (Fig.1a, numeral 104).

**Regarding claim 10**, Kwon discloses after forming the second spacer and before forming the interlayer dielectric film: forming a metal layer (Fig.19, numeral 328) on the semiconductor substrate (Fig.19, numeral 300) included the gate (Fig.19, numeral 306a) and the second spacer (Fig. 19, numeral 332a, 334a) and then forming a silicide layer on the gate and the source/drain area by performing an annealing process on the semiconductor substrate ([0058], [0042]).

**Regarding claim 11**, Kwon discloses that the metal layer comprises cobalt ([0041]).

**Regarding claim 20**, Kwon discloses a method comprising: forming gates spaced apart on a semiconductor substrate (Fig.13, numerals 306a, 306b); and then forming first spacers comprising a first oxide layer (Fig.14, numeral 314) and a first nitride layer (Fig.14, numeral 318) on sidewalls of the gates (Fig.14, numerals 306a, 306b); and then forming source/drain areas in the semiconductor substrate (Fig.16, numeral 326); and
removing the first nitride layer to expose the first oxide layer (Fig.16, [0053]); and then forming second spacers comprising the first oxide layer (Fig.17, numeral 314) and a second nitride layer (Fig. 17, numeral 334) on the sidewalls of the gate (Fig.17, numeral 306a); and then forming silicide layers on the gates and the source/drain areas (Fig.19, numeral 328, [0058]); and then forming an interlayer dielectric film on the semiconductor substrate including the gates, the silicide layers and the second spacers ([0044]); and then forming a contact plug extending through the interlayer dielectric film and electrically connected to the gates, the gate electrode and the source/drain areas ([0044]).

Kwon does not disclose that removing the second dielectric film is performed after forming source and drain areas in the semiconductor substrate.

Kwon however discloses that the source/drain areas can be formed before forming of the silicon epitaxial layer (324) which is formed after removing the second dielectric film (318a) ([0053], [0054]). And Yan discloses removing the second dielectric film (Fig.2D, numeral 193) after forming source and drain areas in the semiconductor substrate (Fig.2D, numeral 192).

It would have been therefore obvious to one of ordinary skill in the art at the time the invention was made to modify Kwon with Yan to remove the second dielectric film after forming source and drain areas in the semiconductor substrate for the purpose of formation deep heavily doped diffusion layers (Kwon, [0054]).

3. Claims 12 -14, and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon in view of Kwak (US 2008/0280442) and Yan.
Regarding claim 12, Kwon discloses a method comprising: forming a gate (Fig.13, numeral 306a) in a cell area of a semiconductor substrate (Fig.13, numeral 10) and a gate electrode (Fig.13, numeral 306b) in a peripheral area of the semiconductor substrate (Fig.13, numeral 20); and then forming first spacers comprising a first dielectric layer (Fig.14, numeral 314) and a second dielectric layer (Fig.14, numeral 318) on sidewalls of the gates and the gate electrode (Fig.15, numeral 306a, 306b); and then forming source/drain areas in the semiconductor substrate (Fig.16, numeral 326); and removing the second dielectric layer to expose the first dielectric layer (Fig.16, [0053]); and then forming second spacers comprising the first dielectric layer (Fig.17, numeral 314a) and a third dielectric layer (Fig. 17, numeral 332) on the sidewalls of the gate (Fig.17, numeral 306a) and the gate electrode (Fig.17, numeral 306b).

Kwon does not disclose (1) that a plurality of gates are formed in a cell area of a semiconductor substrate and (2) that removing the second dielectric film is performed after forming source and drain areas in the semiconductor substrate.

Regarding element (1), Kwak discloses that a plurality of gates is formed in a cell area of a semiconductor substrate (Fig.1A, numeral 107).

It would have been therefore obvious to one ordinary skill in the art at the time the invention was made to modify Kwon with Kwak to form a plurality of gates in a cell area of a semiconductor substrate for the purpose of fabrication a flash memory device (Kwak, [0004]).

Regarding element (2), Kwon discloses that the source/drain areas can be formed before forming of the silicon epitaxial layer (324) which is formed after removing
the second dielectric film (318a) ([0053], [0054]). And Yan discloses removing the second dielectric film (Fig.2D, numeral 193) after forming source and drain areas in the semiconductor substrate (Fig.2D, numeral 192).

It would have been therefore obvious to one of ordinary skill in the art at the time the invention was made to modify Kwon with Yan to remove the second dielectric film after forming source and drain areas in the semiconductor substrate for the purpose of formation deep heavily doped diffusion layers (Kwon, [0054]).

Regarding claim 13, Kwon forming the first dielectric film (Fig.14, numeral 314) against sidewalls of the gate (fig.14, numeral 306a) and the gate electrode (Fig.14, numeral 306b) and on the uppermost surface of the semiconductor substrate (Fig.14, numeral 300); and then forming the second dielectric film (Fig.14, numeral 318) on the first dielectric film (Fig.14, numeral 314); and then performing a first etching process on the first dielectric film and the second dielectric film (Fig.15, [0052]).

Regarding claim 14, Kwon discloses forming the third dielectric film (Fig.17, numeral 332) on the first dielectric film; (Fig.17, numeral 314a) and then forming a fourth dielectric film (Fig.17, numeral 334) on the third dielectric film (Fig.17, numeral 332); and then performing a second etching process on the third dielectric film and the fourth dielectric film (Fig.18, [0056]).

Regarding claim 16, Kwon discloses forming silicide layers (Fig.19, numeral 328) on the gates (Fig.19, numeral 30a), the gate electrodes (Fig.19, numeral 306b) and the source/drain areas (Fig.19, numeral 326); and then forming an interlayer dielectric film on the semiconductor substrate including the gates, the gate electrode, the silicide
layers and the second spacers ([0044]); and then forming a contact plug extending
through the interlayer dielectric film and electrically connected to the gates, the gate
electrode and the source/drain areas ([0044]).

Regarding claim 17, Kwon discloses forming a first metal layer on the
semiconductor substrate including the gates, the gate electrode and the second spacers
(Fig.19, numeral 328); and then performing an annealing process on the semiconductor
substrate ([0042]).

Regarding claim 18, Yan discloses forming via holes (Fig.1D, numeral 126) in the
interlayer dielectric film (Fig.1D, numeral 128) exposing the silicide layers (Fig.1D,
numeral 118); and then forming a second metal layer (Fig.1D, numeral 126) in the via
holes.

Regarding claim 19, Kwon discloses that the first metal layer comprises cobalt
([0041])

Kwon in view of Yan and Kwak does disclose that the second metal layer
comprises tungsten.

It would have been however obvious to one of ordinary skill in the art at the time
the invention was made to have second metal comprising tungsten since this material is
typically used in forming interconnection.

Allowable Subject Matter

4. Claims 8 and 15 are objected to as being dependent upon a rejected base claim,
but would be allowable if rewritten in independent form including all of the limitations of
the base claim and any intervening claims.
5. The following is a statement of reasons for the indication of allowable subject matter: the search of the prior art does not disclose or reasonably suggest removing the entire fourth dielectric film as required by claims 8 and 15.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JULIA SLUTSKER whose telephone number is (571)270-3849. The examiner can normally be reached on Monday-Friday, 8 a.m.-5 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Keisha Bryant can be reached on (571)-272-1844. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic
Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JS
May 14, 2010

/Asok K. Sarkar/
Primary Examiner, Art Unit 2891
May 21, 2010
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Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.
**Search Notes**

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**INTERFERENCE SEARCH**

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**EAST Search History (1 Interference)**

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**INFORMATION DISCLOSURE STATEMENT BY APPLICANT**

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Applicant's unique citation designation number (optional). 

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For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 

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If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.
Mfg. Method of increasing IC assembling density

Application Number: 03150608  Application Date: 2003.08.27
Publication Number: 1591823  Publication Date: 2005.03.09

Priority Information
International Classification: H01L21/82;H01L21/28

Applicant(s) Name: Shanghai Hongli Semiconductor Mfg. Co., Ltd.

Address
Inventor(s) Name: Ye Shuangfeng, Jin Pingzhong


Abstract
The present invention relates to a production method for increasing integrated circuit structure density. Said method includes the following steps: providing a gate structure on a semiconductor base material, forming one oxide thin layer on side surface close to gate structure, and on the oxide thin layer forming and settling a gap wall material, on the gap wall material more forming an oxide, said oxide has a form for covering L-shaped portion of gap wall material, then removing the oxide so as to expose the L-shaped portion of gap wall material. The gate structure with L-shaped gap wall is favorable for filling void and avoiding short circuit of contacting to gate.
发明名称：增加集成电路构装密度的制造方法

摘要
本发明提供一种增加集成电路构装密度的制造方法。其在半导体底材上提供一栅极结构；在紧邻于栅极结构的侧面形成一氧化膜层；於氧化膜层上共形沉积一间隙材料；於间隙材料上再形成一氧化物，此氧化物具有一形状以覆盖间隙材料的一L形部分；接着移除氧化物以暴露出间隙材料的L形部分。此种具有L形间隙的栅极结构有利于间隙充填与避免接触至栅极的短路。
1. 一种增加集成电路构造密度的制造方法，其特征在于，包括下列步骤：
   在一半导体底材上形成一靶极结构;
   在该靶极结构的侧面形成一氧化层;
   在该氧化层上共形沉积一间隙层材料;
   在该间隙层材料上形成一氧化物，该氧化物具有一形状以覆盖该间隙层材料的一L形部分；及
   移除该氧化物以暴露出该间隙层材料的该L形部分。

2. 根据权利要求1所述的增加集成电路构造密度的制造方法，其特征在于，还包含在该氧化物与该半导体底材上沉积一中间介电层。

3. 根据权利要求1所述的增加集成电路构造密度的制造方法，其特征在于，还包含在未被该氧化层层覆盖的该靶极结构上形成一自行对准硅化物填充层。

4. 根据权利要求1所述的增加集成电路构造密度的制造方法，其特征在于，其中该间隙层材料为氮化物材料，较佳的为氮化硅。

5. 一种增加集成电路构造密度的制造方法，其有助于在集成电路中靶极结构之间的间隙填充，其特征在于，包括下列步骤：
   提供至少两靶极结构于一半导体底材上；
   在该半导体底材与该复数个靶极结构上形成一第一氧化层；
   在该第一氧化层上共形沉积一氮化物层，其中相对于该第一氧化层时，该氮化物层具有较厚的一第一厚度；
   在该氮化物层上形成一第二氧化层，其中相对于该氮化物层时，该第二氧化层具有较厚的一第二厚度；及
   移除部分该第一氧化层，该氮化物层与该第二氧化层以暴露出该半导体底材与该等靶极结
6. 根据权利要求 5 所述的增加集成电路结构密度的制造方法，其特征在于，还包含移除该第二氧化层以暴露出该氮化物层的该复数个 L 形部分。

7. 根据权利要求 6 所述的增加集成电路结构密度的制造方法，其特征在于，还包含在该复数个栅极结构与该半导体底材上形成一中间介电层，以及移除介于该复数个栅极结构之间的部分该中间介电层，以形成一接触。

8. 根据权利要求 6 所述的增加集成电路结构密度的制造方法，其特征在于，还包含于在该栅极结构的顶部上形成一自对准硅化物薄膜。

9. 根据权利要求 6 所述的增加集成电路结构密度的制造方法，其特征在于，还包含以该 L 形部分与该栅极结构部分做为一屏蔽，在该半导体底材中植入高子。

10. 根据权利要求 5 所述的增加集成电路结构密度的制造方法，其特征在于，其中该第一厚度实质上为 300 埃。

11. 根据权利要求 5 所述的增加集成电路结构密度的制造方法，其特征在于，其中该第二厚度实质上为 1000 埃。

12. 根据权利要求 5 所述的增加集成电路结构密度的制造方法，其特征在于，其中该提供步骤包含以该栅极结构为一掩蔽，以在该半导体底材中进行离子植入步骤。
说明书

增加集成电路构装密度的制造方法

技术领域

本发明涉及一种其用于改善集成电路中的构装密度（packing density）的制造方法，尤其涉及一种有利于空隙充填（gap-filling）与避免接触至栅极间的短路（contact-to-gate shorts）的制造方法。

背景技术

间隔壁（spacer）为一种紧邻栅极侧面、并且在源极与漏极延伸区上方的结构。较佳的间隔壁为二氧化硅结构，可以选择的其它的材料，例如氮化硅（silicon nitride）、氮氧化硅（silicon oxynitride，SiON）等等也可以做为间隔壁材料。以剖面观察传统的间隔壁，通常为圆柱形状，金氧半导体场效晶体管利用D形间隔壁、三角形氧化物间隔壁、或是梯形氧化物间隔壁，这些形状的间隔壁，有助于分开发源极与漏极延伸区（shallow source and drain extensions）和深源极与漏极接触接合（deep source and drain contact junctions）。

集成电路（IC）长程目标在于尺寸的缩小与构装密度的提升。尺寸缩小的IC减少所占用的面积，对于IC高技术性能是最重要的，且提升的构装密度则可在单位面积上安置更多的半导体元件；此外，IC晶粒面积的减少也可导致IC制造的较高产能，这些优点促使IC尺寸的缩小与构装密度的提升。然而，当欲提升构装密度时，中间介电层（interlayer dielectric）的空隙充填及避免接触至栅极的短路形成一大挑战。传统不同形状的间隔壁，对尺寸的缩小、构装密度的提升、与元件的制造而言，很难有所帮助。
发明内容

本发明所要解决的另一技术问题在于提供一种增加集成电路构装密度的制造方法，其利用深次微米技术形成 L 形间隙壁，以有效提高集成电路的构装密度。

本发明所要解决的另一技术问题是提供一种以深次微米技术制作的制造方法，其有利于空隙充填，避免接触至电极的短路，且 L 形间隙壁有利于空隙的填充，并避免接触之间的短路现象发生。

为了解决上述技术问题，本发明提供一种制造方法，有助于集成电路中的构装密度，包括：提供一集成电路于半导体底材上，并形成一氧化膜层紧邻于集成电路的侧面；共形沉积一间隙膜材料于氧化膜层上，再于间隙膜材料上形成一氧化物层氧化物具有可覆盖间隙膜材料的 L 形结构；接着移除该氧化物以露出间隙膜材料的 L 形部分。

后面通过具体实施例配合所附的图式详加说明，以更容易了解本发明的目的、技术内容、特点及其所达成的功效。

附图说明

图 1-图 3 是根据本发明的 IC 部分的剖面示意图。

图 4 是根据图 3 后沉积一中间介电层的剖视图。

图 5-6 是根据本发明的另一 IC 部分的剖面示意图。

图号说明：

10 底材

12 氧化脂层

14 氧化物材料层（L 形间隙壁）

16 集成电路

18 氧化层

20 中间介电层
22 自行对准硅化物层

具体实施方式

本发明的半导体设计可被广泛地应用到许多半导体设计中，并且可利用许多不同的半导体材料制作，当本发明以较佳实施例来说明本发明方法时，本领域内的普通技术人员应知许多的步骤是可以改变的，材料及杂质也是可替换的，这些一般的替换无疑地不脱离本发明的精神及范围。

其次，本发明用示意图详细描述如下，在详述本发明实施例时，表示半导体结构的剖面图在半导体制程中会不依一般比例作局部放大以利说明，应不能以此作为对本发明的限定。
此外，在实际的制作中，应包含长度、宽度及深度的三维空间尺寸。

图 1 至图 3 为根据本发明的 IC 部分的剖面示意图。如图 1 所示，此部分包含一底材 10、一栅极结构 16、一氧化膜层 12、一氮化物材料层 14 以及一氧化层 18。此一部份可做为半导体晶片，例如硅晶片上 IC 的一部份。底材 10 可以是任何适当的半导体材料，在一实施例中，底材 10 为硅材料，亦可包含若干并入其中；栅极结构 16 可以是任何适当的导体材料，且在此一实施例中，栅极结构 16 为多晶硅材料，而氮化物材料层 14 则为一氮化硅材料或其它间隙壁材料；氧化膜层 12 以适当的方法形成，并紧邻于栅极结构 16 的侧边（lateral sides），其厚度约为 100 埃；氮化物材料层 14 系作为一间隔膜，共形（conformally）沉积于氧化膜层 12 上，其厚度约为 300 埃；以及该氧化层 18 是以适当的方法形成，其具有一厚度大于氮化物材料层 14 的厚度，例如 1000 埃。

如图 2 所示，部分的氧化层 18、氮化物材料层 14 及氧化膜层 12 以蚀刻方式移除，之后暴露出底材 10 与栅极结构 16 的顶部，剩余的氧化层 18 覆盖氮化物材料层 14 及氧化膜层 12 的 L 形部分；此氮化物材料层 14 及氧化膜层 12 的 L 形部分紧邻于栅极结构 16 的侧壁。

接着，如图 3 所示，剩余的氧化层 18 以适当的蚀刻方法移除，氮化物材料层 14 的 L 形部分未被覆盖，其即可视为栅极结构 16 的 L 形间隙壁 14 的一部分。根据本发明，栅极结构
16 的 L 形间隙壁 14 的设计有助于构成密度，因为其使得空隙充填变得很容易，并且避免栅极与接触的短路。如图 2 所示，当进行中间介电层 20 的沉积时，因为 L 形间隙壁 14 不会妨碍中间介电层 20 的充填，因此介于栅极结构 16 之间的微小空隙可以如半导体的其它部分一样顺利充填。因此，L 形间隙壁 14 有助于中间介电层 20 的充填，进而增加 IC 的构成密度。

要了解的是，有许多植入步骤介于上述步骤中，举例来说，例如在氧化膜层 12 形成之前，以栅极结构 16 做为植入掩蔽，对基材 10 进行离子植入步骤，以作为轻掺杂极区域；另在后续步骤进行之前，以栅极结构 16 与 L 形间隙壁 14 作为另一植入掩蔽，对该基材 10 内进行离子植入，以作为深极与漂移区域。

图 5、图 6 为根据本发明的另一 IC 部分的剖面示意图。如图 5 所示，若干设计需在栅极结构 16 的顶部首先形成对准硅化物层 22，之后中间介电层 20 再沉积于基材 10 与栅极结构 16 上。如图 6 所示，移除部分的中间介电层 20，以在栅极结构 16 形成接触。

因此，相较于传统形状间隙壁，当后续完成接触后，本发明的 L 形间隙壁可避免接触至栅极的短路，因此，本发明的优点之一是可避免接触至栅极的短路。

以上所述的实施例仅用于说明本发明的技术思想及特点，其目的在于使本领域内的普通技术人员能够了解本发明的内容并据以实施，并不以此作为限定本发明的专利范围，即凡依本发明所揭示的精神所作的均等变化或修饰，仍应涵盖在本发明的专利范围内。
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**Title of Invention:** METHOD OF MANUFACTURING FLASH MEMORY DEVICE

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Applicant(s)  
Hyun-Ju Lim, Mapo-gu, KOREA, REPUBLIC OF;

Power of Attorney: None

Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted: 07/09/2008

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is US 12/146,486

Projected Publication Date: 01/01/2009

Non-Publication Request: No

Early Publication Request: No
METHOD OF MANUFACTURING FLASH MEMORY DEVICE

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Hyun-Ju Lim

Docket No.: 604-0170

Confirmation No.: 5212

Application No.: 12/146,486

Group Art Unit:

Filed: June 26, 2008

Examiner:

For: METHOD OF MANUFACTURING FLASH MEMORY DEVICE

Commissioner for Patents
P.O. BOX 1450
Alexandria, VA 22313-1450

CLAIM FOR PRIORITY UNDER 35 USC §119

Sir:

Priority under 35 U.S.C. § 119 is hereby claimed to the following priority document(s), filed in a foreign country within twelve (12) months prior to the filing of the above-referenced United States utility patent application:

<table>
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<th>Country</th>
<th>Priority Document Application No.</th>
<th>Filing Date</th>
</tr>
</thead>
</table>

A certified copy of the above listed application is attached. Prompt acknowledgment of the aforementioned claim is respectfully requested.

Respectfully Submitted,

[Signature]

Todd A. Vaughn
Reg. No. 52,319

Sherr & Nourse, PLLC
620 Herndon Parkway
Suite 200
Herndon, Virginia 20170
Tel: 703-673-1141
Fax: 703-935-8473
This is to certify that the following application annexed hereto is a true copy from the records of the Korean Intellectual Property Office.

Application Number: 10-2007-0062648

Filing Date: Jun 26, 2007

Applicant(s): Dongbu HiTek Co., Ltd.

Commissioner

Issue Date: 2008.05.30
출원번호: 10-2007-0062648

【서지사항】

【서류명】 특허출원서
【권리구분】 특허
【수신처】 특허청장
【참조번호】 1088
【제출일자】 2007.06.26
【국제특허분류】 H01L
【발명의 국문명칭】 플래시 메모리 소자의 제조 방법
【발명의 영문명칭】 Method of manufacturing flash memory device

【출원인】

【명칭】 주식회사 동부하이텍
【출원인코드】 1-1998-000857-5

【대리인】

【성명】 허용록
【대리인코드】 9-1998-000616-9
【포괄위임등록번호】 2007-040671-5

【발명자】

【성명】 임현주
【성명의 영문표기】 LIM, HYUN JU
【주민등록번호】 780124-2XXXXX
【우편번호】 121-841
【주소】 서울 마포구 서교동 446-40 현대하이츠빌라 302호
【국적】 KR
【심사청구】 청구
출원번호: 10-2007-0062648

【취지】 특허법 제42조의 규정에 의한 출원, 특허법 제60조의 규정에 의한 심사청구를 합니다.

대리인

허용록 (인)

【수수료】

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【요약서】

【요약】

실시에는 반도체 기판 상에 게이트를 형성하는 단계; 상기 반도체 기판 상에 제1철연막 및 제2철연막을 형성하고, 제1식각공정으로 상기 게이트 측벽에 제1철연막 패턴 및 제2철연막 패턴을 형성하는 단계; 상기 반도체 기판에 소오스 및 드레인 영역을 형성하는 단계; 상기 제2철연막 패턴을 제거하고, 상기 반도체 기판상에 제3철연막 및 제4철연막을 형성하는 단계; 상기 제3철연막 및 제4철연막에 제2식각공정을 진행하여, 상기 게이트 측벽에 상기 제1철연막 패턴 및 제2철연막 패턴으로 형성된 스페이서를 형성하는 단계; 상기 게이트 및 스페이서가 형성된 상기반도체 기판 상에 중간철연막을 형성하는 단계를 포함한다.

실시에는 중간철연막 형성시 보이드의 발생을 방지할 수 있다.

【대표도】

도 11

【책임자】

플래시 메모리
출원번호: 10-2007-0062648

【명세서】

【발명의 명칭】
플래시 메모리 소자의 제조 방법 (Method of manufacturing flash memory device)

【도면의 간단한 설명】

<1> 도 1 내지 도 11은 실시예에 따른 플래시 메모리 소자의 공정 단면도이다.

【발명의 상세한 설명】

【발명의 목적】

【발명이 속하는 기술분야 및 그 분야의 종래기술】

<2> 실시예에는 플래시 메모리 소자에 관한 것이다.

<3> 플래시 메모리 소자는 전원이 깨지더라도 저장된 데이터가 손상되지 않는 비휘발성 기억매체이며서도 데이터의 기록, 읽기, 삭제 등의 처리 속도가 비교적 높다는 장점이 있다.

<4> 이에 따라, 상기 플래시 메모리 소자는 PC의 BIOS용, 셋탑 박스, 프린터 및 네트워크 서버 등의 데이터 저장용으로 널리 사용되고 있으며 최근에는 디지털 카메라와 휴대폰 등에서도 많이 이용되고 있다.

<5> 그러나, 소자가 고점적화됨에 따라 플래시 메모리의 단위 셀의 크기가 작아지고, 단위 셀을 이루는 게이트 영역과 게이트 영역 사이의 간격이 줄기 때문에 금속배선 형성시 보이드가 발생하게 된다.
출원번호: 10-2007-0062648
【발명이 이루고자 하는 기술적 파계】

실시예는 중간절연막 형성시 보이드의 발생을 방지하기 위한 플래시 메모리 소자의 제조 방법을 제공한다.

【발명의 구성】

실시예는 반도체 기판 상에 게이트를 형성하는 단계; 상기 반도체 기판 상에 제1절연막 및 제2절연막을 형성하고, 제1식각공정으로 상기 게이트 측벽에 제1절연막 패턴 및 제2절연막 패턴을 형성하는 단계; 상기 반도체 기판에 소오스 및 드레인 영역을 형성하는 단계; 상기 제2절연막 패턴을 제거하고, 상기 반도체 기판 상에 제3절연막 및 제4절연막을 형성하는 단계; 상기 제3절연막 및 제4절연막에 제2식각공정을 진행하여, 상기 게이트 측벽에 상기 제1절연막 패턴 및 제3절연막 패턴으로 형성된 스페이서를 형성하는 단계; 상기 게이트 및 스페이서가 형성된 상기 반도체 기판 상에 중간절연막을 형성하는 단계를 포함한다.

이하, 실시예를 첨부 도면을 참조하여 설명하기로 한다.

도 1 내지 도 11은 실시예에 따른 플래시 메모리 소자의 공정 단면도이다.

도 1에 도시된 바와 같이, 셀 영역과 폐리 영역으로 이루어진 반도체 기판(10) 상에 게이트(20) 및 게이트 전극(18)을 형성한다.

상기 셀 영역에는 제1게이트 산화막(11), 폼로팅 게이트(12), 유전체막(14) 및 제어 게이트(16)가 형성된 게이트(20)가 형성되며, 상기 폐리 영역에는 제2게이트 산화막(17) 및 게이트 전극(18)이 형성된다.
상기 플로팅 게이트(12), 제어 게이트(16) 및 게이트 전극(18)은 볼리실리콘으로 형성될 수 있으며, 상기 유전체막(14)은 OX(Nitride-Oxide)의 구조로 이루어져 상기 플로팅 게이트(12)와 제어 게이트(16)를 절연하는 역할을 한다.

상기 플로팅 게이트(12)는 데이터가 저장되고, 상기 제어 게이트(16)는 하부에 형성된 상기 플로팅 게이트(12)에 전자를 여기서 충전(charging) 또는 방전(discharging)을 하도록 하는 바이어스 전압을 인가하는 역할을 한다.

이어서, 도 2에 도시된 바와 같이, 상기 게이트(20) 및 게이트 전극(18)이 형성된 상기 반도체 기판(10) 상에 제1산화막(Oxide, 30) 및 제1질화막(nitride, 32)을 순차적으로 적층하여 스페이서막(34)을 형성한다.

상기 제1산화막(30)은 TEOS(Tetra Ethyl Ortho Silicate)가 100-300 A의 두께로 형성되며, 상기 제1질화막(32)은 500-800 A의 두께를 갖는 질화규소(SiN)막으로 형성될 수 있다.

그리고, 도 3에 도시된 바와 같이, 상기 2층막 구조로 형성된 상기 스페이서막(34)에 식각공정을 진행하여, 상기 게이트(20) 및 게이트 전극(18)의 측벽에 제1산화막 패턴(39) 및 제1질화막 패턴(38)을 형성한다.

이어서, 도 4에 도시된 바와 같이, 상기 제1질화막 패턴(38)를 마스크로 이용주입 공정을 진행하여 상기 반도체 기판(10)에 고농도 불순물 영역인 소오스/드리 인 영역(42)을 형성한다.

그리고, 도 5에 도시된 바와 같이, 상기 제1질화막 패턴(38)을 제거한다.
상기 제1절화막 패턴(38)을 제거함으로써, 충간절연막 형성 전, 상기 셀 영역에 형성된 상기 게이트(20) 사이의 간격을 충분히 확보할 수 있다.

따라서, 이후 진행되는 충간절연막 형성시 보이드의 발생을 방지할 수 있다.

또한, 이후 콘택을 형성하기 위한 공정마진을 충분히 확보하고, 제거되는 상기 제1절화막 패턴(38)의 두께만큼 상기 게이트(20) 사이의 간격을 좁혀 소자의 집적도를 증가시킬 수 있게 된다.

상기 제1절화막 패턴(38)은 습식식각 공정을 진행하여 제거되며, 상기 습식식각 공정에는 인산(H₃PO₄)을 사용한다.

이어서, 도 6에 도시된 바와 같이, 상기 반도체 기판(10) 전면에 제2절화막(50)을 형성한다. 상기 제2절화막(50)은 질화규소(SiN)로 형성될 수 있으며, 70-200 Å의 두께로 형성될 수 있다.

상기 제2절화막(50)은 후속 공정인 샐리사이드(salicide) 공정으로 게이트(20) 및 게이트 전극(18)의 측벽에 남겨진 상기 제1산화막 패턴(39)이 샐리사이드가 이루어져, 비경상적인 소자특성이 발생되는 것을 방지한다.

상기 제1절화막 패턴(38) 제거 과정에서 정확히 일정량의 질화막을 남기도록 제어하는 데 공정상 한계가 있기 때문에, 후속에서 재 중착을 시행하는 것이 공정상 더욱 안정적인 방법이다.

그러고, 도 7에 도시된 바와 같이, 상기 제2절화막(50) 상에 제2산화막(55)을 형성한다.
상기 제2산화막(55)은 TEOS로 형성될 수 있으며, 360~440 A의 두께로 형성될 수 있다.

그리고, 도 8에 도시된 바와 같이, 상기 제2산화막(55) 및 제2질화막(50)에 식각 공정을 진행하여, 상기 게이트(20) 및 게이트 전극(18)의 측벽에 제1산화막 패턴(39) 및 제2질화막 패턴(52)으로 이루어진 스페이서(54)를 형성한다.

상기 식각 공정으로 상기 게이트(20), 게이트 전극(18) 및 소오소/드레인 영역(42) 상에 형성된 상기 제2질화막(50) 및 제2산화막(55)은 제거되고, 상기 제1산화막(39)의 측벽에 제2질화막 패턴(52)이 남게 된다.

이어서, 도 9에 도시된 바와 같이, 상기 반도체 기판(10) 상에 실리사이드 형성 금속(57)을 충착한다.

상기 실리사이드 형성 금속(57)으로는 코발트(Co)를 사용할 수 있다.

이어서, 상기 반도체 기판(10) 전면에 열처리 공정을 진행하여, 도 10에 도시된 바와 같이, 상기 게이트(20) 상부 및 소스/드레인 영역(42)에서 실리콘과 금속의 반응을 유도하여 금속 실리사이드(59)를 각각 형성한다.

상기 열처리 공정으로 금속 실리사이드는 금속이 실리콘 및 플리실리콘과 접촉하는 영역에만 형성되고, 그 외의 영역에서는 금속과 실리콘의 반응이 차단되므로 실리사이드가 형성되지 않는다.

이와 같이 상기 게이트(20) 및 소스/드레인 영역(42)에 동시에 상기 실리사이드(59)를 형성한 후, 반응하지 않은 상기 실리사이드 형성 금속(57)은 선택적 식
이어서, 도 11에 도시된 바와 같이, 상기 반도체 기판(10) 상에 충간절연막 (60)을 형성한다.

상기 충간절연막(60)은 PMD(Pre Metal Dielectric)로써, PSG(Phosphorus Silicate Glass), BPSG(Boro-Phosphorus Silicate Glass) 또는 USG(undoped silicate glass)가 사용된다.

상기 제1절화막 패턴(38)을 제거해 상기 게이트(20) 사이의 면적을 충분히 확보했으므로, 상기 충간절연막(60) 형성시 보이드가 발생하지 않는다.

이어서, 도시되지 않았지만 상기 충간절연막(60)을 선택적으로 식각하여 비아홀을 형성한 후, 상기 비아홀에 텅스텐(W)을 매립하여 콘택 플러그를 형성한다.

상기 콘택 플러그의 형성으로 상기 게이트(20) 및 소스/드레인 영역(42)과 전기적으로 연결될 수 있다.

상기 충간절연막(60) 형성시 보이드가 발생되지 않았기 때문에 상기 콘택 플러그 형성시 보이드에 의한 확산현상이 나타나지 않으므로 플래시 메모리 소자는 정상적인 동작을 수행할 수 있게 된다.

또한, 상기 텅스텐 콘택 플러그 형성 후, 보이드에 의한 소자 간의 브리지를 방지할 수 있다.

이상에서 설명한 바와 같이, 실시예에 의한 플래시 메모리 소자의 제조 방법에 의하면 게이트 사이에 충분한 공간을 확보해 주므로써, 충간절연막 형성시 보이
이로 인해, 콘택 플러그 형성시 텅스텐에 의한 소자 간의 브리지를 제거하여 플래시 메모리 소자의 신뢰성을 확보할 수 있을 뿐만 아니라 소자의 고정적화를 실현할 수 있다.

이상에서 실시예를 중심으로 설명하였으나 이는 단지 예시일 뿐 본 발명을 한정하는 것이 아니며, 본 발명이 속하는 분야의 통상의 지식을 가진 자라면 본 실시예의 본질적인 특성을 벗어나지 않는 범위에서 이상에 예시되지 않은 여러 가지의 변형과 응용이 가능함을 알 수 있을 것이다. 예를 들어, 실시예에 구체적으로 나타난 각 구성 요소는 변형하여 실시할 수 있는 것이다. 그리고 이러한 변형과 응용에 관계된 차이점들은 첨부된 청구 범위에서 규정하는 본 발명의 범위에 포함되는 것으로 해석되어야 할 것이다.

【발명의 효과】

실시예는 층간절연막 형성시 보이드의 발생을 방지할 수 있다.
【특허청구범위】

【청구항 1】
반도체 기판 상에 채이트를 형성하는 단계;
상기 반도체 기판 상에 에 제1절연막 및 제2절연막을 형성하고, 제1식각공정
으로 상기 채이트 측벽에 제1절연막 패턴 및 제2절연막 패턴을 형성하는 단계;
상기 반도체 기판에 소오스 및 드레인 영역을 형성하는 단계;
상기 제2절연막 패턴을 제거하고, 상기 반도체 기판 상에 제3절연막 및 제4
절연막을 형성하는 단계;
상기 제3절연막 및 제4절연막에 제2식각공정을 진행하여, 상기 채이트 측벽
에 상기 제1절연막 패턴 및 제3절연막 패턴으로 형성된 스페이서를 형성하는 단계;
상기 채이트 및 스페이서가 형성된 상기 반도체 기판 상에 충전절연막을 형
성하는 단계를 포함하는 플래시 메모리 소자의 제조 방법.

【청구항 2】
제 1항에 있어서,
상기 제2절연막 패턴은 습식식각 공정을 진행하여 제거하는 것을 포함하는
플래시 메모리 소자의 제조 방법.

【청구항 3】
제 2항에 있어서,
출원번호: 10-2007-0062648
상기 습식식각 공정시 식각용액으로는 인산(H₃PO₄) 용액이 사용되는 것을 포함하는 플레시 메모리 소자의 제조 방법.

【청구항 4】

제 1항에 있어서,
상기 제1절연막 및 제4절연막은 산화막이고, 상기 제2절연막 및 제3절연막은 절화막인 것을 포함하는 플레시 메모리 소자의 제조 방법.

【청구항 5】

제 4항에 있어서,
상기 산화막은 TEOS이고, 상기 절화막은 SiN인 것을 포함하는 플레시 메모리 소자의 제조 방법.

【청구항 6】

제 4항에 있어서,
상기 제1절연막은 100~300 A, 상기 제2절연막은 500~800 A, 상기 제3절연막은 70~200 A, 상기 제4절연막은 360~440 A의 두께로 형성된 것을 포함하는 플레시 메모리 소자의 제조 방법.

【청구항 7】

제 1항에 있어서,
상기 제2식각공정시,
출원번호: 10-2007-0062648
상기 게이트 상부, 소오스 및 드레인 영역에 형성된 상기 제3절연막 및 제4
절연막이 모두 제거되는 것을 포함하는 폴레시 메모리 소자의 제조 방법.

【청구항 8】

제 1항에 있어서,

상기 게이트는 게이트 산화막, 플로팅 게이트, 유전체막 및 제어 게이트의
적층으로 형성된 것을 포함하는 폴레시 메모리 소자의 제조 방법.

【청구항 9】

제 1항에 있어서,

상기 충간절연막을 형성하기 전,

상기 게이트 및 스페이서가 형성된 반도체 기판 상에 실리사이드 형성 금속
을 증착하는 단계;

상기 반도체 기판 전면에 열처리 공정을 진행하여, 상기 게이트의 상부 및
소스/드레인 영역에 실리사이드를 형성하는 단계; 및

반응하지 않은 상기 실리사이드 형성 금속을 제거하는 단계를 더 포함하는
폴레시 메모리 소자의 제조 방법.

【청구항 10】

제 9항에 있어서,

상기 실리사이드 형성 금속은 코발트(Co)인 것을 포함하는 폴레시 메모리 소
자의 제조 방법.
출원번호: 10-2007-0062648

【도면】

【도 1】

Cell Area  Peri Area

【도 2】

Cell Area  Peri Area

【도 3】

Cell Area  Peri Area
출원번호: 10-2007-0062648

【도 4】

【도 5】

【도 6】
DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

Attorney Docket Number: 604-0170

First Name: Hyun-Ju

Last Name: Lim

Application Number: COMPLETE IF KNOWN

Filing Date: June 26, 2008

Art Unit: TSA

Examiner Name: TSA

I hereby declare that:

Each inventor’s residence, mailing address, and citizenship are as stated below next to their name.

I believe the inventor(s) named below to be the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD OF MANUFACTURING FLASH MEMORY DEVICE

(Title of the Invention)

is attached hereto

OR

was filed on (MM/DD/YYYY)

as United States Application Number or PCT International Application Number

and was amended on (MM/DD/YYYY) (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the priority application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)–(d) or (f), or 365(b) of any foreign application(s) for patent, inventor’s or plant breeder’s rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America listed below and have also identified below, by checking the box, any foreign application for patent, inventor’s or plant breeder’s rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)

Country

Foreign Filing Date

Priority Not Claimed

Certified Copy Attached?

10-2007-0062848

KR

06/28/2007

Yes

No

Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 21 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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DECLARATION — Utility or Design Patent Application

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Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioners/applicants are advised that the record of a patent application is available to the public after publication of the application (unless a non-disclosure request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

NAME OF SOLE OR FIRST INVENTOR:

☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any]) Family Name or Surname

Hyun-Ju Lim

Inventor's Signature Date

Residence City State Country Citizenship

Maipo-gu Seoul Republic of Korea Republic of Korea

Mailing Address

4022, Hyan Dal High Village, Seoogyo-dong

City State Zip Country

Maipo-gu Seoul

Republic of Korea

☐ Additional inventors or a legal representative are being named on the supplemental sheet(s) PTO/DS/20A or CDR attached hereto.
METHOD OF MANUFACTURING FLASH MEMORY DEVICE


BACKGROUND

Flash memory devices are non-volatile memory media in which stored data is not lost even when power is turned off. Flash memory devices can be advantageous in having a high processing speed when operations are performed such as recording, reading, and deleting, etc. Therefore, flash memory devices have been widely used in data storage for Bios for personal computers (PC), a set-top box, a printer, and a network server, etc. Recently, flash memory devices have widespread application in devices such as digital cameras and cellular phones.

However, as flash memory devices have become more highly integrated, the size of a unit cell of the flash memory is reduced, and in turn, the spatial interval between gate areas forming the unit cell are also reduced so that voids are generated when forming a metal wire.

SUMMARY

Embodiments relate to a method of manufacturing a flash memory device for preventing a generation of voids when forming an interlayer dielectric film.

Embodiments relate to a method of manufacturing a flash memory device including at least one of the following steps: forming a gate on and/or over a semiconductor substrate; and then sequentially stacking a first dielectric film and a second dielectric film on and/or over the
semiconductor substrate and forming a first dielectric pattern and a second dielectric pattern on and/or over sidewalls of the gate through a first etching process; and then forming source and drain regions on and/or over the semiconductor substrate; and then removing the second dielectric pattern and forming a third dielectric film on and/or over the semiconductor substrate; and then performing a second etching process on the third dielectric film to form a spacer formed in the first dielectric pattern and the third dielectric pattern on and/or over the gate sidewalls; and then forming an interlayer dielectric film on and/or over the semiconductor substrate formed with the gate and the spacer.

Embodiments relate to a method including at least one of the following steps: forming a gate on a semiconductor substrate; and then sequentially stacking a first dielectric film and a second dielectric film on the semiconductor substrate; and then forming a first spacer comprising a first dielectric film pattern and a second dielectric film pattern on sidewalls of the gate by performing a first etching process; and then forming source and drain areas in the semiconductor substrate; and then removing the second dielectric film; and then sequentially stacking a third dielectric film and a fourth dielectric film on the semiconductor substrate; and then forming a second spacer comprising the first dielectric pattern and a third dielectric pattern on the sidewalls of the gate by performing a second etching process; and then forming an interlayer dielectric film on the semiconductor substrate including the gate and the first spacer.

Embodiments relate to a method including at least one of the following steps: forming a plurality of gates in a cell area of a semiconductor substrate and a gate electrode in a peripheral area of the semiconductor substrate; and then forming first spacers comprising a first dielectric layer and a second dielectric layer on sidewalls of the gates and the gate electrode; and then forming source/drain areas in the semiconductor substrate; and then removing the second
dielectric layer to expose the first dielectric layer; and then forming second spacers comprising the first dielectric layer and a third dielectric layer on the sidewalls of the gate and the gate electrode.

Embodiments relate to a method including at least one of the following steps: forming gates spaced apart on a semiconductor substrate; and then forming first spacers comprising a first oxide layer and a first nitride layer on sidewalls of the gates; and then forming source/drain areas in the semiconductor substrate; and then removing the first nitride layer to expose the first oxide layer; and then forming second spacers comprising the first oxide layer and a second nitride layer on the sidewalls of the gate; and then forming silicide layers on the gates and the source/drain areas; and then forming an interlayer dielectric film on the semiconductor substrate including the gates, the silicide layers and the second spacers; and then forming a contact plug extending through the interlayer dielectric film and electrically connected to the gates, the gate electrode and the source/drain areas.

**DRAWINGS**

Example FIGS. 1 to 11 illustrate a method of manufacturing a flash memory device in accordance with embodiments.

**DESCRIPTION**

As illustrated in example FIG. 1, gate electrode 18 and gate 20 and are formed on and/or over semiconductor substrate 10 formed having a cell region or area cell area and a peripheral (peri) region or area. In the cell area, gate 20 may be formed including first gate oxide 11, floating gate 12, dielectric film 14 and control gate 16. In the peripheral area, second gate oxide
film 17 and gate electrode 18 are formed. Floating gate 12, control gate 16 and gate electrode 18 may be made of polysilicon. Dielectric film 14 may be formed having an oxide-nitride-oxide (ONO) structure for insulating floating gate 12 from control gate 16. Floating gate 12 may serve to store data while control gate 16 may serve to apply bias voltage exciting electrons to floating gate 12 formed below to charge or discharge the electrons.

As illustrated in example FIG. 2, spacer film 34 may then be formed on and/or over semiconductor substrate 10 including gate 20 and gate electrode 8. Spacer film 34 may be formed by sequentially stacking first oxide film 30 and first nitride film 32. First oxide film 30 may be formed of tetra ethyl ortho silicate (TEOS) having a thickness in a range between 100 to 300Å. First nitride film 32 may be formed of silicon nitride (SiN) having a thickness in a range between 500 to 800Å.

As illustrated in example FIG. 3, spacer film 34 formed in a bi-layer structure may then be subject to an etching process to form a first spacer composed of first oxide film pattern 39 and first nitride film pattern 38 on sidewalls of gate 20 and gate electrode 18. For example, first oxide film pattern 39 may be formed directly against sidewalls of gate 20 and gate electrode 18 and also on and/or semiconductor substrate 10. First nitride film pattern 38 may be formed on and/or over first oxide film pattern 39.

As illustrated in example FIG. 4, an ion-implant process may then be performed using first nitride film pattern 38 as a mask to form source/drain region 42 serving as a high-concentration impurity region or area in semiconductor substrate 10.

As illustrated in example FIG. 5, first nitride film pattern 38 may then be removed after the ion-implantation process is performed. First nitride film pattern 38 may be removed by performing a wet etching process. The wet etching process may include phosphoric acid (H₃PO₄).
Removal of first nitride film pattern 38 makes it possible to sufficiently secure a spatial interval between gates 20 formed in the cell area, before forming an interlayer dielectric film. Therefore, generation of voids may be prevented when subsequently forming an interlayer dielectric film and a process margin for forming a contact later may be sufficiently secured. Moreover, a spatial interval between gates 20 may be reduced in accordance with the thickness of the removed first nitride film pattern 38, thereby making it possible to increase integration of the device.

As illustrated in example FIG. 6, second nitride film 50 may then be formed on and/or over semiconductor substrate 10 including gates 20 in the cell area and gate electrode 18 in the peri area. Second nitride film 50 may be made of silicon nitride (SiN) having a thickness in a range of between 70 to 200Å. Second nitride film 50 may serve to prevent generation of abnormal device property resulting from the subsequent formation of a salicide on and/or over first oxide film pattern 39 through a salicide process. Since there is a process limit in controlling a predetermined amount of nitride film to be maintained during the process removing first nitride film pattern 38, it is a more stable method to perform a re-deposition in a subsequent process.

As illustrated in example FIG. 7, second oxide film 55 may then be formed on and/or over second nitride film 50. Second oxide film 55 may be made of TEOS having a thickness in a range of between 360 to 440Å.

As illustrated in example FIG. 8, an etching process may then be performed on second oxide film 55 and second nitride film 50, thereby forming second spacer 54 composed of first oxide film pattern 39 and second nitride film pattern 52 against the sidewalls of gate 20 and gate electrode 18. During the etching process, a portion of second nitride film 50 and the entire second oxide film 55 formed on and/or over gate 20, gate electrode 18 and source/drain region 42 are removed.
As illustrated in example FIG. 9, silicide-forming metal 57 may then be deposited on and/or over semiconductor substrate 10 including gates 20 formed in the cell area, gate electrode 18 formed in the peri area, spacer 54 and first oxide film pattern 39. Silicide-forming metal 57 may be made of cobalt (Co).

As illustrated in example FIG. 10, an annealing process may then be performed on and/or over semiconductor substrate 10 to induce a reaction between silicon and metal, thereby simultaneously forming metal silicide layer 59 on and/or over the uppermost surface of gates 20, gate electrode 18 and source/drain regions 42, respectively. Through the annealing process, metal silicide layer 59 may be formed only in areas where metal contacts silicon and polysilicon. In turn, metal silicide layer 59 may not be formed in other areas since a reaction between metal and silicon is blocked. After simultaneously forming metal silicide 59 on gates 20, gate electrode 18 and source/drain areas 42, silicide-forming metal 57 not reacted with silicon and polysilicon may be removed through a selective etching process.

As illustrated in example FIG. 11, interlayer dielectric film 60 may then be formed on and/or over semiconductor substrate 10 including gates 20 formed in the cell area, gate electrode 18 formed in the peri area, spacer 54, first oxide film pattern 39 and metal silicide layer 59. Interlayer dielectric film 60 may be a pre-metal dielectric (PMD) film and be made of at least one of phosphorus silicate glass (PSG), boro-phosphorus silicate glass (BPSG) and undoped silicate glass (USG). In accordance with embodiments, a sufficient space between gates 20 may be secured by removing first nitride film pattern 38 so that voids between gates 20 are not generated when forming interlayer dielectric film 60. At least one via hole may be formed in interlayer dielectric film 60 exposing metal silicide layer 59 by selectively etching interlayer dielectric film 60. A metal layer made of tungsten (W) may then be buried in the via hole to form
a contact plug electrically connected to gate 20 and source/drain area 42. In accordance with embodiments, since voids are not generated when forming interlayer dielectric film 60, a diffusion phenomenon due to the void is not generated when forming the contact plug. In turn, the flash memory device can have enhanced performance during operation. Moreover, prevention of void formation also prevents formation of bridges when the contact plug is formed.

In accordance with embodiments, a method of manufacturing a flash memory device secures a sufficient space between gates, thereby making it possible to prevent generation of voids when forming an interlayer dielectric film. Thereby, a bridge between devices due to the removal of the metal layer when forming a contact plug is prevented, making it possible to secure reliability of the flash memory device as well as to realize high integration of the device.

Although embodiments have been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the spirit and scope of the principles of this disclosure. More particularly, various variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the disclosure, the drawings and the appended claims. In addition to variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.
WHAT IS CLAIMED IS:

1. A method comprising:
   forming a gate on a semiconductor substrate; and then
   sequentially stacking a first dielectric film and a second dielectric film on the semiconductor substrate; and then
   forming a first spacer comprising a first dielectric film pattern and a second dielectric film pattern on sidewalls of the gate by performing a first etching process; and then
   forming source and drain areas in the semiconductor substrate; and then
   removing the second dielectric film; and then
   sequentially stacking a third dielectric film and a fourth dielectric film on the semiconductor substrate; and then
   forming a second spacer comprising the first dielectric pattern and a third dielectric pattern on the sidewalls of the gate by performing a second etching process; and then
   forming an interlayer dielectric film on the semiconductor substrate including the gate and the first spacer.

2. The method of claim 1, wherein removing the second dielectric pattern comprises:
   removing the second dielectric film pattern by performing a wet etching process.

3. The method of claim 2, wherein the wet etching process is performed using phosphoric acid (H₃PO₄) as an etching solution.
4. The method of claim 1, wherein the first and fourth dielectric films comprise an oxide film and the second and third dielectric films comprise a nitride film.

5. The method of claim 4, wherein the oxide film comprises TEOS and the nitride film comprises SiN.

6. The method of claim 1, wherein sequentially stacking the first dielectric film and the second dielectric film comprises:
   sequentially forming the first dielectric film having a thickness in a range between 100 to 300Å and the second dielectric film having a thickness in a range between 500 to 800Å.

7. The method of claim 1, wherein sequentially stacking the third dielectric film and the fourth dielectric film comprises:
   forming the third dielectric film having a thickness in arrange between 70 to 200Å and the fourth dielectric film having a thickness in a range between 360 to 440Å.

8. The method of claim 1, wherein forming the second spacer comprises:
   performing the second etching process removing a portion of the third dielectric film and the entire fourth dielectric film.

9. The method of claim 1, wherein forming the gate includes sequentially stacking a gate oxide film, a floating gate, a dielectric film and a control gate on the semiconductor substrate.
10. The method of claim 1, further comprising, after forming the second spacer and before forming the interlayer dielectric film:

    forming a metal layer on the semiconductor substrate including the gate and the second spacer; and then

    forming a silicide layer on the gate and the source/drain area by performing an annealing process on the semiconductor substrate.

11. The method of claim 10, wherein the metal layer comprises cobalt.

12. A method comprising:

    forming a plurality of gates in a cell area of a semiconductor substrate and a gate electrode in a peripheral area of the semiconductor substrate; and then

    forming first spacers comprising a first dielectric layer and a second dielectric layer on sidewalls of the gates and the gate electrode; and then

    forming source/drain areas in the semiconductor substrate; and then

    removing the second dielectric layer to expose the first dielectric layer; and then

    forming second spacers comprising the first dielectric layer and a third dielectric layer on the sidewalls of the gate and the gate electrode.

13. The method of claim 12, wherein forming the first spacers comprises:

    forming the first dielectric film against sidewalls of the gate and the gate electrode and on the uppermost surface of the semiconductor substrate; and then

    forming the second dielectric film on the first dielectric film; and then
performing a first etching process on the first dielectric film and the second dielectric film.

14. The method of claim 12, wherein forming the second spacers comprises:
forming the third dielectric film on the first dielectric film; and then
forming a fourth dielectric film on the third dielectric film; and then
performing a second etching process on the third dielectric film and the fourth dielectric film.

15. The method of claim 14, wherein performing the second etching process comprises:
removing a portion of the third dielectric film and the entire fourth dielectric film.

16. The method of claim 12, further comprising, after forming the second spacers:
forming silicide layers on the gates, the gate electrodes and the source/drain areas; and then
forming an interlayer dielectric film on the semiconductor substrate including the gates, the gate electrode, the silicide layers and the second spacers; and then
forming a contact plug extending through the interlayer dielectric film and electrically connected to the gates, the gate electrode and the source/drain areas.

17. The method of claim 16, wherein forming the silicide layer comprises:
forming a first metal layer on the semiconductor substrate including the gates, the gate
electrode and the second spacers; and then
performing an annealing process on the semiconductor substrate.

18. The method of claim 17, wherein forming the contact plugs comprises:
forming via holes in the interlayer dielectric film exposing the silicide layers; and then
forming a second metal layer in the via holes.

19. The method of claim 18, wherein the first metal layer comprises cobalt and the
second metal layer comprises tungsten.

20. A method comprising:
forming gates spaced apart on a semiconductor substrate; and then
forming first spacers comprising a first oxide layer and a first nitride layer on sidewalls of
the gates; and then
forming source/drain areas in the semiconductor substrate; and then
removing the first nitride layer to expose the first oxide layer; and then
forming second spacers comprising the first oxide layer and a second nitride layer on the
sidewalls of the gate; and then
forming silicide layers on the gates and the source/drain areas; and then
forming an interlayer dielectric film on the semiconductor substrate including the gates,
the silicide layers and the second spacers; and then
forming a contact plug extending through the interlayer dielectric film and electrically
connected to the gates, the gate electrode and the source/drain areas.
ABSTRACT

A method of manufacturing a flash memory device that prevents generation of voids when forming an interlayer dielectric film. The method may include forming a gate on a semiconductor substrate, and then sequentially stacking a first dielectric film and a second dielectric film on the semiconductor substrate, and then forming a first spacer comprising a first dielectric film pattern and a second dielectric film pattern on sidewalls of the gate by performing a first etching process, and then forming source and drain areas in the semiconductor substrate, and then removing the second dielectric film, and then sequentially stacking a third dielectric film and a fourth dielectric film on the semiconductor substrate, and then forming a second spacer comprising the first dielectric pattern and a third dielectric pattern on the sidewalls of the gate by performing a second etching process, and then forming an interlayer dielectric film on the semiconductor substrate including the gate and the first spacer.
**Title of Invention:**  
METHOD OF MANUFACTURING FLASH MEMORY DEVICE

**First Named Inventor/Applicant Name:**  
Hyun-Ju Lim

**Filer:**  
Todd Anthony Vaughn

**Attorney Docket Number:**  
604-0170

**Filed as Large Entity**

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**Miscellaneous-Filing:**

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- **Payment was successfully received in RAM:** $1030
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.
**PATENT APPLICATION FEE DETERMINATION RECORD**  
Substitute for Form PTO-875

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*** If the “Highest Number Previously Paid For” IN THIS SPACE is less than 3, enter “3”.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

*If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.*