ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 329 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Jin-Ha Park, Gyeonggi-do, KOREA, REPUBLIC OF;
Jae-Hee Kim, Gyeonggi-do, KOREA, REPUBLIC OF;
PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

or Fax
(571) 273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders, and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address, and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60803 7590 08/19/2010

SHERR & VAUGHN, PLLC
620 HERNDON PARKWAY
SUITE 320
HERNDON, VA 20170

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or be facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Date)

APPLICATION NO. 11932,273
FILING DATE 10/31/2007
FIRST NAMED INVENTOR Jin-Ha Park
ATTORNEY DOCKET NO. 604-0117
CONFIRMATION NO. 2246

TITLE OF INVENTION: FLASH MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME

APPLN. TYPE SMALL ENTITY ISSUE FEE DUE PUBLICATION FEE DUE PREV. PAID ISSUE FEE TOTAL FEES DUE DATE DUE

nonprovisional NO $1510 $300 $0 $1810 11/19/2010

EXAMINER LEE, CALVIN
ART UNIT 2892
CLASS-SUBCLASS 257-314000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.563).

   □ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
   □ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

   (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
   (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

   1 Sherr & Vaughn, PLLC

   2

   3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

   (A) NAME OF ASSIGNEE
   Dongbu HiTek Co., Ltd.

   (B) RESIDENCE: (CITY and STATE OR COUNTRY)
   Seoul, Republic of Korea

   Please check the appropriate assignee category or categories (will not be printed on the patent):
   □ Individual  □ Corporation or other private group entity  □ Government

4a. The following fee(s) are submitted:

   □ Issue Fee
   □ Publication Fee (No small entity discount permitted)
   □ Advance Order - # of Copies

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

   □ A check is enclosed.
   □ Payment by credit card. Form PTO-2038 is attached.
   □ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any
   overpayment, to Deposit Account Number ____________ (enclose a copy of this form).

5. Change in Entity Status (from status indicated above)

   □ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
   □ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the record in the United States Patent and Trademark Office.

Authorized Signature

Date 17 November 2010

Typed or printed name  Todd A. Vaughn

Registration No. 52,319

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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### Utility under 35 USC 111(a) Filing Fees

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<tr>
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<td>Daniel Hilary Sherr</td>
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.
NOTICE OF ALLOWANCE AND FEE(S) DUE

66803  7590  08/19/2010
SHERR & VAUGHN, PLLC
620 HERNDON PARKWAY
SUITE 320
HERNDON, VA 20170

EXAMINER
LEE, CALVIN

ART UNIT 2892
PAPER NUMBER

APPLICATION NO.  FILING DATE  FIRST NAMED INVENTOR ATTORNEY DOCKET NO. CONFIRMATION NO.

TITLE OF INVENTION: FLASH MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME

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THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:
A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.
B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:
A. Pay TOTAL FEE(S) DUE shown above, or
B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.
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Complete and send this form, together with applicable fee(s), to:

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Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

or Fax
(571) -273-2885

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(Date)

APPLICATION NO.   FILING DATE   FIRST NAMED INVENTOR   ATTORNEY DOCKET NO.   CONFIRMATION NO.

11/932,273   10/31/2007   Jin-Ha Park   604-0117   2246

TITLE OF INVENTION: FLASH MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME

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EXAMINER   ART UNIT   CLASS-SUBCLASS

LEE, CALVIN   2892   257-314000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (Change of Correspondence Address Form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47, Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

☐ the names of up to 3 registered patent attorneys or agents OR, alternatively,

☐ the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent):

☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☐ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

☐ A check is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number (enclose an extra copy of this form).

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☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

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Authorized Signature

Date

Typed or printed name

Registration No.

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Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 271 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 271 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.
-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to Amendment dated May 17, 2010.

2. ☒ The allowed claim(s) is/are 1-3 and 5-10.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All
   b) ☐ Some*
   c) ☐ None
   of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____.
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER’S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as “replacement sheets”) must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson’s Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner’s Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner’s comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

---

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
3. ☐ Information Disclosure Statements (PTO/SD/08), Paper No./Mail Date _____
4. ☐ Examiner’s Comment Regarding Requirement for Deposit of Biological Material
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☒ Examiner’s Amendment/Comment
8. ☒ Examiner’s Statement of Reasons for Allowance
9. ☐ Other _____.

/Calvin Lee/
Primary Examiner, Art Unit 2892

---

U.S. Patent and Trademark Office
PTOL-37 (Rev. 08-06)
OFFICE ACTION

Examiner’s Amendment

1. An examiner’s amendment to the record appears below. Should the changes or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. Labeled “PRIOR ART” to the figures/drawings 1-3. Corrected DRAWINGS in compliance with 37 CFR 1.121(d) are required in reply to this Office action to avoid abandonment of the application.

Allowable Subject Matter

2. Claims 1-3 and 5-10 are allowed. Following is the Examiner’s reason for allowance:

The closest prior art, US 2006/0163678 to Anezaki et al, discloses a flash memory device process, except for the teaching of “forming a source/drain region by performing an ion implantation process using the spacer pattern and the gate region as a mask; removing the second oxide film disposed at an outermost position of the spacer pattern after forming the source/drain region,” of the pending claims in a manner which would warrant a rejection under 35 USC § 102 and/or 35 USC § 103. There was no other prior art that suggested modification or combination with the cited prior art so as to satisfy the combination of the independent claim 1.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Contact Information

4. Any inquiry concerning this communication from the Examiner should be directed to Calvin Lee at (571) 272-1896 on Mondays thru Thursdays 7AM-5PM (E.S.T.). If attempts to reach the examiner by telephone are unsuccessful, the Examiner’s Supervisor Thao Xuan Le can be reached at (571) 272-1708 on Mon-Fri. The official fax phone number for the organization is (571) 273-8300.

Information regarding the status of an application may be obtained from either Public Patent Application Information Retrieval system (PAIR) at http://pair-direct.uspto.gov or Private (PAG). Should you have questions on access to the PAG system, contact EBC at (866) 217-9197.

/Calvin Lee/

Dated: August 12, 2010

Primary Examiner, Art Unit 2892
## Index of Claims

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- Rejected
- Cancelled
- Restricted
- Allowed
- Non-Elected
- Interference
- Appeal
- Objected

☐ Claims renumbered in the same order as presented by applicant
☐ CPA  ☐ T.D.  ☐ R.1.47

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**Total Claims Allowed:**

9

(Primary Examiner) Calvin Lee
Primary Examiner. Art Unit 2892

O.G. Print Claim(s) 1
O.G. Print Figure 4-5

Aug 12 *10

(Date)
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Jin-Ha Park
Docket No.: 604-0117
Confirmation No.: 2246
Application No.: 11/932,273
Group Art Unit: 2813
Filed: August 31, 2007
Examiner: CHAN, CANDICE

For: FLASH MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME

Commissioner for Patents
P.O. BOX 1450
Alexandria, VA 22313-1450

REPLY AND AMENDMENT UNDER 37 C.F.R. § 1.111

Sir:

In response to the Non-final Office Action mailed February 16, 2010, Applicant respectfully requests reconsideration of the application in view of the following Amendments and Remarks.

Applicant believes that no extensions of time are required at this time. However, if extensions of time are necessary to prevent abandonment of this application, such extensions of time are hereby petitioned for under 37 C.F.R. §1.136(a).

Amendments to the Claims are reflected in the listing of claims which begins on page 2.

Remarks begin on page 5.
AMENDMENTS TO THE CLAIMS

Please **CANCEL** claims 4 and 11-20 without prejudice or disclaimer.

Please **AMEND** claims 1, 2, and 5 as shown below.

The following is a complete list of all claims in this application.

1. (Currently Amended) A method comprising:

   forming a gate region including a tunnel oxide film, a floating gate, a dielectric film and a control gate over a semiconductor substrate;

   forming a spacer film having a multi-layer insulating film structure a first oxide film, a nitride film, and a second oxide film against a sidewall of the gate region;

   forming a spacer pattern by performing an entire surface etching on the spacer film;

   forming a source/drain region by performing an ion implantation process using the spacer pattern and the gate region as a mask;

   removing an insulating film the second oxide film disposed at an outermost position of the spacer pattern after forming the source/drain region; and then

   forming an interlayer insulating film over the semiconductor substrate with the gate region and a spacer formed thereon.

2. (Currently Amended) The method of claim 1, wherein the insulating film the second oxide film disposed at the outermost position of the multi-layer insulating film the spacer pattern is removed using a wet etching method.
3. (Original) The method of claim 2, wherein a BHF solution is used as an etching solution in the wet etching method.

4. (Canceled)

5. (Currently Amended) The method of claim [4] 1, wherein the first oxide film comprises TEOS.

6. (Original) The method of claim 5, wherein the second oxide film comprises TEOS.

7. (Original) The method of claim 6, wherein the nitride film comprises SiN.

8. (Original) The method of claim 7, wherein the first oxide film has a thickness between approximately 150 to 300Å.

9. (Original) The method of claim 8, wherein the nitride film has a thickness between approximately 100 to 300Å.

10. (Original) The method of claim 9, wherein the second oxide film has a thickness between approximately 500 to 800Å.

11-20. (Canceled)
REMARKS

Claims 1-3 and 5-10 are currently pending in the above-referenced patent application. Claims 4 and 11-20 are canceled and claims 1, 2, and 5 are amended by way of the present amendment. No new matter is added as the amendments have support in the original disclosure.

In the Non-Final Office Action: Claims 1, 4-7, and 11 were rejected under 35 U.S.C. 102(b) as being anticipated by Anezaki (U.S. Patent Publication No. 2006/0163678. Claims 8-10 were rejected under 35 U.S.C. 103(a) as being unpatentable over Anezaki. Claims 2-3 was rejected under 35 U.S.C. 103(a) as being unpatentable over Anezaki in view of Murase (U.S. Patent No. 5,436,489).

In reply to the rejection of claims 1, 4-7, and 11 under 35 U.S.C. 102(b) as being anticipated by Anezaki, Applicant respectfully requests reconsideration.

Claim 1 is amended to incorporate features of claims 4 and 11 and claims 4 and 11 are canceled.

Claim 1 now recites “…forming a spacer film having a first oxide film, a nitride film, and a second oxide film against a sidewall of the gate region;…forming a source/drain region by performing an ion implantation process using the spacer pattern and the gate region as a mask; removing the second oxide film disposed at an outermost position of the spacer pattern after forming the source/drain region…”

Anezaki relates to a semiconductor device and method for manufacturing semiconductor device, as specified in the title.
The Office Action asserts on page 2, lines 18-21 that Anezaki discloses the feature of claim 1 of “…removing an insulating film disposed at an outermost position of the spacer pattern…”

However, Anezaki fails to disclose the feature of amended claim 1 of “…removing the second oxide film disposed at an outermost position the spacer pattern after forming the source/drain region…”

Unlike the claimed second oxide film removed from the spacer pattern, a removed portion of a side wall spacer of Anezaki is not an oxide film. The removed portion of the side wall spacer is a silicon nitride film 37 as described in paragraph [0097] of Anezaki.

Further, the Office Action asserts on page 3, line 5 that a side wall spacer 44c of silicon oxide of Anezaki is equivalent to the claimed second oxide film.

However, the side wall spacers 44c of Anezaki is patentably distinguishable from the claimed second oxide film because the side wall spacer 44c of Anezaki is not removed after forming source/drain regions 31 and 33 as shown in Figs. 6R to 6U of Anezaki.

At least for this reason, as Anezaki does not disclose all of the features of claim 1, the rejection of claims 1, 4-7, and 11 under 35 U.S.C. 102(b) cannot be established.

Accordingly, Applicant respectfully requests withdrawal of the rejection of claims 1, 4-7, and 11.

In reply to the rejection of claims 8-10 under 35 U.S.C. 103(a) as being unpatentable over Anezaki, Applicant respectfully requests reconsideration.

Claims 8-10 include the features discussed above for claims 1, 4-7, and 11.
As discussed above, Anezaki does not teach or suggest the features of “...removing the second oxide film disposed at an outermost position the spacer pattern after forming the source/drain region...”

At least for this reason, Anezaki does not teach or suggest, alone or in combination, the features of claims 8-10 and therefore a prima facie case of obviousness under 35 U.S.C. 103(a) cannot be established in this rejection.

Accordingly, Applicant respectfully requests withdrawal of the rejection to claims 8-10.

In reply to the rejection of claims 2-3 under 35 U.S.C. 103(a) as being unpatentable over Anezaki in view of Murase (U.S. Patent No. 5,436,489), Applicant respectfully requests reconsideration.

Claims 2-3 include the features discussed above for claims 1, 4-7, and 11.

As discussed above, Anezaki does not teach or suggest the features of “...removing the second oxide film disposed at an outermost position the spacer pattern after forming the source/drain region...”

Murase relates to a field effect transistor, as specified in the title. However, Murase does not teach or suggest “...removing the second oxide film disposed at an outermost position the spacer pattern after forming the source/drain region...” Therefore, Murase does not alleviate the deficiencies of Anezaki of not teaching or suggesting the features discussed above.

At least for these reasons, neither Anezaki nor Murase teach or suggest, alone or in combination, the features of claims 2-3 and therefore a prima facie case of obviousness under 35 U.S.C. 103(a) cannot be established in this rejection.
Accordingly, Applicant respectfully requests withdrawal of the rejection to claims 2-3.
CONCLUSION

Applicant believes that a full and complete response has been made to the Office Action and respectfully submits that all of the stated objections and grounds for rejection have been overcome or rendered moot. Accordingly, Applicant respectfully submits that all pending claims are allowable and that the application is in condition for allowance.

Should the Examiner feel that there are any issues outstanding after consideration of this response, the Examiner is invited to contact the Applicant's undersigned representative at the number below to expedite prosecution.

Prompt and favorable consideration of this Reply is respectfully requested.

Respectfully Submitted,

Todd A. Vaughn
Reg. No. 52,319

Sherr & Vaughn, PLLC
620 Herndon Parkway
Suite 320
Herndon, Virginia 20170
Tel: 571-313-7559
Fax: 703-935-8473

TAV/JKP
Electronic Acknowledgement Receipt

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Title of Invention: FLASH MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME

First Named Inventor/Applicant Name: Jin-Ha Park

Customer Number: 60803

Filer: Daniel Hilary Sherr

Filer Authorized By: 

Attorney Docket Number: 604-0117

Receipt Date: 17-MAY-2010

Filing Date: 31-OCT-2007

Time Stamp: 15:38:39

Application Type: Utility under 35 USC 111(a)

Payment information:

Submitted with Payment: no

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Warnings:

Information:
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.
# Patent Application Fee Determination Record

**FOR**
- Basic Fee (37 CFR 1.16(a), (b), or (c))
- Search Fee (37 CFR 1.16(k), (l), or (m))
- Examination Fee (37 CFR 1.16(b), (g), or (h))
- Total Claims (37 CFR 1.16(i))
- Independent Claims (37 CFR 1.16(h))
- Application Size Fee (37 CFR 1.16(s))

**SMALL ENTITY**
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- Number Extra
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- Fee ($) OR Small Entity

**OTHER THAN SMALL ENTITY**
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**TOTAL**
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## Application as Amended – Part I

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**TOTAL ADD'L FEE**
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**LEGAL INSTRUMENT EXAMINER:**

LINDA A. WASHINGTON

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.
Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.
Office Action Summary

Application No. 11/932,273
Applicant(s) PARK ET AL.
Examiner Candice Y. Chan
Art Unit 2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)x Responsive to communication(s) filed on 23 July 2009.
2a)☐ This action is FINAL. 2b)x This action is non-final.
3)x Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)x Claim(s) 1-20 is/are pending in the application.
   4a) Of the above claim(s) 12-20 is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)x Claim(s) 1-11 is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)x Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)x Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a)☐ All  b)☐ Some * c)☐ None of:
      1.☐ Certified copies of the priority documents have been received.
      2.☐ Certified copies of the priority documents have been received in Application No. _____.
      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsman’s Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO/SB/08)
   Paper No(s)/Mail Date 6/15/09.
4)☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date _____.
5)☐ Notice of Informal Patent Application
6)☐ Other: _____.
DETAILED ACTION

Election/Restrictions

Applicant’s election without traverse of Group I, claims 1-11, in the reply filed on 23 July 2009 is acknowledged.

Claims 12-20 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made without traverse in the reply filed on 23 July 2009.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4-7 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Anezaki (US 2006/0163678).

Regarding claim 1, Anezaki (Figs. 6A-6U) teaches a method comprising: forming a gate region including a tunnel oxide film 25 (¶ 0083), a floating gate 26 (¶ 0093), a dielectric film 27 (¶ 0093) and a control gate 28 (¶ 0093) over a semiconductor substrate 11; forming a spacer film having a multi-layer insulating film structure against a sidewall of the gate region (see Fig. 6N); forming a spacer pattern by performing an entire surface etching on the spacer film (¶ 0097); removing an insulating film disposed at an outermost position of the spacer pattern (see Figs.
6M-6N; 37 is removed); and then forming an interlayer insulating film 21 over the semiconductor substrate with the gate region and a spacer formed thereon (see Fig. 6U).

Regarding claim 4, Anezaki (Figs. 6A-6U) teaches the method of claim 1, wherein forming the spacer film comprises sequentially depositing a first oxide film 36 (¶ 0097), a nitride film 37 (¶ 0097) and a second oxide film 44 (¶ 0103).

Regarding claim 5, Anezaki (Figs. 6A-6U) teaches the method of claim 4, wherein the first oxide film 36 comprises TEOS (¶ 0097).

Regarding claim 6, Anezaki (Figs. 6A-6U) teaches the method of claim 5, wherein the second oxide film 44 comprises TEOS (¶ 0103).

Regarding claim 7, Anezaki (Figs. 6A-6U) teaches the method of claim 6, wherein the nitride film 37 comprises SiN (¶ 0097).

Regarding claim 11, Anezaki (Figs. 6A-6U) teaches the method of claim 1, further comprising forming a source/drain region 32/33 through an ion implantation process using the spacer pattern and the gate region as a mask before removing the insulating film disposed at an outermost position of the spacer pattern (¶¶ 0095-96; see Figs. 6K-6L).
Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anezaki (US 2006/0163678).

Regarding claims 8-10, Anezaki teaches the method of claim 7, however fails to expressly disclose wherein the first oxide film has a thickness between approximately 150 to 300Å, the nitride film has a thickness between approximately 100 to 300Å, and the second oxide film has a thickness between approximately 500 to 800Å. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the claimed film thicknesses, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anezaki (US 2006/0163678) as applied to claim1 above, and further in view of Murase (US 5,436,489).

Regarding claim 2, Anezaki teaches the method of claim 1, wherein the insulating film 37 (SiN, ¶ 0097) disposed at the outermost position of the multi-layer insulating film is removed (Figs. 6M-6N) however fails to expressly disclose using a wet etching method. Murase teaches a
method of making a semiconductor device including utilizing a BHF wet etch solution to etch a silicon nitride film (¶ 0061). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Anezaki to utilize a wet etching step since a BHF wet etch step is an art recognized method suitable for etching silicon nitride (as in Murase ¶ 0061).

Regarding claim 3, Anezaki and Yamada teach the method of claim 2, Yamada teaches further wherein a BHF solution is used as an etching solution in the wet etching method (¶ 0061).

**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Candice Y. Chan whose telephone number is (571) 272-9013. The examiner can normally be reached on M-F, 8-4:30PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Matthew Landau can be reached on (571) 272-1731. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Matthew C. Landau/
Supervisory Patent Examiner, Art Unit 2813
cyc
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(e).)
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U.S. Patent and Trademark Office
PTO-892 (Rev. 01-2001)
### Search Notes

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**APPLICANTS**
- Jin-Ha Park, Gyeonggi-do, KOREA, REPUBLIC OF;
- Jae-Hee Kim, Gyeonggi-do, KOREA, REPUBLIC OF;

**CONTINUING DATA ********************

**FOREIGN APPLICATIONS ********************

**IF REQUIRED, FOREIGN FILING LICENSE GRANTED **
- 11/20/2007

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**ADDRESS**
- SHERR & VAUGHN, PLLC
- 620 HERNDON PARKWAY
- SUITE 320
- HERNDON, VA 20170
- UNITED STATES

**TITLE**
- FLASH MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME

**FILING FEE RECEIVED**
- 1030

FEES: Authority has been given in Paper No._________ to charge/credit DEPOSIT ACCOUNT No._________ for following:

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Examiner Signature: /Candice Chan/

Date Considered: 02/01/2010

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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. * Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450. If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Jin-Ha Park et al.  
Docket No.: 604-0117  
Confirmation No.: 2246  
Application No.: 11/932,273  
Group Art Unit: 2813  
Filed: October 31, 2007  
Examiner:  

For: FLASH MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME  
Commissioner for Patents  
P.O. BOX 1450  
Alexandria, VA 22313-1450

REPLY TO RESTRICTION REQUIREMENT

Sir:

In response to the Restriction Requirement mailed July 6, 2009, Applicant elects Group I (claims 1-11), without traverse.

It is not believed that any extensions of time or fees are required. If extensions of time are necessary to prevent abandonment of this application, such extensions of time are hereby petitioned for under 37 C.F.R. §1.136(a).

Respectfully Submitted

Todd A. Vaughn  
Reg. No. 52,319

Sherr & Vaughn, PLLC  
620 Herndon Parkway  
Suite 320  
Herndon, Virginia 20170  
Tel: 571-313-7556  
Fax: 703-935-8473

TAV/SWL/jjl
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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.
Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.
**Office Action Summary**

<table>
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<th>Application No.</th>
<th>Applicant(s)</th>
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<td>11/932,273</td>
<td>PARK ET AL.</td>
</tr>
<tr>
<td>Examiner</td>
<td>Art Unit</td>
</tr>
<tr>
<td>Candice Y. Chan</td>
<td>2813</td>
</tr>
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**The MAILING DATE of this communication appears on the cover sheet with the correspondence address**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1. [X] Responsive to communication(s) filed on 15 June 2009.
2a. [ ] This action is FINAL.
2b. [X] This action is non-final.
3. [ ] Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4. [X] Claim(s) 1-20 is/are pending in the application.
   4a. Of the above claim(s) ______ is/are withdrawn from consideration.
5. [ ] Claim(s) ______ is/are allowed.
6. [ ] Claim(s) ______ is/are rejected.
7. [ ] Claim(s) ______ is/are objected to.
8. [X] Claim(s) 1-20 are subject to restriction and/or election requirement.

**Application Papers**

9. [ ] The specification is objected to by the Examiner.
10. [ ] The drawing(s) filed on ______ is/are: a. [ ] accepted or b. [ ] objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11. [ ] The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12. [ ] Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a. [ ] All
   b. [ ] Some * c. [ ] None of:
      1. [ ] Certified copies of the priority documents have been received.
      2. [ ] Certified copies of the priority documents have been received in Application No. ______.
      3. [ ] Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1. [ ] Notice of References Cited (PTO-892)
2. [ ] Notice of Draftsperson’s Patent Drawing Review (PTO-948)
3. [ ] Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date ______.
4. [ ] Interview Summary (PTO-413) Paper No(s)/Mail Date ______.
5. [ ] Notice of Informal Patent Application
6. [ ] Other: ______.
DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-11, drawn to a method of making a semiconductor device, classified in class 438, subclass 261.

II. Claims 12-20, drawn to a semiconductor device, classified in class 257, subclass 321.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claimed can be made by another and materially different process, for example a process in which the spacer pattern is formed by selectivity depositing the spacer film.

Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and examination burden if restriction were not required because one or more of the following reasons apply:

(a) the inventions have acquired a separate status in the art in view of their different classification;
(b) the inventions have acquired a separate status in the art due to their recognized divergent subject matter;
(c) the inventions require a different field of search (for example, searching different classes/subclasses or electronic resources, or employing different search queries);
(d) the prior art applicable to one invention would not likely be applicable to another invention;
(e) the inventions are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

Applicant is advised that the reply to this requirement to be complete must include
(i) an election of a invention to be examined even though the requirement may be traversed (37 CFR 1.143) and (ii) identification of the claims encompassing the elected invention.

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected invention.

If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the
inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

The examiner has required restriction between product and process claims. Where applicant elects claims directed to the product, and the product claims are subsequently found allowable, withdrawn process claims that depend from or otherwise require all the limitations of the allowable product claim will be considered for rejoinder. All claims directed to a nonelected process invention must require all the limitations of an allowable product claim for that process invention to be rejoined.

In the event of rejoinder, the requirement for restriction between the product claims and the rejoined process claims will be withdrawn, and the rejoined process claims will be fully examined for patentability in accordance with 37 CFR 1.104. Thus, to be allowable, the rejoined claims must meet all criteria for patentability including the requirements of 35 U.S.C. 101, 102, 103 and 112. Until all claims to the elected product are found allowable, an otherwise proper restriction requirement between product claims and process claims may be maintained. Withdrawn process claims that are not commensurate in scope with an allowable product claim will not be rejoined. See MPEP § 821.04(b). Additionally, in order to retain the right to rejoinder
in accordance with the above policy, applicant is advised that the process claims should be amended during prosecution to require the limitations of the product claims. **Failure to do so may result in a loss of the right to rejoinder.** Further, note that the prohibition against double patenting rejections of 35 U.S.C. 121 does not apply where the restriction requirement is withdrawn by the examiner before the patent issues. See MPEP § 804.01.

**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Candice Y. Chan whose telephone number is (571)272-9013.

The examiner can normally be reached on M-F, 8-4:30PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Matthew Landau can be reached on (571) 272-1731. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Matthew C. Landau/
Supervisory Patent Examiner, Art Unit 2813

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<th>Foreign Patent Document</th>
<th>Publication Date</th>
<th>Name of Patentee or Applicant of Cited Document</th>
<th>Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear</th>
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. Applicant’s unique citation designation number (optional). * See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. * Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). * For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. * Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form as well as suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.
Abstract

Yu Mengwei 31219
Ye Shuangqiang, Jin Pingzhang

Address
Shanghai Hongqi Semiconductor Mfg. Co., Ltd.
H01L21/22; H01L21/28

Priority Information
Publication Date 2003.03.09
Application Date 2003.08.27
Publication Number 199823
Application Number 0315068

Title: Method of increasing IC assembling density
发明名称：增加集成电路构装密度的制造方法

摘要

本发明提供一种增加集成电路构装密度的制造方法，其在半导体底材上提供一栅极结构；在紧邻于栅极结构的侧面形成一氧化物层，并于氧化物层上共形沉积一间隙层材料于间隙层材料上再形成一氧化物，此氧化物具有一形状以覆盖间隙层材料的一 L 形部分；接着移除氧化物以暴露出间隙层材料的 L 形部分。此种具有 L 形间隙层的栅极结构有利于空隙填充与避免接触至栅极的短路。
权利要求书

1、一种增加集成电路构装密度的制造方法，其特征在于，包括下列步骤：

在半导体底材上形成一栅极结构；

在紧邻该栅极结构的侧面形成一氧化层；

在该氧化层上共形沉积一间隙壁材料；

在该间隙壁材料上形成一氧化物，该氧化物具有一形状以覆盖该间隙壁材料的一 L 形部分；及

移除该氧化物以暴露出该间隙壁材料的该 L 形部分。

2、根据权利要求 1 所述的增加集成电路构装密度的制造方法，其特征在于，还包含在该氧化物与该半导体底材上沉积一中间介电层。

3、根据权利要求 1 所述的增加集成电路构装密度的制造方法，其特征在于，还包含在未被该氧化膜层覆盖的该栅极结构上形成一自开发硅化物膜层。

4、根据权利要求 1 所述的增加集成电路构装密度的制造方法，其特征在于，其中该间隙壁材料为氮化物材料，较佳的为氮化硅。

5、一种增加集成电路构装密度的制造方法，其特征在于，包括下列步骤：

提供至少两栅极结构于半导体底材上；

在该半导体底材与该复数个栅极结构上形成一第一氧化层；

在该第一氧化层上共形沉积一氮化物层，其中相对于该第一氧化层时，该氮化物层具有较厚的一第一厚度；

在该氮化物层上形成一第二氧化层，其中相对于该氮化物层时，该第二氧化层具有较厚的一第二厚度；及

移除部分该第一氧化层、该氮化物层与该第二氧化层以暴露出该半导体底材与该等栅极结
构的顶部，且该氮化物层的复数个 L 形部分紧邻于该复数个栅极结构的侧面。

6. 根据权利要求 5 所述的增加集成电路构装密度的制造方法，其特征在于，还包含移除该第二氧化层以暴露出该氮化物层的该复数个 L 形部分。

7. 根据权利要求 6 所述的增加集成电路构装密度的制造方法，其特征在于，还包含在该复数个栅极结构与该半导体底材上形成一中间介电层，以及移除介于该复数个栅极结构之间的部分该中间介电层，以形成一接触。

8. 根据权利要求 6 所述的增加集成电路构装密度的制造方法，其特征在于，还包含于在该栅极结构的顶部上形成一自行对准硅化物薄膜层。

9. 根据权利要求 6 所述的增加集成电路构装密度的制造方法，其特征在于，还包含以该 L 形部分与该栅极结构部分做为一屏蔽，在该半导体底材中植入离子。

10. 根据权利要求 5 所述的增加集成电路构装密度的制造方法，其特征在于，其中该第一厚度实质上为 300 埃。

11. 根据权利要求 5 所述的增加集成电路构装密度的制造方法，其特征在于，其中该第二厚度实质上为 1000 埃。

12. 根据权利要求 5 所述的增加集成电路构装密度的制造方法，其特征在于，其中该提供步骤包含以该栅极结构为一掩蔽，以在该半导体底材中进行离子植入步骤。
增加集成电路构装密度的制造方法

技术领域

本发明涉及一种用于改善集成电路中的构装密度（packing density）的制造方法，尤其涉及一种有利于间隙充填（gap-filling）与避免接触至栅极间的短路（contact-to-gate shorts）的制造方法。

背景技术

间隙壁（spacer）为一种紧邻栅极侧面，并且在源极与漏极延伸区上方的结构。较佳的间隙壁为二氧化硅结构，可以选择的其它的材料，例如氮化硅（silicon nitride）、氮氧化硅（silicon oxynitride, SiON）等等也可以做为间隙壁材料。以截面观察传统的间隙壁，通常为圆滑形状，金氧半导体场效晶体管则利用 D 形间隙壁、三角形氧化物间隙壁、或是楔形氧化物间隙壁，这些形状的间隙壁，有助于分开浅源极与漏极延伸区（shallow source and drain extensions）和深源极与漏极接触接合（deep source and drain contact junctions）。

集成电路（IC）长程目标在于尺寸的缩小与构装密度的提升，尺寸缩小的 IC 减少所占用的面积，对于 IC 高速效能表现是很重要的，且提升的构装密度则可在单位面积上安置更多的半导体元件；此外，IC 晶粒面积的减少也可导致 IC 制造的较高产能，这些优点驱使 IC 尺寸的缩小与构装密度的提升。然而，当欲提升构装密度时，中间介电层（interlayer dielectric）的间隙充填及避免接触至栅极的短路形成一大挑战。传统不同形状的间隙壁，对于尺寸的缩小、构装密度的提升、与元件的制造而言，很难有所帮助。
发明内容

本发明所要解决的技术问题在于提供一种增加集成电路构成密度的制造方法，其利用深次微米技术形成L形间隙壁，以有效提高集成电路的构成密度。

本发明所要解决的另一技术问题是提供一种以深次微米技术制作的制造方法，其有利于空隙充填与避免接触至金属的短路，且L形间隙壁有利于空隙的充填，并避免与接触之间的短路现象发生。

为了解决上述技术问题，本发明提供一种制造方法，有助于集成电路中的构成密度，包括：提供一栅极结构于一半导体底材上，并形成一氧化膜层紧邻于栅极结构的侧面上；共形沉积一间隙壁材料于氧化膜层上，再于间隙壁材料上形成一氧化物，此氧化物具有一可覆盖间隙壁材料的L形结构，接着移除该氧化物以露出间隙壁材料的L形部分。

后面通过具体实施例结合所附的图式详细说明，以更容易了解本发明的目的、技术内容、特点及其所达成的功效。

附图说明

图1-图3是根据本发明的IC部分的剖面示意图。
图4是根据图3后沉积一中间介电层的剖视图。
图5-6是根据本发明的另一IC部分的剖面示意图。

图号说明：
10 基材
12 氧化膜层
14 氧化物材料层（L形间隙壁）
16 栅极结构
18 氧化层
20 中间介电层
具体实施方式

本发明的半导体设计可被广泛地应用到许多半导体设计中，并且可利用许多不同的半导体材料制作，当本发明以一较佳实施例来说明本发明方法时，本领域内的普通技术人员应知许多的步骤是可以改变的，材料及杂质也是可替换的，这些一般的替换无疑地不脱离本发明的精神及范畴。

其次，本发明用示意图详细描述如下，在详述本发明实施例时，表示半导体结构的剖面图在半位体制程中会不依一般比例作局部放大以利说明，应不能以此作为对本发明的限定，此外，在实际的制作中，应包含长度、宽度及深度的三维空间尺寸。

图 1 至图 3 为根据本发明的 IC 部分的剖面示意图。如图 1 所示，此部分包含一底材 10、一栅极结构 16、一氧化层 12、一氮化物材料层 14 以及一氧化层 18。此一部份可做为半导体晶片，例如硅晶片上 IC 的一部份。底材 10 可以是任何适当的半导体材料，在一实施例中，底材 10 为硅材料，亦可包含若干井于其中；栅极结构 16 可以是任何适当的导体材料，且在此实施例中，栅极结构 16 是多晶硅材料，而氮化物材料层 14 则为一氧化硅材料或是其它间隙壁材料；氧化层 12 以适当的方法形成，并紧邻于栅极结构 16 的侧壁（lateral sides），其厚度约为 100 埃；氮化物材料层 14 是作为一间隙壁，共形（conformally）沉积于氧化层 12 上，其厚度约为 300 埃；以及该氧化层 18 是以适当的方法形成，其具有一厚度大于氮化物材料层 14 的厚度，例如 1000 埃。

如图 2 所示，部分的氧化层 18、氮化物材料层 14，及氧化层 12 以蚀刻方式移除。之后暴露出底材 10 与栅极结构 16 的顶部，剩余的氧化层 18 覆盖氮化物材料层 14 及氧化层 12 的 L 形部分；此氧化物材料层 14 及氧化层 12 的 L 形部分紧邻于栅极结构 16 的侧壁。

接着，如图 3 所示，剩余的氧化层 18 以适当的蚀刻方法移除，氮化物材料层 14 的 L 形部分未被覆盖，其即可视为栅极结构 16 的 L 形间隙壁 14 的一部分。根据本发明，栅极结构
16 的 L 形间隙壁 14 的设计有助于构装密度，因为其使得空隙充填变得很容易，并且避免栅极与接触的短路。如图 2 所示，当进行中间介质层 20 的沉积时，因为 L 形间隙壁 14 不会妨碍中间介质层 20 的充填，因此介于栅极结构 16 之间的微小空隙可以如半导体的其它部分一样地顺利充填。因此，L 形间隙壁 14 有助于中间介质层 20 的充填，进而增加 IC 的构装密度。

要了解的是，有许多植入步骤介于上述步骤中，举例来说，例如在氧化薄层 12 形成之前，以栅极结构 16 做为植入掩蔽，对底材 10 进行离子植入步骤，以作为轻掺杂极区域；另在后续步骤进行之前，以栅极结构 16 与 L 形间隙壁 14 作为另一植入掩蔽，对该底材 10 内进行离子植入，以作为源极与漏极区域。

图 5、图 6 为根据本发明的另一 IC 部分的剖面示意图。如图 5 所示，若干设计需在栅极结构 16 的顶部首先形成自准硅化物层 22，之后中间介质层 20 再沉积于底材 10 与栅极结构 16 上。如图 6 所示，移除部分的中间介质层 20，以在栅极结构 16 形成接触。

因此，相较于传统形状间隙壁，当后续完成接触后，本发明的 L 形间隙壁可避免接触至栅极的短路。因此，本发明的优点之一是可避免接触至栅极的短路。

以上所述的实施例仅用于说明本发明的技术思想及特点，其目的在使本领域内的普通技术人员能够了解本发明的内容并据以实施，并不能仅以此来限定本发明的专利范围，即凡依本发明所揭示的精神所作的等效变化或修饰，仍应涵盖在本发明的专利范围内。
# Electronic Acknowledgement Receipt

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**Title of Invention:**
FLASH MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME

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<th>Jin-Ha Park</th>
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<td>Customer Number:</td>
<td>60803</td>
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<tr>
<td>Filer:</td>
<td>Daniel Hilary Sherr</td>
</tr>
<tr>
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<td></td>
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**Payment information:**
Submitted with Payment: no

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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60803
SHERR & NOURSE, PLLC
620 HERNDON PARKWAY
SUITE 200
HERNDON, VA20170

Title: FLASH MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME

Publication Date: 06/05/2008

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO’s publicly available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO’s Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Pre-Grant Publication Division, 703-605-4283
Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections.

Applicant(s)  
Jin-Ha Park, Gyeonggi-do, KOREA, REPUBLIC OF;  
Jae-Hee Kim, Gyeonggi-do, KOREA, REPUBLIC OF;

Power of Attorney: None

Domestic Priority data as claimed by applicant

Foreign Applications  
REPUBLIC OF KOREA 10-2006-0120171 11/30/2006

If Required, Foreign Filing License Granted: 11/20/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is US 11/932,273

Projected Publication Date: 06/05/2008

Non-Publication Request: No

Early Publication Request: No
Title
FLASH MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME

Preliminary Class
438

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process simplifies the filing of patent applications on the same invention in member countries, but does not result in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

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<td>Jin-Ha Park</td>
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CONFIRMATION NO. 2246
FORMALITIES LETTER

Date Mailed: 11/26/2007

NOTICE TO FILE CORRECTED APPLICATION PAPERS

_Filing Date Granted_

An application number and filing date have been accorded to this application. The application is informal since it does not comply with the regulations for the reason(s) indicated below. Applicant is given TWO MONTHS from the date of this Notice within which to correct the informalities indicated below. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

The required item(s) identified below must be timely submitted to avoid abandonment:

- Replacement drawings in compliance with 37 CFR 1.84 and 37 CFR 1.121(d) are required. The drawings submitted are not acceptable because:
  - The drawings submitted to the Office are not electronically reproducible because portions of figures 8 are missing and/or blurry.

Applicant is cautioned that correction of the above items may cause the specification and drawings page count to exceed 100 pages. If the specification and drawings exceed 100 pages, applicant will need to submit the required application size fee.
Replies should be mailed to:

Mail Stop Missing Parts
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/lee/

________________________________________
Office of Initial Patent Examination (571) 272-4000 or 1-800-PTO-9199
ENCLdures (Check all that apply)

- Fee Transmittal Form
  - Fee Attached
- Amendment/Reply
  - After Final
  - Affidavits/declaration(s)
- Extension of Time Request
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- Information Disclosure Statement
- Certified Copy of Priority Document(s)
- Reply to Missing Parts/Incomplete Application
  - Reply to Missing Parts under 37 CFR 1.52 or 1.53
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- Petition to Convert to a Provisional Application
- Power of Attorney, Revocation
- Change of Correspondence Address
- Terminal Disclaimer
- Request for Refund
- CD, Number of CD(s)
- Landscape Table on CD

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name          Sherr & Nourse, PLLC
Signature          
Printed name       Daniel H. Sherr
Date               12/10/2007
Reg. No.           46,425

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature          
Typed or printed name Daniel H. Sherr
Date               12/10/2007

This collection of information is required by 37 CFR 1.1. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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In the United States Patent and Trademark Office

In re Patent Application of: Jin-Ha PARK

Docket No.: 604-0117

Confirmation No.: 2246

Application No.: 11/932,273

Group Art Unit: 2812

Filed: October 31, 2007

Examiner:

For: FLASH MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME

MAIL STOP MISSING PARTS
Commissioner for Patents
P.O. BOX 1450
Alexandria, VA 22313-1450

REPLY TO NOTICE TO FILE CORRECTED APPLICATION PAPERS

Sir:

In response to the Notice to File Corrected Application Papers mailed November 26, 2007, Applicant respectfully requests reconsideration of the application in view of the following Amendments and Remarks.

Amendments to the Drawings begin on page 2.
AMENDMENTS TO THE DRAWINGS

Attached in the Appendix is a Replacement Sheet for Fig. 8 which includes the changes, without markings, identified below. No new matter has been added.

Fig. 8 has been amended to correct blurry figures.
Conclusion

Should the Examiner feel that there are any issues outstanding after consideration of this response, the Examiner is invited to contact the Applicant's undersigned representative at the number below to expedite prosecution.

Respectfully Submitted,

[Signature]

Daniel H. Sherr
Reg. No. 46,425

Sherr & Nourse, PLLC
620 Herndon Parkway
Suite 200
Herndon, Virginia 20170
Tel: 703-673-1141
Fax: 703-935-8473
DHS/tljw

APPENDIX: Replacement Drawing Fig. 8
SCORE Placeholder Sheet for IFW Content

Application Number: **11932273**  
Document Date: **12/12/2007**

The presence of this form in the IFW record indicates that the following document type was received in paper and is scanned and stored in the SCORE database.

- Drawings

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Form Revision Date: December 8, 2006
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Jin-Ha PARK et al.

Docket No.: 604-0117

Confirmation No.: 2246

Group Art Unit: Examiner:

Application No.: 11/932,273

Filed: October 31, 2007

For: FLASH MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME

Commissioner for Patents
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Alexandria, VA 22313-1450

CLAIM FOR PRIORITY UNDER 35 USC §119

Sir:

Priority under 35 U.S.C. § 119 is hereby claimed to the following priority document(s), filed in a foreign country within twelve (12) months prior to the filing of the above-referenced United States utility patent application:

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<tr>
<td>KOREA</td>
<td>10-2006-0120171</td>
<td>November 30, 2006</td>
</tr>
</tbody>
</table>

A certified copy of the above listed application is attached. Prompt acknowledgment of the aforementioned claim is respectfully requested.

Respectfully Submitted,

Daniel H. Sherr
Reg. No. 46,425

Sherr & Nourse, PLLC
620 Herndon Parkway
Suite 200
Herndon, Virginia 20170
Tel: 703-673-1141
Fax: 703-935-8473
This is to certify that the following application annexed hereto is a true copy from the records of the Korean Intellectual Property Office.

Application Number: 10-2006-0120171
Filing Date: NOV 30, 2006
Applicant(s): Dongbu Electronics Co., Ltd.

COMMISSIONER

Note: This certificate was issued by the Korean Intellectual Property Office. Please confirm any forgery or alteration of the contents by an issue number or a barcode of the document below through the KIPOnet Online Issue of the Certificates’ menu of Korean Intellectual Property Office homepage (www.kipo.go.kr). But please notice that the confirmation by the issue number is available only for 90 days.
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【권리구분】 특허
【수신처】 특허청장
【참조번호】 2653
【제출일자】 2006.11.30
【국제특허분류】 H01L
【발명의 국문명칭】 플래시 메모리 소자 및 그의 제조방법
【발명의 영문명칭】 Flash Memory Device and Method of Manufacturing the same

【출원인】
【명칭】 동부일렉트로닉스 주식회사
【출원인코드】 1-1998-002671-9

【대리인】
【성명】 허용록
【대리인코드】 9-1998-000616-9
【포괄위임등록번호】 2005-075256-1

【발명자】
【성명】 박진하
【성명의 영문표기】 PARK, Jin Ha
【주민등록번호】 740224-1XXXXXX
【우편번호】 467-773
【주소】 경기 이천시 부발읍 신하리 진우아파트 101-601
【국적】 KR

【발명자】
【성명】 김재희
【성명의 영문표기】 KIM, Jea Hee
【주민등록번호】 690630-1XXXXXX

23-1
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【국적】 KR
【성명】 청구
【취지】 특허법 제42조의 규정에 의한 출원, 특허법 제60조의 규정에 의한 심사청구를 합니다.

대리인

허용록 (인)

【수수료】
【기본출원료】 0 면 38,000 원
【가산출원료】 19 면 0 원
【우선권주장료】 0 건 0 원
【심사청구료】 12 항 493,000 원
【합계】 531,000 원
【요약서】

【요약】

본 발명은 플래시 메모리 및 그의 제조방법에 관한 것으로서, 반도체 기판상에 터널 산화막, 폴로링 게이트, 유전체막 및 컨트롤 게이트로 구성된 게이트 영역을 형성하는 단계; 상기 게이트 영역의 측벽에 3층 절연막 구조의 스페이서막을 형성하는 단계; 상기 스페이서막을 전면식각하여 스페이서 패턴을 형성하는 단계; 상기 스페이서 패턴의 최외각에 위치한 절연막을 제거하는 단계; 상기 게이트 영역 및 스페이서가 형성된 반도체 기판상에 중간 절연막을 형성하는 단계를 포함하여 이루어져, 상기 중간절연막에서의 보이드 발생을 차단할 수 있는 플래시 메모리 및 그의 제조방법에 관한 것이다.

【대표도】

도 7

【색인어】

플래시 메모리, 중간 절연막, 보이드
【명세서】

【발명의 명칭】
플래시 메모리 소자 및 그의 제조방법(Flash Memory Device and Method of Manufacturing the same)

【도면의 간단한 설명】
<1> 도 1은 종래의 플래시 메모리 소자의 셀 어레이를 도시한 평면도,
<2> 도 2는 도 1에 도시된 셀 어레이 일부분의 A-A'선 단면도,
<3> 도 3은 셀 어레이의 측면 결합과 형성시 보이드가 형성된 상태를 도시한 단면도,
<4> 도 4 및 도 7은 본 발명에 따른 플래시 메모리 소자의 제조방법을 설명하기 위한 단면도이다.

*도면의 주요부분에 대한 부호의 설명*
<6> 10: 반도체 기판  20: 터널 산화막
<7> 30: 플로팅 게이트  40: 유전체막
<8> 50: 컨트롤 게이트  60: 스페이서막
<9> 61: 스페이서 패턴  62: 스페이서
<10> 63: 제1 산화막  64: 절화막
<11> 65: 제2 산화막  70: 충간 결연막
<12> 80: 드레인 콘택  A,B: 게이트 영역

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D1: 정영역  D2: 정영역

【발명의 상세한 설명】

【발명의 목적】

【발명이 속하는 기술분야 및 그 분야의 종래기술】

본 발명은 플래시 메모리 소자 및 그의 제조방법에 관한 것으로서, 특히 게이트 영역 사이에서 충전결연막 층착시 보이드 발생을 미연에 방지할 수 플래시 메모리 및 그의 제조방법에 관한 것이다.

반도체 메모리 장치는 DRAM(Dynamic Random Access Memory) 및 SRAM(Static Random Access Memory)과 같이 시간이 지남에 따라 데이터를 잃어버리는 휘발성이면서 데이터의 임출력이 빠른 RAM 제품과, 한번 데이터를 입력하면 그 상태를 유지할 수 있지만 데이터의 임출력이 느린 ROM(Read Only Memory) 제품으로 크게 구분할 수 있다.

휘발성 메모리 장치는 거의 무기한의 축적용량을 갖는데, EEPROM(Electrically erasable and programmable ROM)과 같이 전기적으로 데이터의 임출력이 가능한 플래시 메모리에 대한 수요가 늘고 있다. 상기 플래시 메모리는 전원이 끊겨더라도 저장된 데이터가 손상되지 않는 비휘발성 기억매체이면서도 데이터의 기록, 읽기, 삭제 등의 처리 속도가 비교적 높다는 장점이 있다. 이에 따라, 상기 플래시 메모리는 PC의 BIOS, 셋톱박스, 프린터 및 네트워크 서버등의 데이터 저장용으로 널리 사용되고 있으며 최근에는 디지털 카메라와 휴대폰 등에서
도 많이 이용되고 있는 추세이다.

이러한 플래시 메모리 소자는 셀 트랜지스터들이 직렬로 연결되어 단위 스트。

링(string)을 이루고 이러한 단위 스트링들이 비트라인(bit line)과 접지라인

(ground line)사이에 병렬로 연결되어 고집적화에 유리한 난드형(NAND type)과,

각각의 셀 트랜지스터들이 비트라인과 접지라인사이에 병렬로 연결되어 고속동작에

유리한 노아형(NOR type)으로 구분된다.

도 1은 일반적 노아형 플래시 메모리 소자의 셀 어레이의 구조를 도시한

평면도로서, 상기 셀 어레이의 구조는 채널이 형성되어 열전자(Hot electron)가 발
생하는 액티브 영역과 주입된 열전자가 저장되는 플로팅 게이트와 드레인 콘택트

이 나타나 있으며, 'X'는 셀 어레이의 단위 셀을 나타내는 것으로 두 개의 게이트 영
역이 하나의 드레인 콘택을 공유하는 구조이다.

도 2는 상기 단위 셀인 'X'를 A-A' 방향으로 절단한 단면도로서, 상기 단위

셀은 데이터가 저장되는 플로팅 게이트(102), 상기 플로팅 게이트(102)와 기판

(100) 사이에 형성된 터널 산화막(101)과, 위드라인으로 기능하는 컨트롤 게이트

(103)와, 상기 컨트롤 게이트(103)와 플로팅 게이트(102)를 분리시키기 위하여 이
들 사이에 형성된 유전체막(105)을 포함한다.

그리고, 상기 게이트 영역을 분리 및 보호하기 위하여 산화막(103)을 도포한

다음 접화막(107)을 도포하여 전면시각을 하여 형성된 ON 구조의 스페이서(108)를

포함한다.

그리고, 상기 스페이서(108)를 마스크로 하여 이온주입에 의해 형성된 소스

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/드레인 영역(미도시)을 포함한다.

그리고, 상기 스페이서(108) 상부로에는 BPSG(Boron Phosphorus Silicate Glass)막 또는 HDP-USG의 절연물로 촉간절연막(109)을 형성한 다음, 상기 촉간절연막(109)을 관통하여 비트라인 콘택트 드레인 콘택트(110)으로 도입된다. 여기서, 상기 콘트롤 게이트(103)는 단위 셀의 프로그램(progran), 소거(erase), 독출(read)할 때 워드라인 역할을 하며 드레인 콘택트(110)은 비트라인 역할을 하게 된다.

그러면, 도 3에 도시된 바와 같이, 현재 노아 플래시의 주종을 이루고 있는 0.13μm급의 플래시 메모리 소자 소자에서는 단위 셀에 콘택트 형성되는 공간이 충분하였으나, 단위 셀의 크기가 작아짐에 따라 단위 셀을 이루는 게이트 영역과 게이트 영역 사이의 간격이 줄기 때문에 촉간절연막(109) 중착공정 후 보이드(void)(111)가 발생하게 된다.

이러한 보이드(111)는 각 셀의 특성을 변화시키게 된다. 상기 보이드(111)가 발생하면 위드라인과 워드라인이 서로 다르게 동작되는 문제가 있고, 이후 드레인 콘택트(110) 형성 후 금속물질인 텅스텐이 채워지면 상기 보이드(111)에 의하여 텅스텐이 확산되어 단위 셀을 이루는 셀들이 서로 전기적으로 연결되는 문제가 있다.
이로 인해 워드라인이 올바르게 작동되지 않고 동작 오류를 발생하여 셀 동작에 불량이 발생되는 문제점이 있다.

【발명이 이루고자 하는 기술적 과제】

본 발명은 상기와 같은 종래의 문제점을 해결하기 위한 것으로, 본 발명의
목적은 스페이서 형성 시 중래의 ON(Oxide-Nitride) 구조를 ON(Oxide-Nitride-Oxide) 구조로 형성함으로써 소오스/드레인 형성 후 가장 바깥쪽의 Oxide를 제거함으로써 충간 절연막 및 드레인 콘택트 형성되는 충분한 공간을 확보하여 보이드 발생을 방지할 수 있는 플래시 메모리 소자 및 그의 제조방법을 제공하는 데 있다.

【발명의 구성】

본 발명에 따른 플래시 메모리 소자의 제조방법은, 반도체 기판 상에 터널 산화막, 폴로망 게이트, 유전체막 및 컨트롤 게이트로 구성된 게이트 영역을 형성하는 단계; 상기 게이트 영역의 측벽에 3중 절연막 구조의 스페이서막을 형성하는 단계; 상기 스페이서막을 전면식각하여 스페이져 패턴을 형성하는 단계; 상기 스페이져 패턴의 최외각에 위치한 절연막을 제거하는 단계; 상기 게이트 영역 및 스페이져가 형성된 반도체 기판 상에 충간 절연막을 형성하는 단계를 포함한다.

또한, 본 발명에 따른 플래시 메모리 소자는, 반도체 기판; 상기 반도체 기판에 터널 산화막, 폴로망 게이트, 유전체막 및 컨트롤 게이트가 적층되어 형성된 게이트 영역; 상기 게이트 영역의 측벽에 3중 절연막이 적층된 스페이서막; 상기 스페이서막을 전면식각하여 형성된 스페이서 패턴; 상기 스페이져 패턴의 최외각 절연막을 습식식각에 의해 제거하여 형성된 스페이서; 상기 게이트 영역 및 스페이서 상부로 형성된 충간절연막을 포함한다.

이하, 참조된 도면들을 참조하여 본 발명의 실시예들에 따른 플래시 메모리 소자 및 이의 제조방법에 대하여 상세하게 설명하지만, 본 발명이 하기의 실시예들에 제한되는 것은 아니며, 해당 분야에서 통상의 지식을 가진 자라면 본 발명의 기
술적 사상을 벗어나지 않는 범위 내에서 본 발명의 다양한 다른 형태를 구현할 수 있을 것이다.

한편, 어떤 막이나 다른 막 또는 반도체 기판의 '상'에 있다고 기재되는 경우에 상기 여면 막은 상기 다른 막 또는 반도체 기판에 직접 접촉하여 존재할 수 있고, 또는 그 사이에 제3의 막이 개개되어 질 수도 있다. 또한 도면에서 각 층의 두께나 크기는 설명의 편의 및 명확성 위하여 과장되었다.

플래시 메모리 소자

도 7은 본 발명의 실시예에 따른 플래시 메모리 소자를 나타낸 단면도이다.

본 발명의 플래시 메모리 소자의 설명은 셀, 즉 두 개의 게이트 영역(A,B)이 하나의 드레인 컨택(80)을 공유하는 구조로 형성된 단위 셀을 기준으로 한다. 상기 게이트 영역은 동일한 구조를 가지므로 동일한 도면부호가 사용된다.

반도체 기판(10)의 상부의 게이트 영역(A,B)은 터널 산화막(20), 폴로팅 게이트(30), 유전체막(40) 및 컨트롤 게이트(50)를 포함한다. 여기서 상기 유전체막(40)은 ONO(Oxide-Nitride-Oxide) 구조로 이루어져 있다.

그리고 상기 게이트 영역(A,B)을 분리 및 보호하기 위한 스페이서(62)를 포함한다.

상기 스페이서(62)의 형성은, 우선 상기 단위 셀 전체에 대하여 스페이서막(60)을 충착시킨다. 상기 스페이서막(60)은 제1 산화막(63), 질화막(64), 제2 산화
막(63)으로 구성되며, 순차적으로 상기 게이트 영역(A,B)의 상부로 충착된다. 
이때, 상기 제1 산화막(63)(Oxide)은 TEOS가 150~300Å의 두께로 형성되며, 상기 
질화막(64)(Nitride)은 SiN가 100~300Å의 두께로 형성되며, 상기 제2 산화막 
(63)(Oxide)은 TEOS가 500~800Å의 두께로 형성된다.

상기 게이트 영역(A,B)를 마스크로 하여 저농도 이온주입하여 LDD 영역(미도 
시)을 형성한다.

상기 스페이서막(60)이 중착되면 식각공정을 이용하여 스페이서 패턴(61)이 
형성됨과 동시에 상기 게이트 영역(A)과 게이트 영역(B) 사이의 공간인 제1 갭영역 
(D1)이 형성된다.

그리고, 상기 스페이서 패턴(61)을 이온주입 마스크로 하여 상기 반도체 기 
판(10)에 이온주입하여 형성된 소스/드레인 영역을 포함한다.

이때, 상기 제1 갭영역(D1)은 상기 스페이서 패턴(61)에 의해 좁게 형성되어 
이후 공정인 충간 절연막(70)의 형성시 보이드가 발생되는 문제가 있다.

이를 해결하기 위해 상기 스페이서 패턴(61)의 제2 산화막(63) 습식식각(wet etching) 방법을 사용하여 제거한다. 그러므로, 상기 제2 산화막(63)이 제거되어 상 
기 게이트 영역(A,B)에는 제1 산화막(63)과 질화막(64)으로 구성된 스페이서(62)가 
형성되고 상기 게이트 영역(A, B)의 사이는 넓은 공간을 가지는 제2 갭영역(D2)이 
형성된다.

그리고, 상기 게이트 영역(A,B)의 상부로 형성된 충간 절연막(70)을 포함한
다. 상기 중간 절연막(70)은 PMD(Pre Metal Dielectric)로서 PSG(Phosphorus Silicate Glass), BPSG(Boro-Phosphorus Silicate Glass) 또는 PE-TEOS가 사용된다. 이때 상기 제2 접영역(D2)은 충분한 공간을 가지고 형성되어 상기 중간 절연막(70)의 형성시 보이드가 발생되지 않게 된다.

이후, 상기 게이트 영역과 게이트 영역 사이에 콘택홀을 형성하여 금속물질은 탕스텐(W)을 증착하여 드레인 콘택(80)을 형성한다.

플래시 메모리 소자의 제조방법

상기한 구조를 갖는 플래시 메모리 소자의 제조방법을 도 3 내지 도 7을 참조하여 단계별로 설명한다. 본 발명의 플래시 메모리 소자의 제조방법의 설명은 두 개의 셀 즉 두 개의 게이트 영역(A,B)이 하나의 드레인 콘택(90)을 공유하는 구조로 형성된 단위 셀을 기준으로 한다.

도 4에 도시된 바와 같이, 반도체 기판(10) 상에 단위 셀을 이루는 두 개의 게이트 영역(A, B)을 각각 형성한다. 상기 두 개의 게이트 영역(A,B)은 동일한 형태므로 게이트 영역의 구성요소는 동일한 부호가 사용된다.

상기 게이트 영역(A, B)은 데이터가 저장되는 플로팅 게이트(30), 상기 플로팅 게이트(30)와 상기 반도체 기판(10) 사이에 형성된 터널 산화막(20), 위드라인으로 기능하는 컨트롤 게이트(50), 상기 컨트롤 게이트(50)와 플로팅 게이트(30)를 분리시키기 위하여 이들 사이에 형성된 유전체막(40)으로 이루어진다. 여기서, 상
기 반도체 기판(10)은 소자분리막(미도시) 형성, 웨(미도시) 형성 및 채널(미도시) 형성공정이 완료된 상태이다. 그리고 상기 유전체막(40)은 ONO(Oxide-Nitried-Oxide) 구조로 이루어져 있다.

상기 케이트 영역(A,B)이 형성된 후에는 이온주입공정으로 상기 케이트 영역 (A,B) 사이의 반도체 기판(10)에 저농도 불순물을 이온주입하여 LDD(미도시)를 형성한다.

그리고, 상기 케이트 영역(A,B)을 분리 및 보호하기 위하여 스페이서막(60)을 형성한다.

상기 스페이서막(60)은 제1 산화막(63)(Oxide), 절화막(64)(Nitride) 및 제2 산화막(63)(Oxide)을 순차적으로 상기 단위 셀 전체에 대하여 충착하여 형성한다.

여기서 상기 제1 산화막(63)(Oxide)은 TEOS가 150-300Å의 두께로 형성되며, 상기 절화막(64)(Nitride)은 SiN가 100-300Å의 두께로 형성되며, 상기 제2 산화막 (63)(Oxide)은 TEOS가 500-800Å의 두께로 형성된다.

그 다음, 도 5에 도시된 바와 같이, 상기와 같이 3중막 구조로 형성된 스페이서막(60)을 전면식각 방법을 사용하여 식각시키면 상기 케이트 영역(A,B)의 양쪽으로 스페이서 패턴(61)이 형성되고 상기 케이트 영역(A)과 케이트 영역(B) 사이에 빈 공간인 제1 갯영역(D1)이 형성되면서 상기 제1 갯영역(D1)의 반도체 기판(10) 표면은 노출되어 진다. 이때, 상기 절화막(64)이 식각경지막으로 사용되어 식각공정이 상기 절화막(64)에서 종료되도록 한다.
그리고 상기 스페이서 패턴(61)을 이온주입 마스크로 사용하여 이온주입 공정을 진행하여 반도체 기판(10)의 고품도 불순물 영역인 소오스/드레인 영역(미도시)을 형성한다.

그 다음, 상기 제2 산화막(63)을 제거한다. 상기 게이트 영역(A)과 게이트 영역(B) 사이의 제1 접영역(D1)을 증가시켜 이후 트랜스 콘택을 형성하는 공정의 공정마진을 충분히 확보하고, 제거되는 상기 제2 산화막(63)의 두께 맨큼 게이트 영역(A,B) 사이의 간격을 좁혀 소자의 집적도를 증가시킬 수 있게 된다.

따라서, 상기 스페이서 패턴(61)의 가장 바깥 쪽에 위치한 제2 산화막(63)을 제거한다. 이때, 상기 스페이서 패턴(61)의 프로파일(Profile)이 바뀌어도 플래시 메모리 소자의 전체 동작에 영향을 미치지 않게 된다.

여기서, 상기 제2 산화막(63)의 식각은 습식식각 공정을 이용하여 BHF용액으로 제거한다. 특히, 상기 제2 산화막(63)의 식각공정시 동일한 물질인 제1 산화막(63)의 외측부분도 함께 식각되므로, 노 6에 도시된 스페이서(62) 및 제2 접영역(D2)이 형성된다.

이것은 상기 스페이서 패턴(61)을 형성한 후 콘택이 형성되어야 할 제1 접영역(D1)이 좁기 때문에 충간 절연막(70)의 형성시 보이드가 발생할 수 있으므로, 이를 방지하기 위해 상기 스페이서 패턴(61)의 제2 절막막(64)을 제거함으로써 상기 게이트 영역(A)과 게이트 영역(B) 사이의 충분한 공간인 제2 접영역(D2)을 확보하여 충간 절연막(70) 형성시 보이드의 발생을 미연에 제거하기 위한 것이다. 특히, 상기 제2 산화막(63)의 두께로 인해 상기 제2 산화막(63)이 제거되면 상기
제2 접영역(D2)은 충분한 공간을 확보하게 된다.

그 다음, 도 7에 도시된 바와 같이 상기 게이트 영역의 상부로 충간 절연막(70)을 형성한다. 상기 충간 절연막(70)은 PMD(Pre Metal Dielectric)로서 PSG(Phosphorus Silicate Glass), BPSG(Boro-Phosphorus Silicate Glass) 또는 PTEOS가 사용된다. 이때 상기 제2 접영역(D2)은 충분한 공간을 가지고 형성되어 상기 충간 절연막(70)의 형성시 보이드가 발생되지 않는다.

이 다음, 상기 게이트 영역(A)과 게이트 영역(B)의 사이에 콘텍을 형성한 후 금속물질인 텅스텐(W)을 증착하여 드레인 콘텍(80)을 형성한다. 이때 상기 충간 절연막(70)의 보이드가 발생되지 않았기 때문에 상기 텅스텐의 증착시 보이드에 의한 확산현상이 나타나지 않으므로 폴래시 메모리 소자는 정상적인 동작을 수행할 수 있게 된다.

이상과 같이 본 발명에 따른 폴래시 메모리 소자 및 그 제조방법을 예시한 도면을 참조로 하여 설명하였으나, 본 명세서에 개시된 실시예와 도면에 의해 본 발명이 한정되는 것은 아니며, 본 발명의 기술사항 범위 내에서 당업자에 의해 다양한 변형이 이루어질 수 있음을 본론이다.

【발명의 효과】

이상에서 설명한 바와 같이, 본 발명에 따른 폴래시 메모리 소자 및 그 제조방법에 의하면, 게이트 영역의 스페이서가 ONO(Oxide-Nitride-Oxide) 구조로 형성
이로 인해 비트라인 형성을 위한 드레인 콘택트 형성 시 워드라인이 전기적으로 연결되는 것을 방지하여 폴래시 메모리 소자의 신뢰성을 확보할 수 있을 뿐만 아니라 소자의 고집적화를 실현할 수 있다.
【특허청구범위】

【청구항 1】
반도체 기판 상에 터널 산화막, 플로팅 게이트, 유전체막 및 컨트롤 게이트로 구성된 게이트 영역을 형성하는 단계;
상기 게이트 영역의 측벽에 3종 절연막 구조의 스페이서막을 형성하는 단계;
상기 스페이서막을 전면시각하여 스페이서 패턴을 형성하는 단계;
상기 스페이서 패턴의 최외각에 위치한 절연막을 제거하는 단계;
상기 게이트 영역 및 스페이서가 형성된 반도체 기판 상에 충간 절연막을 형성하는 단계를 포함하는 플래시 메모리 소자의 제조방법.

【청구항 2】
제1항에 있어서,
상기 스페이서의 3종 절연막 중 가장 바깥 측에 위치한 절연막의 제거는 습식식각 방법을 사용하는 것을 포함하는 플래시 메모리 소자의 제조방법.

【청구항 3】
제2항에 있어서,
상기 습식식각 시 식각용액으로는 BHF 용액이 사용되는 것을 포함하는 플래시 메모리 소자의 제조방법.

【청구항 4】
제1항에 있어서,
상기 스페이서막은 제1 산화막, 절화막, 제2 산화막이 순차적으로 적층된 것을 포함하는 플레시 메모리 소자 및 그의 제조방법.

【청구항 5】

제4항에 있어서,

상기 스페이서막의 제1 산화막은 TEOS이고, 절화막은 SiN이고, 제2 산화막은 TEOS인 것을 포함하는 플레시 메모리 소자 및 그의 제조방법.

【청구항 6】

제5항에 있어서,

상기 제1 산화막은 150~300A, 절화막은 100~300A, 제2 산화막은 500~800A의 두께로 형성된 것을 포함하는 플레시 메모리 소자 및 그의 제조방법.

【청구항 7】

제1항에 있어서,

상기 스페이서는 제1 산화막, 절화막으로 구성된 것을 포함하는 플레시 메모리 소자 및 그의 제조방법.

【청구항 8】

반도체 기판;

상기 반도체 기판에 터널 산화막, 플로팅 게이트, 유전체막 및 컨트롤 게이트가 적층되어 형성된 게이트 영역;

상기 게이트 영역의 측벽에 3층 절연막이 적층된 스페이서막;
상기 스페이서막을 전면식각하여 형성된 스페이서 패턴;

상기 스페이서 패턴의 최외각 절연막을 습식식각에 의해 제거하여 형성된 스페이서;

상기 케이트 영역 및 스페이서 상부로 형성된 충합절연막을 포함하는 플래시 메모리 소자.

【청구항 9】

제8항에 있어서,

상기 스페이서막은 제1 산화막, 절화막, 제2 산화막이 순차적으로 적층된 것을 포함하는 플래시 메모리 소자 및 그의 제조방법.

【청구항 10】

제9항에 있어서,

상기 스페이서막의 제1 산화막은 TEOS 이고, 절화막은 SiN이고, 제2 산화막은 TEOS 인 것을 포함하는 플래시 메모리 소자 및 그의 제조방법.

【청구항 11】

제10항에 있어서,

상기 제1 산화막은 150-300Å, 절화막은 100-300Å, 제2 산화막은 500-800Å의 두께로 형성된 것을 포함하는 플래시 메모리 소자 및 그의 제조방법.

【청구항 12】

제12항에 있어서,
상기 스페이서는 제1 산화막, 질화막으로 구성된 것을 포함하는 플래시 메모리 소자 및 그의 제조방법.
도면

도 1
【도 7】
NOTICE TO FILE CORRECTED APPLICATION PAPERS

Filing Date Granted

An application number and filing date have been accorded to this application. The application is informal since it does not comply with the regulations for the reason(s) indicated below. Applicant is given TWO MONTHS from the date of this Notice within which to correct the informalities indicated below. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

The required item(s) identified below must be timely submitted to avoid abandonment:

- Replacement drawings in compliance with 37 CFR 1.84 and 37 CFR 1.121(d) are required. The drawings submitted are not acceptable because:
  - The drawings submitted to the Office are not electronically reproducible because portions of figures 8 are missing and/or blurry.

Applicant is cautioned that correction of the above items may cause the specification and drawings page count to exceed 100 pages. If the specification and drawings exceed 100 pages, applicant will need to submit the required application size fee.
Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
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CONFIRMATION NO. 2246

60803
SHERR & NOURSE, PLLC
620 HERNDON PARKWAY
SUITE 200
HERNDON, VA 20170

Date Mailed: 11/26/2007

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections.

Applicant(s)  
Jin-Ha Park, Gyeonggi-do, KOREA, REPUBLIC OF;  
Jae-Hee Kim, Gyeonggi-do, KOREA, REPUBLIC OF;

Power of Attorney: None

Domestic Priority data as claimed by applicant

Foreign Applications  
REPUBLIC OF KOREA 10-2006-0120171 11/30/2006

If Required, Foreign Filing License Granted: 11/20/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is US 11/932,273

Projected Publication Date: To Be Determined - pending completion of Corrected Papers

Non-Publication Request: No

Early Publication Request: No
FLASH MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME

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DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

Attorney Docket Number 604-0117
First Named Inventor Jin-Ha PARK et al.

COMPLETE IF KNOWN

Application Number
Filing Date October 31, 2007
Art Unit TBA
Examiner Name TBA

I hereby declare that:

Each inventor's residence, mailing address, and citizenship are as stated below next to their name.

I believe the inventor(s) named below to be the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

FLASH MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME

(Title of the Invention)

the specification of which
☐ is attached hereto

☐ was filed on (MM/DD/YYYY) as United States Application Number or PCT International Application Number and was amended on (MM/DD/YYYY) (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent, inventor's or plant breeder's rights certificate(s), or any PCT International application having a filing date before that of the application on which priority is claimed.

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Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

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# Declaration — Utility or Design Patent Application

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

**NAME OF SOLE OR FIRST INVENTOR:**

[ ] A petition has been filed for this unsigned inventor

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<td>PARK</td>
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Inventor’s Signature:  

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Date:  

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[☑️ Additional inventors or legal representative are being named on the 1 supplemental sheet(s) PTO/SB/22A or GLR attached hereto.]

[Page 2 of 2]
**DECLARATION**

**ADDITIONAL INVENTOR(S)**

**Supplemental Sheet**

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This collection of information is required by 36 U.S.C. 116 and 57 CFR 1.58. The information is required to obtain or retain a benefit by the public which is not the subject of the USPTO to process an application. Confidentiality is governed by 36 U.S.C. 122 and 37 CFR 1.17 and 1.14. This collection is estimated to take 21 minutes to complete, including gathering, preparing, and submitting the completed application forms to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and whether the form should be completed electronically are kindly invited. This sheet is not required. If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.
FLASH MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME


BACKGROUND

Semiconductor memory devices may be categorized as read only memory (ROM) devices or volatile RAM devices such as dynamic random access memory (DRAM) and static random access memory (SRAM). ROM devices can maintain data over time, but have low I/O data rates. RAM devices have high I/O data rates, but gradually lose data over time.

Non-volatile memory devices have an almost unlimited accumulation capacity. There has been increasing demand for flash memory devices such as electrically erasable and programmable ROM having I/O data capabilities. Flash memory is a non-volatile memory medium without damage on the stored data even though power is off. Flash memory has an advantage such as relatively high writing, reading and erasing processing speed. Accordingly, flash memory may be used for PC bias or for storing data in a set-top box, a printer, a network server and also for digital cameras and mobile phones.

Flash memory devices may be categorized as NAND type devices or NOR type devices. NAND flash memory devices may include cell transistors that may be connected in series to form a unit string. The unit strings may be connected in parallel between a bit line and a ground line, thereby allowing high integration. NOR flash memory devices may include cell transistors that may be connected in parallel between a bit line and a ground line, thereby allowing high-speed operation.
As illustrated in example FIG. 1, the structure of a cell array may include an active region in which a channel is formed to generate hot electrons, a floating gate for storing injected hot electrons and a drain contact. According to the structure of the cell array, two gate regions may share one drain contact in a unit cell.

Example FIG. 2 illustrates a cross-sectional view of the unit cell of example FIG. 1 taken along a line A-A'. The unit cell may include tunnel oxide film 101 formed on and/or over semiconductor substrate 100. Floating gate 102 for storing data may be formed on and/or over tunnel oxide film 101. Dielectric film 105 may be formed on and/or overfloating gate 102. Control gate 103 serving as a word line, may be formed on and/or over dielectric film 105. Thus, dielectric film 105 separates floating gate and control gate 103. A pair of spacers 108 having an oxide-nitride (ON) structure may be formed by sequentially coating and etching oxide film 106 and nitride film 107 to separate and protect the gate region. The unit cell may further include a source/drain region formed by ion implantation using spacer 108 as a mask. Interlayer insulating film 109 may be formed on and/or over control gate 103 and spacer 108 using a boron phosphorus silicate glass (BPSG) film or an insulating material such as HDP-USG. Drain contact 110 serving as a bit line contact may be formed to pass through interlayer insulating film 109. Control gate 103 serves as a word line and drain contact 110 serves as a bit line in programming, erasing and reading the unit cell.

As illustrated in example FIG. 3, the unit cell may have sufficient space for forming a contact in a flash memory device of the order of 0.13 um, which is a main type of the NOR type flash memory device. However, as the size of the unit cell is smaller, a distance between the gate regions forming the unit cells may be reduced, thereby generating void 111 after a deposition process for forming interlayer insulating film 109. Void 111 may change the characteristics of the respective cells. When void 111 is generated, there is a
problem that the word lines may operate differently. If a metal material such as tungsten (W) is filled after formation of drain contact 110, the tungsten may be diffused into void 111. This may in turn generate a contact bridge phenomenon in which tungsten forms a bridge by another contact. Accordingly, the gate formed in the word line may not operate properly and thus generates an operation error, thereby causing defects in the cell operation.

**SUMMARY**

Embodiments relate to a flash memory device and a method of manufacturing the same in which a spacer of a gate region can be formed in an oxide-nitride-oxide (ONO) structure instead of a oxide-nitride (ON) structure. Moreover, a source/drain region can be formed using the spacer, and the outermost oxide layer in the ONO structure can be removed, thereby prevent generation of a void by ensuring sufficient space for forming an interlayer insulating film and a drain contact.

Embodiments relate to a method of manufacturing a flash memory device that can include at least one of the following steps: forming a gate region including a tunnel oxide film, a floating gate, a dielectric film and a control gate over a semiconductor substrate; forming a spacer film having a multi-layer insulating film structure against a sidewall of the gate region; forming a spacer pattern by performing an entire surface etching on the spacer film; removing an insulating film disposed at an outermost position of the spacer pattern; and then forming an interlayer insulating film over the semiconductor substrate with the gate region and a spacer formed thereon.

Embodiments relate to a flash memory device that can include a semiconductor substrate; a gate region including a tunnel oxide film, a floating gate, a dielectric film and a control gate formed over the semiconductor substrate; a spacer film including an lower
spacer film and an upper spacer film formed on a sidewall of the gate region; and an interlayer insulating film formed over the gate region and the spacer.

**DRAWINGS**

Example FIGS. 1 to 3 illustrate a cell array of a flash memory device.

Example FIGS. 4 to 8 illustrate a flash memory device, in accordance with embodiments.

**DESCRIPTION**

When it is described that a certain film is disposed “on” another film or a semiconductor substrate, the certain film may be in direct contact with the other film or the semiconductor substrate or a third film may be interposed therebetween. Further, the thickness and size of the respective layers in the drawings are exaggerated for convenience and clearness of explanation.

As illustrated in example FIG. 4, semiconductor substrate 10 can be divided into a logic region and a cell or SONOS region. The logic region can include a logic PMOS region and a logic NMOS region. The thickness of a gate oxide film formed in the logic region may vary according to a low-voltage region, a high-voltage region and an ultrahigh-voltage region.

In accordance with embodiments, a flash memory device may include a plurality of gate patterns A, B and C formed in the cell region and the logic region, respectively. A unit cell has a structure in which two gate regions A and B can share drain contact 80. The contact in the logic region is assigned for gate region C. The same reference numerals are used for the same configurations in the gate regions A, B and C. Semiconductor substrate 10 can include a device isolation film, a well and a channel.
Gate region A or B of the cell region can include tunnel oxide film 20 formed on and/or over semiconductor substrate 10. Floating gate 30 for storing data can be formed on and/or over semiconductor substrate 10 including tunnel oxide film 20. Gate control 50 can serve as a word line, and dielectric film 40 can be formed between floating gate 30 and control gate 50 to separate them from each other. Dielectric film 40 can have a multi-layer structure such as an oxide-nitride-oxide (ONO) structure.

Gate region C of the logic region can include gate oxide film 21 formed on and/or over semiconductor substrate 10 and polysilicon gate 31 formed on and/or over gate oxide film 21. A lightly doped drain (LDD) region, which can serve as a low concentration impurity region, may be disposed between gate regions A and B of the cell region. The unit cell can include spacer 62 for separating and protecting gate regions A and B. Spacer 62 can have a multi-layer stacked structure including lower spacer film 63 and upper spacer film 64. Lower spacer film 63 may be composed of an oxide-based material and upper spacer film layer 64 may be composed of a nitride-based material.

Interlayer insulating film 70 can be formed on and/or over gate regions A, B and C. The flash memory device in accordance with embodiments has sufficient space between gate regions A and B. Accordingly, a void is not generated when interlayer insulating film 70 is formed. Thereafter, a contact hole can be formed on and/or over a side portion of gate region C and also between gate regions A and B. A metal material such as tungsten (W) can be filled in the contact hole to form drain contact 80 and contact 81.

As illustrated in example FIG. 5, a plurality of gate patterns A, B and C can be formed in the cell region and the logic region of semiconductor substrate 10, respectively. Tunnel oxide film 20 for storing data, floating gate 30, dielectric film 40 and control gate 50 can be sequentially stacked and patterned on and/or over semiconductor substrate 10 to form gate regions A and B. Gate region C of the logic region can be formed by sequentially
stacking and patterning gate oxide film 21 and polysilicon gate 31 on and/or over semiconductor substrate 10.

After formation of gate regions A, B and C, an LDD can be formed between the gate regions on and/or over semiconductor substrate 10 using ion implantation of low concentration impurities through an ion implantation process and gate regions A and B as masks.

A spacer film having a multi-layer insulating film structure can be formed on and/or over a sidewall of gate regions A, B and C. The multi-layer insulating film structure can be formed by sequentially depositing first oxide film 63, nitride film 64 and second oxide film 65 on and/or over the entire unit cell. First oxide film 63 may be composed of tetraethyl orthosilicate (TEOS) at a thickness between approximately 150 to 300Å. Nitride film 64 may be composed of SiN at a thickness between approximately 100 to 300Å. Second oxide film 65 may be composed of TEOS at a thickness between approximately 500 to 800Å.

As illustrated in example FIG. 6A, after formation of spacer film 60 of a triple insulating film structure is formed, spacer film 60 can be etched using an entire surface etching method to form spacer pattern 61 at opposite sides of gate regions A, B and C. First gap region D1 can be formed as an empty space to expose an uppermost surface of semiconductor substrate 10 between gate regions A and B. Spacer pattern 61 may be formed having a substantially spherical shape using reactive ion etching. The outermost ends of first oxide film 63, nitride film 64 and second oxide film 65 may be exposed using an etching process. Nitride film 64 can be used as an etching stop film such that an etching process can be stopped at nitride film 64.

An ion implantation process can be performed using spacer pattern 61 and gate regions A, B and C as ion implantation masks to form source/drain region 35 having a high concentration impurity region on and/or over semiconductor substrate 10. Source/drain
region 35 can have conductivity as ions are implanted therein using an ion implantation process.

As illustrated in example FIG. 7, first gap region D1 can be narrowly formed adjacent spacer pattern 61. A void may be generated when interlayer insulating film 70 is subsequently formed. However, in order to prevent generation of the void, second oxide film 65 disposed at an outermost position of spacer pattern 61 can be removed. Second oxide film 65 may be etched using a wet etching method.

Second oxide film 65 may be removed by etching second oxide film 65 using a buffered HF (BHF) solution. Second oxide film 65 may be removed by soaking semiconductor substrate 10 in an etching solution such as hydrogen fluoride (HF). A mixing ratio of hydrogen fluoride (HF) and water (H₂O) may be in a range between approximately 1:100 to 1:200. The processing time can be in a range of between approximately 100 to 140 seconds. When second oxide film 65 is etched, an outer portion of first oxide film 63 which is the same material as the second oxide film 65 can also be etched, thereby forming spacer 62 and second gap region D2. Nitride film 64 can be used as an etching stop film in the etching process for removing second oxide film 65. Even though a profile of spacer pattern 61 is changed into spacer 62, there is no effect on the operation of the flash memory device. As a result, since second oxide film 65 is removed, spacer 62 including first oxide film 63 and nitride film 64 can be formed on and/or over gate regions A and B. Second gap region D2 having a large space can be formed between gate regions A and B.

Example FIG. 8 illustrates a photograph obtained by a scanning electron microscope (SEM) after removal of second oxide film 65 in which poly is used as a capping layer.

As illustrated in example FIG. 8, after poly is deposited as capping layer 200, a photograph was taken using an SEM. It can be seen that the second oxide film is removed up to the nitride film. First gap region D1 between gate regions A and B is increased to the
second gap region D2. Accordingly, it can be possible to sufficiently ensure a process margin in the following step for forming a drain contact. Moreover, it can be possible to reduce the distance between gate regions A and B to an amount substantially equal to the thickness of the removed second oxide film 65, thereby increasing the integration density of the flash memory device.

As illustrated in example FIG. 4, interlayer insulating film 70 can be formed on and/or over gate regions A, B and C. Interlayer insulating film 70 can be composed of a pre-metal dielectric (PMD) such as at least one of phosphorus-doped silicate glass (PSG), borophosphorus silicate glass (BPSG) and plasma enhanced TEOS (PE-TEOS). Because second gap region D2 has a sufficient space, a void is not generated when interlayer insulating film 70 is formed.

After a contact hole is formed between gate regions A and B and in a side portion of gate region C, a metal material such as tungsten (W) can be formed in the contact hole, thereby forming drain contact 80 and contact 81. Since the void of is not generated in interlayer insulating film 70, a diffusion phenomenon is not generated during the deposition of tungsten. Accordingly, the flash memory device can perform a normal operation.

Although gate regions A and B and gate region C can be formed simultaneously, gate regions A and B may be formed separately from the formation of gate region C.

In accordance with embodiments, a flash memory device and a method of manufacturing the flash memory device may include a spacer of a gate region formed having an oxide-nitride-oxide (ONO) structure and a source/drain region formed using the ONO structure. The outermost oxide of the ONO structure can be removed to form an interlayer insulating film to provide sufficient space between the gate regions. Accordingly, formation of a void in the interlayer insulating film can be prevented, and thus, also prevents a word line from being electrically connected to a drain contact for forming a bit
line. Meaning, a contact bridge phenomenon can be prevented, thereby ensuring reliability of the flash memory device and realizing high integration.

Although embodiments have been described herein, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the spirit and scope of the principles of this disclosure. More particularly, various variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the disclosure, the drawings and the appended claims. In addition to variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.
WHAT IS CLAIMED IS:

1. A method comprising:
   forming a gate region including a tunnel oxide film, a floating gate, a dielectric film
   and a control gate over a semiconductor substrate;
   forming a spacer film having a multi-layer insulating film structure against a
   sidewall of the gate region;
   forming a spacer pattern by performing an entire surface etching on the spacer film;
   removing an insulating film disposed at an outermost position of the spacer pattern;
   and then
   forming an interlayer insulating film over the semiconductor substrate with the gate
   region and a spacer formed thereon.

2. The method of claim 1, wherein the insulating film disposed at the outermost
   position of the multi-layer insulating film is removed using a wet etching method.

3. The method of claim 2, wherein a BHF solution is used as an etching
   solution in the wet etching method.

4. The method of claim 1, wherein forming the spacer film comprises
   sequentially depositing a first oxide film, a nitride film and a second oxide film.

5. The method of claim 4, wherein the first oxide film comprises TEOS.

6. The method of claim 5, wherein the second oxide film comprises TEOS.
7. The method of claim 6, wherein the nitride film comprises SiN.

8. The method of claim 7, wherein the first oxide film has a thickness between approximately 150 to 300Å.

9. The method of claim 8, wherein the nitride film has a thickness between approximately 100 to 300Å.

10. The method of claim 9, wherein the second oxide film has a thickness between approximately 500 to 800Å.

11. The method of claim 1, further comprising forming a source/drain region through an ion implantation process using the spacer pattern and the gate region as a mask before removing the insulating film disposed at an outermost position of the spacer pattern.

12. An apparatus comprising:

a semiconductor substrate;

a gate region including a tunnel oxide film, a floating gate, a dielectric film and a control gate formed over the semiconductor substrate;

a spacer film including an lower spacer film and an upper spacer film formed on a sidewall of the gate region; and

an interlayer insulating film formed over the gate region and the spacer.

13. The apparatus of claim 12, wherein the lower spacer film comprises an oxide film.
14. The apparatus of claim 13, wherein the upper spacer film comprises a nitride film.

15. The apparatus of claim 14, wherein the oxide film comprises TEOS.

16. The apparatus of claim 15, wherein the nitride film comprises SiN.

17. The apparatus of claim 16, wherein the first oxide film has a thickness of between approximately 150 to 300Å.

18. The apparatus of claim 17, wherein the nitride film has a thickness of between approximately 100 to 300Å.

19. The apparatus of claim 12, wherein the interlayer insulating film comprises a pre-metal dielectric material.

20. The apparatus of claim 19, wherein the pre-metal dielectric material comprises at least one of phosphorus-doped silicate glass, boro-phosphorus silicate glass and plasma enhanced TEOS.
ABSTRACT

A flash memory device having a spacer of a gate region formed in an oxide-nitride-oxide (ONO) structure and a source/drain region formed using the ONO structure. The outermost oxide in the ONO structure is removed and an interlayer insulating film is formed to ensure sufficient space between the gate regions. Thus, it is possible to prevent a void from being generated in the interlayer insulating film and prevent a word line from being electrically connected to a drain contact for forming a bit line.
FIG. 1
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<td>First Named Inventor/Applicant Name:</td>
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### Utility Filing Fees

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| Petition:                    |          |          |        |                      |
| Patent-Appeals-and-Interference: |          |          |        |                      |</p>
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<td><strong>First Named Inventor/Applicant Name:</strong></td>
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<td><strong>Customer Number:</strong></td>
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**Payment information:**

- Submitted with Payment: yes
- Payment was successfully received in RAM: $1030
- RAM confirmation Number: 4195

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**Warnings:**

**Information:**

2. Fee Worksheet (PTO-06)

| Fee-Info.pdf | 8380 | no | 2 |

**Warnings:**

**Information:**

Total Files Size (in bytes): 2627286

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.
# PATENT APPLICATION FEE DETERMINATION RECORD

**Substitute for Form PTO-875**

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## APPLICATION AS AMENDED – PART II

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* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" in this space is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" in this space is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending on the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9999 and select option 2.