ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

**Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)**
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Sang-Woo Nam, Chungcheongbuk-do, KOREA, REPUBLIC OF;
**PART B - FEE(S) TRANSMITTAL**

Complete and send this form, together with applicable fee(s), to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

**INSTRUCTIONS:** This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

**CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)**

60803 7590 07/06/2009

SHERR & VAUGHN, PLLC
620 HERndon PARKWAY
SUITE 320
HERNDON, VA 20170

**APPLICATION NO.** 11/849,673  **FILING DATE** 09/04/2007  **FIRST NAMED INVENTOR** Sang-Woo Nam  **ATTORNEY DOCKET NO.** 604-0075  **CONFIRMATION NO.** 6118

**TITLE OF INVENTION:** METHOD OF FABRICATING FLASH MEMORY DEVICE WITH INCREASED COUPLING RATIO

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**EXAMINER** FAN, SU JYA  **ART UNIT** 2823  **CLASS-SUBCLASS** 438-257000

1. **Change of correspondence address or indication of "FEE Address" (37 CFR 1.55).**
   - Change of correspondence address (or Change of Correspondence Address Form PTO/SB/122) attached.
   - "FEE Address" indication (or "FEE Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

   1. Sherr & Vaughn, PLLC
   2. 
   3. 

3. **ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)**
   **PLEASE NOTE:** Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filling an assignment.

   **(A) NAME OF ASSIGNEE** Dongbu HiTek Co., Ltd.

   **(B) RESIDENCE (CITY AND STATE OR COUNTRY)** Seoul, Republic of Korea

Please check the appropriate assignee category or categories (will not be printed on the patent):

- Individual
- Corporation or other private group entity
- Government

4a. The following fee(s) are submitted:
   - Issue Fee
   - Publication Fee
   - Advance Order - # of Copies

4b. **Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)**
   - A check is enclosed.
   - Payment by credit card. Form PTO-2038 is attached.
   - The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number __________ (enclose an extra copy of this form).

5. **Change in Entity Status (from status indicated above)**
   - a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
   - b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

   **NOTE:** The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

   **Authorized Signature** [Signature]

   **Typed or printed name** Daniel H. Sherr

   **Date** 10/2/2009

   **Registration No.** 46,425

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
**Electronic Patent Application Fee Transmittal**

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Filed as Large Entity

**Utility under 35 USC 111(a) Filing Fees**

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**Title of Invention:**
METHOD OF FABRICATING FLASH MEMORY DEVICE WITH INCREASED COUPLING RATIO

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<th><strong>First Named Inventor/Applicant Name:</strong></th>
<th>Sang-Woo Nam</th>
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<td><strong>Filer:</strong></td>
<td>Daniel Hilary Sherr</td>
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- Payment Type: Credit Card
- Payment was successfully received in RAM: $1810
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- Deposit Account
- Authorized User

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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.
NOTICE OF ALLOWANCE AND FEE(S) DUE

SHERR & VAUGHN, PLLC
620 HERNDON PARKWAY
SUITE 320
HERNDON, VA 20170

EXAMINER
FAN, SU JYA
ART UNIT 2823
PAPER NUMBER

APPLICATION NO. 11/849,673
FILING DATE 09/04/2007
FIRST NAMED INVENTOR Sang-Woo Nam
ATTORNEY DOCKET NO. 604-0075
CONFIRMATION NO. 6118

TITLE OF INVENTION: METHOD OF FABRICATING FLASH MEMORY DEVICE WITH INCREASED COUPLING RATIO

APPLN. TYPE SMALL ENTITY ISSUE FEE DUE $1510
PUBLIC FEE DUE $300
PREV. PAID ISSUE FEE $0
TOTAL FEE(S) DUE $1810
DATE DUE 10/06/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Page 1 of 3

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.
PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

or Fax

(571) 273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate “FEE ADDRESS” for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60803 7590 07/06/2009

SHERR & VAUGHN, PLLC
620 HERndon PARKWAY
SUITE 320
HERndon, VA 20170

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Date)

EXAMINER
FAN, SU JYA
2823
438-257000

APPLICATION NO.  FILING DATE  FIRST NAMED INVENTOR  ATTORNEY DOCKET NO.  CONFIRMATION NO.

11/849,673  09/04/2007  Sang-Woo Nam  604-0075  6118

TITLE OF INVENTION: METHOD OF FABRICATING FLASH MEMORY DEVICE WITH INCREASED COUPLING RATIO

APPLN. TYPE  SMALL ENTITY  ISSUE FEE DUE  PUBLICATION FEE DUE  PREV. PAID ISSUE FEE  TOTAL FEE(S) DUE  DATE DUE

nonprovisional  NO  $1510  $300  $0  $1810  10/06/2009

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): Individual Corporation or other private group entity Government

4a. The following fee(s) are submitted:

☐ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

☐ A check is encosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number __________________________ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature

Date

Typed or printed name

Registration No.

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.
Notice of Allowability

Application No. 11/849,673
Applicant(s) NAM, SANG-WOO
Examiner MICHELE FAN
Art Unit 2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 5/12/09.

2. ☑ The allowed claim(s) is/are 1,3-13 and 15.

3. □ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☑ All   b) ☑ Some*   c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. ______.
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
   * Certified copies not received: ______.

   Applicant has THREE MONTHS FROM THE “MAILING DATE” of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
   THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. □ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER’S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. □ CORRECTED DRAWINGS (as “replacement sheets”) must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson’s Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date ______.
   (b) □ including changes required by the attached Examiner’s Amendment / Comment or in the Office action of Paper No./Mail Date ______.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. □ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner’s comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.
EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

- This application is in condition for allowance except for the presence of claims 16-20 directed to an invention non-elected without traverse. Accordingly, claims 16-20 been cancelled.

- The title of application has been changed to "Method of Fabricating Flash Memory Device with Increased Coupling Ratio". Authorization for this examiner's amendment was given in a telephone interview with Daniel Sherr on July 1, 2009.

EXAMINER'S REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance: upon consideration of the prior art and the attorney/applicant's arguments, the prior art alone or in combination, cannot anticipate or render obvious the following limitations in claim 1: "forming a photoresist as a mask on the first insulation film; performing an
etching process using the photoresist as a mask...forming a hard mask for prevention of oxidation on the semiconductor substrate."

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

For the prosecution record, this office action introduces prior art, Kim et al., US Publication No. 2002/0187609 A1.

Referring to fig. 8A, Kim teaches a floating gate (24) that is larger than the tunnel oxide film (14) in size of area, to obtain a coupling ratio between the floating gate and the control gate, as required by the limitations of claim 1. See Abstract, pg. 1, ¶4-6, pg. 2-4, ¶16-46, fig. 4A-8B.

However, Kim lacks forming a photoresist as a mask on the first insulation film; performing an etching process using the photoresist as a mask...forming a hard mask for prevention of oxidation on the semiconductor substrate (as indicated above).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHELE FAN whose telephone number is (571)270-7401. The examiner can normally be reached on M-F from 8 am to 4 pm (EST).
If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Matthew Smith, can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/M. F./
Examiner, Art Unit 2823

/Matthew S. Smith/
Supervisory Patent Examiner, Art Unit 2823

1 July 2009
# Notice of References Cited

**U.S. PATENT DOCUMENTS**

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U.S. Patent and Trademark Office
PTO-892 (Rev. 01-2001)
### Index of Claims

**Application/Control No.**
11849673

**Applicant(s)/Patent Under Reexamination**
NAM, SANG-WOO

**Examiner**
MICHELE FAN

**Art Unit**
2823

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/MICHELE FAN/
Examiner Art Unit 2823

(MICHELE FAN)
(Examiner)
(Dated)

/MATTHEW SMITH/
Supervisory Patent Examiner Art Unit 2823

(MATTHEW SMITH)
(Primary Examiner)
(Dated)

Total Claims Allowed:
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**APPLICANTS**
Sang-Woo Nam, Chungcheongbuk-do, KOREA, REPUBLIC OF;

**CONTINUING DATA**

**FOREIGN APPLICATIONS**
REPUBLIC OF KOREA 10-2006-0084538 09/04/2006

**IF REQUIRED, FOREIGN FILING LICENSE GRANTED**
09/14/2007

Foreign Priority claimed Y Yes N No
35 USC 119(a-d) conditions met Y Yes N No

STATE OR COUNTRY
KOREA, REPUBLIC OF

SHEETS DRAWINGS 6 TOTAL CLAIMS 20 INDEPENDENT CLAIMS 2

ADDRESS
SHERR & VAUGHN, PLLC
620 HERNDON PARKWAY
SUITE 200
HERNDON, VA 20170
UNITED STATES

TITLE
METHOD OF FABRICATING FLASH MEMORY DEVICE WITH INCREASED COUPLING RATIO

FILING FEE RECEIVED 1000

FEES: Authority has been given in Paper No._________ to charge/credit DEPOSIT ACCOUNT No._________ for following:

- All Fees
- 1.16 Fees (Filing)
- 1.17 Fees (Processing Ext. of time)
- 1.18 Fees (Issue)
- Other _______________
- Credit
REPLY AND AMENDMENT UNDER 37 C.F.R. § 1.111

Sir:

In response to the Non-Final Office Action mailed February 12, 2009, Applicant respectfully requests reconsideration of the application in view of the following Amendments and Remarks.

Amendments to the Drawings begins on page 2.

Amendments to the Claims are reflected in the listing of claims which begins on page 3.

Remarks begin on page 7.
AMENDMENTS TO THE DRAWINGS

Attached in the Appendix is a Replacement Sheet for figures 1a-1f, which include the changes, without makings, identified below.

Figures 1a-1f have been amended to be designated by a legend as "Related Art."
AMENDMENTS TO THE CLAIMS

Please AMEND claims 1 and 6 as shown below.

Please CANCEL claims 2 and 14 without prejudice or disclaimer.

The following is a complete list of all claims in this application

1. (Currently Amended) A method of fabricating a flash memory device comprising:
   sequentially forming a tunnel oxide film, a polysilicon film and a first insulation film for a floating gate on an active area of a semiconductor substrate;
   forming a photoresist as a mask on the first insulation film;
   performing an etching process using the photoresist as the mask;
   performing an etching process on the first insulation film;
   forming a hard mask for prevention of oxidation on the semiconductor substrate;
   forming an STI by using the hard mask;
   oxidizing sidewalls of the STI and gap-filling the STI;
   forming a the floating gate by removing the hard mask; and
   sequentially forming an ONO film and control gate on the floating gate, wherein the floating gate is larger than the tunnel oxide film in size of area, to obtain a coupling ratio between the floating gate and the control gate.

2. (Canceled).
3. (Original) The method of claim 1, wherein forming the hard mask includes depositing a second insulation film on the semiconductor substrate.

4. (Original) The method of claim 3, wherein the second insulation film prevents oxidation.

5. (Original) The method of claim 3, wherein removing the hard mask includes removing the second insulation film remaining as the hard mask.

6. (Currently Amended) The method of claim 2 claim 1, wherein the first insulation film and the polysilicon film are etched by using the photoresist as the mask.

7. (Original) The method of claim 1, wherein the tunnel oxide film has a thickness between approximately 30Å and approximately 300Å.

8. (Original) The method of claim 7, wherein the tunnel oxide film is grown.

9. (Original) The method of claim 7, wherein the tunnel oxide film is deposited.

10. (Original) The method of claim 3, wherein the first and second insulation films are formed of oxide films of SiO₂.

11. (Original) The method of claim 3, wherein the first and second insulation films are formed of nitride films of SiN.
12. (Original) The method of claim 1, wherein the sidewalls of the STI are oxidized in an oxide-oxidization method.

13. (Original) The method of claim 1, wherein the sidewalls of the STI are oxidized in an oxide-oxidization method, and then the STI is gap-filled to prevent forming voids therein.

14. (Canceled)

15. (Original) The method of claim 1, wherein the flash memory device has an ETOX (EPROM Thin Oxide) cell structure.

16. (Withdrawn) A flash memory device comprising:
   a floating gate including a tunnel oxide film and a polysilicon film on an active area of a semiconductor substrate;
   an STI wherein the sidewalls of the STI are oxidized in an oxide-oxidization method, and then the STI is gap-filled to prevent forming voids therein; and
   an ONO film and a control gate sequentially formed on the floating gate.

17. (Withdrawn) The flash memory device of claim 16, wherein the floating gate is larger than the tunnel oxide film in size of area, to obtain a coupling ratio between the floating gate and the control gate.

18. (Withdrawn) The flash memory device of claim 16, wherein the tunnel oxide film has a thickness between approximately 30Å and approximately 300Å.
19.  (Withdrawn) The flash memory device of claim 16, wherein the flash memory device has an ETOX (EPROM Thin Oxide) cell structure.

20.  (Withdrawn) The flash memory device of claim 16, wherein a top surface of the tunnel oxide film and a bottom surface of the floating gate are coplanar across substantially their entire area.
REMARKS

Claims 1, 3-13, and 15-20 are pending in the above-referenced patent application. Claims 1 and 6 are amended by way of the present amendment. Claims 2 and 14 are canceled without prejudice or disclaimer. Claims 16-20 are withdrawn from further consideration. In the Office Action: The specification was objected to, informalities. Claims 1-15 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng (U.S. Patent Publication No. 2003/0054608).

In reply to the objection to the drawings, the Applicants request reconsideration. The drawings are amended to overcome this objection. Accordingly, the Applicants respectfully request withdrawal of this objection.

In reply to the objection to the specification, the Applicants request reconsideration. The Applicants respectfully submit that the specification is adequately clear. Further, the Office Action offered no rule or statutory support for the basis of this objection. Accordingly, the Applicants respectfully request withdrawal of this objection.

In reply to the rejection to claims 1-15 under 35 U.S.C. §103(a) as being unpatentable over Tseng et al., the Applicants respectfully request reconsideration. Claims 1-15 now recite "the floating gate is larger than the tunnel oxide film in size of area, to obtain a coupling ratio between the floating gate and the control gate."
Tseng et al. relates to a method for forming shallow trench isolation in semiconductor device, as specified in the title. The Office Action asserts on page 8 that "Tseng teaches...limitations from claim 14, the method of claim 1, (see fig. 4) wherein the floating gate (width \( W_2 \)) is larger than the tunnel oxide film (width \( W_1 \) of active area, 110, below tunnel oxide film 102) in size of area, to obtain a coupling ratio between the floating gate and the control gate, pg. 2, ¶ 23-24, fig. 4..." However, the Applicants respectfully submit that Tseng et al. does not teach the above claim recitations. Tseng et al. merely discloses at Figures 3 and 4, and paragraphs [0023] and [0024] that the width "\( W_2 \)" of the silicon layer 104 is broader than the width "\( W_1 \)" of the active region 110. Tseng et al. clearly states in paragraph [0024] that "the amorphous silicon layer 104 has a width \( W_2 \) broader than the width \( W_1 \) of the active region 110." Further, as clearly shown in Figures 3 and 4 of Tseng et al., the width \( W_2 \) of the silicon layer 104 is narrower than the width of the oxide layer 102 which is located above the indication "\( W_1 \)." Accordingly, Tseng et al. does not teach the recitations in claims 1-15 of "the floating gate is larger than the tunnel oxide film in size of area, to obtain a coupling ratio between the floating gate and the control gate."

At least for these reasons, a \textit{prima facie} case of obviousness cannot be established under 35 U.S.C. §103(a), as Tseng et al. does not teach or suggest, alone or in combination, all the recitations of claims 1-15. Accordingly, the Applicants respectfully request withdrawal of the rejection of claims 1-15 under 35 U.S.C. § 103(a).
CONCLUSION

Applicant believes that a full and complete response has been made to the Office Action and respectfully submits that all of the stated objections and grounds for rejection have been overcome or rendered moot. Accordingly, Applicant respectfully submits that all pending claims are allowable and that the application is in condition for allowance.

Should the Examiner feel that there are any issues outstanding after consideration of this response, the Examiner is invited to contact the Applicant’s undersigned representative at the number below to expedite prosecution.

Prompt and favorable consideration of this Reply is respectfully requested.

Respectfully Submitted,

[Signature]

Daniel H. Sherr
Reg. No. 46,425

Sherr & Vaughn, PLLC
620 Herndon Parkway
Suite 320
Herndon, Virginia 20170
Tel: 571-313-7556
Fax: 703-935-8473

Appendix: Replacement Sheet for figures 1a-1f
Fig. 1a
Related Art

Fig. 1b
Related Art
Fig. 1c
Related Art

Fig. 1d
Related Art
Fig. 1e
Related Art

Fig. 1f
Related Art
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## Warnings:

## Information:
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.
### PATENT APPLICATION FEE DETERMINATION RECORD

**APPLICATION AS FILED – PART I**

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**MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))**

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**FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))**

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**Application Size Fee (37 CFR 1.16(e))**

**FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))**

---

Legal Instrument Examiner: CHRISTINE MOLLISSH

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-860-PTO-9199 and select option 2.
Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.
Office Action Summary

Application No. 11/849,673
Applicant(s) NAM, SANG-WOO
Examiner MICHELE FAN
Art Unit 2823

--- The MAGING DATE of this communication appears on the cover sheet with the correspondence address ---

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☑ Responsive to communication(s) filed on 14 November 2008.
2a) ☐ This action is FINAL. 2b) ☑ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☑ Claim(s) 1-20 is/are pending in the application.
   4a) Of the above claim(s) 16-20 is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☑ Claim(s) 1-15 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☑ The specification is objected to by the Examiner.
10) ☑ The drawing(s) filed on 04 September 2007 is/are: a) ☐ accepted or b) ☑ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☑ All  b) ☐ Some  * c) ☐ None of:
   1. ☑ Certified copies of the priority documents have been received.
   2. ☑ Certified copies of the priority documents have been received in Application No. _____.
   3. ☑ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsman’s Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
   Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.
DETAILED ACTION

Election/Restrictions

Claims 1-20 are pending.

Applicant’s election without traverse of claims 1-15 in the reply filed on November 14, 2008 is acknowledged.

Claims 16-20 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a non-elected invention, there being no allowable generic or linking claim.

Drawings

Figure 1a-1f should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled “Replacement Sheet” in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities:
Examiner notes it is not clear from the written disclosure how or why the decrease in the tunnel oxide width, and a corresponding increase in the floating gate width is achieved when viewing Fig. 2C and Fig. 2D. It simply states the sidewalls of the STI are oxidized and gap-filled. (See specification on pg. 6, ¶4-6, the disclosure indicates a STI is formed as shown in Fig. 2C, and the sidewalls of the STI are oxidized and gap-filled as shown in Fig. 2D.)

Appropriate correction is required.

Claim Objections

Claim 14 is objected to because of the following informalities:

The increase in coupling ratio is attributed to a larger floating gate width when compared to the width of the tunnel oxide. It is not clear from the written disclosure how or why the decrease in the tunnel oxide width, and a corresponding increase in the floating gate width is achieved when viewing Fig. 2C and Fig. 2D. (See specification on pg. 6, ¶4-6.)

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Tseng teaches:

limitations from claim 1, a method of fabricating a flash memory device comprising:

(see fig. 3) sequentially forming a tunnel oxide film (102) and a polysilicon film (104) on an active area of a semiconductor substrate (100), pg. 2, ¶19-20;
forming a hard mask (106) on the semiconductor substrate, pg. 2, ¶21;
forming an STI (108) by using the hard mask, pg. 2, ¶22;
oxidizing sidewalls of the STI (112/112a/112b) and gap-filling the STI (114), pg. 2, ¶23-25;

![Diagram of flash memory device]

(see fig. 7) forming a floating gate by removing the hard mask, pg. 2, ¶26; and sequentially forming an ONO film (118) and a control gate (120) on the floating gate (122), pg. 2, ¶127, fig. 1-7;
Tseng lacks:

- forming a first insulation film;
- performing an etching process on the first insulation film;

Tseng discloses the claimed invention except for forming a first insulation film and etching the first insulation film. It would have been obvious matter of design to form a first insulation film and etch the first insulation film, since applicant has not disclosed that the first insulation film solves any stated problems or is for any particular purpose and it appears that the invention would perform equally well with the only a single insulation film (-i.e. the applicant’s second insulation film), as disclosed by Tseng.

Examiner notes:

Tseng accomplishes the formation of a STI and a floating gate with a single insulation film rather than two insulation films (first insulation film and second insulation film of the current application).

Tseng discloses a single insulation film (-i.e. the applicant’s second insulation film) to form a STI and floating gate, where the width of the floating gate is larger than
the width of the active area (substrate with tunnel oxide) to increase the coupling ratio, as required by the applicant.

Regarding claim 2, Tseng lacks a first insulation film and a photoresist mask formed to etch the first insulation film.

limitations from claim 2, the method of claim 1, wherein performing the etching process includes forming a photoresist as a mask on the first insulation film, and performing the etching process using the photoresist as the mask.

Tseng discloses the claimed invention except for forming a first insulation film and etching the first insulation film. See explanation as applied to claim 1 above.

Tseng teaches:

limitations from claim 3, the method of claim 1, wherein forming the hard mask includes depositing a second insulation film (106, silicon nitride) on the semiconductor substrate (100), pg. 2, ¶ 21;

limitations from claim 4, the method of claim 3, wherein the second insulation film (106) prevents oxidation, pg. 2, ¶ 21;

limitations from claim 5, the method of claim 3, wherein removing the hard mask includes removing the second insulation film (106) remaining as the hard mask, pg. 2, ¶ 26;

Regarding claim 6, Tseng lacks a first insulation film and a photoresist mask formed to etch the first insulation film.
limitations from claim 6, the method of claim 2, wherein the first insulation film and the polysilicon film are etched by using the photoresist as the mask.

Tseng discloses the claimed invention except for forming a first insulation film and etching the first insulation film. See explanation as applied to claim 1 above.

Tseng teaches:

limitations from claim 7, the method of claim 1, wherein the tunnel oxide film (102) has a thickness between approximately 30 Å and approximately 300 Å (50-350 Å), pg. 2, ¶ 19;

limitations from claim 8, the method of claim 7, wherein the tunnel oxide film (102) is grown (thermal oxidation), pg. 2, ¶ 19;

limitations from claim 9, the method of claim 7, wherein the tunnel oxide film (102) is deposited (LPCVD), pg. 2, ¶ 19;

Regarding claim 10, Tseng lacks a first insulation film. Tseng discloses the claimed invention except for forming a first insulation film. See explanation as applied to claim 1 above.

limitations from claim 10, the method of claim 3, wherein the second insulation films (106) are formed of oxide films of SiO₂ (silicon nitride), pg. 2, ¶ 21;

Tseng discloses the claimed invention except for forming a second insulation film from oxide films of SiO₂. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form a second insulation film from oxide films of SiO₂, since it has been held to be within the general skill of a worker in the art to select known material on the basis of its suitability for the intended use as a matter of obvious
design choice. *In re Leshin*, 125 USPQ 416. See MPEP § 2144.07, Art Recognized Suitability for an Intended Purpose.

Regarding claim 11, Tseng lacks a first insulation film. *Tseng* discloses the claimed invention except for forming a first insulation film. See explanation as applied to claim 1 above.

limitations from claim 11, the method of claim 3, wherein and second insulation films are formed of nitride films of SiN (silicon nitride), pg. 2, ¶ 21;

Tseng teaches:

limitations from claim 12, the method of claim 1, wherein the sidewalls of the STI are oxidized (112/112a/112b) in an oxide-oxidization method, pg. 2, ¶ 23, fig. 3;

limitations from claim 13, the method of claim 1, wherein the sidewalls of the STI are oxidized in an oxide-oxidization method (112/112a/112b), and then the STI is gap-filled (114/116) to prevent forming voids therein, pg. 2, ¶ 23-26, fig. 3;

limitations from claim 14, the method of claim 1, (see fig. 4) wherein the floating gate (width W₂) is larger than the tunnel oxide film (width W₁ of active area, 110, below tunnel oxide film 102) in size of area, to obtain a coupling ratio between the floating gate and the control gate, pg. 2, ¶ 23-24, fig. 4;
limitations from claim 15, the method of claim 1, wherein the flash memory device has an ETOX (EPROM Thin Oxide) cell structure, pg. 1, ¶ 2, pg. 2, ¶ 27; fig. 7. (A memory device is formed comprising a control gate stacked over a floating gate (cell structure).)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHELE FAN whose telephone number is (571)270-7401. The examiner can normally be reached on M-F from 8 am to 4 pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for
published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/W. David Coleman/
Primary Examiner, Art Unit 2823

9 February 2009

/M. F./
Examiner, Art Unit 2823
**Notice of References Cited**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Sang-Woo Nam
Application No.: 11/849,673
Docket No.: 604-0075
Confirmation No.: 6118
Filed: September 4, 2007
Group Art Unit: 2826
Examiner: Mandala, Victor A

For: METHOD OF FABRICATING FLASH MEMORY DEVICE

Commissioner for Patents
P.O. BOX 1450
Alexandria, VA 22313-1450

REPLY TO RESTRICTION REQUIREMENT

Sir:

In response to the Restriction Requirement mailed October 17, 2008, Applicant elects Group II (Method claims 1-15), without traverse.

It is not believed that any extensions of time or fees are required. If extensions of time are necessary to prevent abandonment of this application, such extensions of time are hereby petitioned for under 37 C.F.R. §1.136(a).

Respectfully Submitted,

[Signature]

Daniel H. Sherr
Reg. No. 46,425

Sherr & Vaughn, PLLC
620 Herndon Parkway
Suite 320
Herndon, Virginia 20170
Tel: 571-313-7556
Fax: 703-935-8473
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## Information:
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**New Applications Under 35 U.S.C. 111**
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.
Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.
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--- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If no period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1. [X] Responsive to communication(s) filed on 04 September 2007.
2. [ ] This action is FINAL.
2. [ ] This action is non-final.
3. [ ] Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

4. [X] Claim(s) 1-20 is/are pending in the application.
   4a. Of the above claim(s) _____ is/are withdrawn from consideration.
5. [ ] Claim(s) _____ is/are allowed.
6. [ ] Claim(s) _____ is/are rejected.
7. [ ] Claim(s) _____ is/are objected to.
8. [ ] Claim(s) 1-20 are subject to restriction and/or election requirement.

## Application Papers

9. [ ] The specification is objected to by the Examiner.
10. [ ] The drawing(s) filed on _____ is/are: a) [ ] accepted or b) [ ] objected to by the Examiner.
    
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11. [ ] The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

12. [ ] Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) [ ] All  b) [ ] Some * c) [ ] None of:
   1. [ ] Certified copies of the priority documents have been received.
   2. [ ] Certified copies of the priority documents have been received in Application No. _____.
   3. [ ] Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

1. [ ] Notice of References Cited (PTO-892)
2. [ ] Notice of Draftsman’s Patent Drawing Review (PTO-948)
3. [ ] Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date ______.
4. [ ] Interview Summary (PTO-413) Paper No(s)/Mail Date ______.
5. [ ] Notice of Informal Patent Application
6. [ ] Other; ______.

U.S. Patent and Trademark Office
PTOL-326 (Rev. 08-06)
Office Action Summary
Part of Paper No./Mail Date 20081014
DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 16-20 are drawn to a flash memory device, classified in class 257, subclass 314.

   II. Claims 1-14 are drawn to a method of fabricating a flash memory device, classified in class 438, subclass 201.

   The inventions are distinct, each from the other because of the following reasons:

2. Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the device is made by selectively etching the device, but the device could be made by selectively depositing the device.

3. Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and examination burden if restriction were not required because one or more of the following reasons apply:

   (a) the inventions have acquired a separate status in the art in view of their different classification;
(b) the inventions have acquired a separate status in the art due to their recognized
divergent subject matter;

(c) the inventions require a different field of search (for example, searching different
classes/subclasses or electronic resources, or employing different search queries);

(d) the prior art applicable to one invention would not likely be applicable to another
invention;

(e) the inventions are likely to raise different non-prior art issues under 35 U.S.C. 101
and/or 35 U.S.C. 112, first paragraph.

Applicant is advised that the reply to this requirement to be complete must include

(i) an election of a invention to be examined even though the requirement may be traversed (37
CFR 1.143) and (ii) identification of the claims encompassing the elected invention.

The election of an invention may be made with or without traverse. To reserve a right to
petition, the election must be made with traverse. If the reply does not distinctly and specifically
point out supposed errors in the restriction requirement, the election shall be treated as an
election without traverse. Traversal must be presented at the time of election in order to be
considered timely. Failure to timely traverse the requirement will result in the loss of right to
petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate
which of these claims are readable on the elected invention.

If claims are added after the election, applicant must indicate which of these claims are
readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct,
aplicant should submit evidence or identify such evidence now of record showing the
inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

4. The examiner has required restriction between product and process claims. Where applicant elects claims directed to the product, and the product claims are subsequently found allowable, withdrawn process claims that depend from or otherwise require all the limitations of the allowable product claim will be considered for rejoinder. All claims directed to a nonelected process invention must require all the limitations of an allowable product claim for that process invention to be rejoined.

In the event of rejoinder, the requirement for restriction between the product claims and the rejoined process claims will be withdrawn, and the rejoined process claims will be fully examined for patentability in accordance with 37 CFR 1.104. Thus, to be allowable, the rejoined claims must meet all criteria for patentability including the requirements of 35 U.S.C. 101, 102, 103 and 112. Until all claims to the elected product are found allowable, an otherwise proper restriction requirement between product claims and process claims may be maintained. Withdrawn process claims that are not commensurate in scope with an allowable product claim will not be rejoined. See MPEP § 821.04(b). Additionally, in order to retain the right to rejoinder in accordance with the above policy, applicant is advised that the process claims should be amended during prosecution to require the limitations of the product claims. **Failure to do so may result in a loss of the right to rejoinder.** Further, note that the prohibition against double patenting rejections of 35 U.S.C. 121 does not apply where the restriction requirement is withdrawn by the examiner before the patent issues. See MPEP § 804.01.
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to VICTOR A. MANDALA whose telephone number is (571)272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/VICTOR A MANDALA JR/
Examiner, Art Unit 2826
10/14/08
## Index of Claims

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- **Rejected**
- **Cancelled**
- **Restricted**
- **Non-Elected**
- **Interference**
- **Appeal**
- **Objected**
APPLICATION NUMBER | FILING OR 371(c) DATE | FIRST NAMED APPLICANT | ATTY. DOCKET NO./TITLE
---|---|---|---
11/849,673 | 09/04/2007 | Sang-Woo Nam | 604-0075

CONFIRMATION NO. 6118

60803
SHERR & NOURSE, PLLC
620 HERNDON PARKWAY
SUITE 200
HERNDON, VA20170

Title: METHOD OF FABRICATING FLASH MEMORY DEVICE

Publication Date: 03/06/2008

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Pre-Grant Publication Division, 703-605-4283
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Docket No.: 604-0075
Sang-Woo NAM Confirmation No.: 6118
Application No.: 11/849,673 Group Art Unit: 2812
Filed: September 4, 2007 Examiner:

For: METHOD OF FABRICATING FLASH MEMORY DEVICE

Commissioner for Patents
P.O. BOX 1450
Alexandria, VA 22313-1450

CLAIM FOR PRIORITY UNDER 35 USC §119

Sir:

Priority under 35 U.S.C. § 119 is hereby claimed to the following priority document(s), filed in a foreign country within twelve (12) months prior to the filing of the above-referenced United States utility patent application:

<table>
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<td>KOREA</td>
<td>10-2006-0084538</td>
<td>September 4, 2006</td>
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A certified copy of the above listed application is attached. Prompt acknowledgment of the aforementioned claim is respectfully requested.

Respectfully Submitted,

Daniel H. Sherr
Reg. No. 46,425

Sherr & Nourse, PLLC
620 Herndon Parkway
Suite 200
Herndon, Virginia 20170
Tel: 703-673-1141
Fax: 703-935-8473
This is to certify that the following application annexed hereto is a true copy from the records of the Korean Intellectual Property Office.

Application Number: 10-2006-0084538
Filing Date: SEP 04, 2006
Applicant(s): Dongbu Electronics Co., Ltd.

2007년 06월 25일

Issue Date: 2007.06.25
【서지사항】
【서류명】 특허출원서
【권리구분】 특허
【수신처】 특허청장
【제출일자】 2006.09.04
【발명의 국내명칭】 ETOX 셀 플래시 메모리의 자기정렬 STI 및 플로팅 게이트 제조 방법
【발명의 영문명칭】 Method of Fabricating a Self-Aligned STI and Floating Gate a ETOX Cell Flash Memory Device

【출원인】
【명칭】 동부알렉트로닉스 주식회사
【출원인코드】 1-1998-002671-9

【대리인】
【성명】 남희섭
【대리인코드】 9-1999-000451-4
【포괄위임등록번호】 2004-071223-9

【대리인】
【성명】 정승훈
【대리인코드】 9-2002-000245-5
【포괄위임등록번호】 2004-071226-1

【발명자】
【성명】 남상우
【성명의 영문표기】 NAM, Sang Woo
【주민등록번호】 691007-1XXXXXXX
【우편번호】 361-240
【주소】 충북 청주시 흉덕구 개신동 개신주공아파트 210-203
【국적】 KR
【심사청구】 청구
【취지】 특허법 제42조의 규정에 의한 출원, 특허법 제60조의 규정에 의한 출원심사를 청구합니다.

대리인

남희섭 (인)

대리인

정승훈 (인)

【수수료】

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【요약서】

【요약】

본 발명은 반도체 기판상의 활성 영역 위에 터널 산화막(tunnel oxide)과, 플로팅 게이트의 폴리(Poly) 실리콘막과, 질화막과, 포토 레지스트(Photo Resist)로 마스크를 형성한 후 식각하는 단계; 활성 영역의 산화시 상기 플로팅 게이트가 산화되는 것을 차단하도록 산화 방지용 질화막을 증착시켜 하드 마스크를 형성하는 단계; 하드 마스크를 이용하여 STI를 형성하고 STI측벽을 산화시킴과 동시에 STI 절편(Gap Fill)을 형성하여 STI 마스크를 제조하는 단계; 하드 마스크로 있던 상기 질화막을 제거하여 플로팅 게이트를 형성하는 단계; 및 상기 플로팅 게이트 상에 ONO와 컨트롤 게이트를 순차적으로 형성하는 단계를 포함하는 ETOX 셀 플래시 메모리의 자기정렬 STI 및 플로팅 게이트 제조 방법에 관한 것이다.

【대표도】

도 2d

【색인어】

ETOX, 플래시 메모리, 자기정렬, STI, 플로팅 게이트, 컨트롤 게이트, 커플링 비율
【명세서】

【발명의 명칭】

ETOX 셀 플래시 메모리의 자기경렬 STI 및 플로팅 게이트 제조 방법

{Method of Fabricating a Self-Aligned STI and Floating Gate a ETOX Cell Flash Memory Device}

【도면의 간단한 설명】

<1> 도 1a 내지 도 1f는 동래 기술에 의한 ETOX 셀 플래시 메모리의 자기경렬 STI 및 플로팅 게이트를 제조하는 과정을 나타낸 도면.

<2> 도 2a 내지 도 2f는 본 발명에 의한 ETOX 셀 플래시 메모리의 자기경렬 STI 및 플로팅 게이트를 제조하는 과정을 나타낸 도면.

<3> <도면의 주요 부분에 관한 부호의 설명>

<4> 100 : 반도체 기판 110 : 터널 산화막

<5> 120 : 폴리 실리콘막 130 : 절화막

<6> 140 : 마스크 150 : 산화 방지용 절화막

<7> 160 : STI 170 : STI 갤필

<8> 180 : 플로팅 게이트 190 : ONO

<9> 200 : 컨트롤 게이트

【발명의 상세한 설명】

【발명의 목적】
【발명이 속하는 기술분야 및 그 분야의 종래기술】

본 발명은 플래시 메모리 제조 방법에 관한 것으로서, 특히 플래시 메모리의 ETOX(EPROM Thin OXide) 셀내 플로팅 게이트와 컨트롤 게이트간의 커플링 비율 (coupling ratio)을 증가시킬 수 있는 ETOX 셀 플래시 메모리의 자기정렬 STI 및 플로팅 게이트 제조 방법에 관한 것이다.

일반적으로 플래시 메모리는 전원이 중단되어도 저장된 데이터가 손실되지 않는 장점을 가지고 있어 PC Bios용, Set-top Box, 프린터 및 네트워크 서버 등의 데이터 저장용으로 많이 사용되고 있으며 최근에는 디지털 카메라와 휴대폰 등에서도 많이 이용되고 있는 실정이다.

이러한 플래시 메모리 중에서도 전기적으로 메모리 셀의 데이터를 일괄적으로 또는 섹터 단위로 소거하는 기능을 가지고 있는 EEPROM(Electrically Erasable Programmable Read-Only Memory)형 플래시 메모리장치는 프로그램시 드레인 측에 채널 열 전자(channel hot electron)를 형성시켜 전자를 플로팅 게이트(floating gate)에 축적함으로써 셀 트랜지스터의 문턱 전압을 증가시킨다.

반면에, 플래시 메모리장치의 소거 동작은 소오스/기판과 플로팅 게이트간에 고전압을 발생시켜 플로팅 게이트에 축적된 전자를 방출함으로써 셀 트랜지스터의 문턱 전압을 낮춘다.

한편 EEPROM형 플래시 메모리장치의 대표적인 셀 구조로는 단순 적층(stack) 구조의 ETOX(EPROM Thin OXide)셀과, 1셀당 2개 트랜지스터로 이루어진 스플리트
게이트(splite gate)형 셀로 구분된다. ETOX 셀 구조는 게이트를 구성하는 전하 저
장용 플로팅 게이트(floating gate) 및 구동 전원이 인가되는 컨트롤 게이트
(control gate)가 적층된 구조인데 반하여, 스플리트 게이트형 셀 구조는 선택 트랜지스터와 셀 트랜지스터 2개를 하나의 컨트롤 게이트를 이용하여 컨트롤 게이트
의 일부가 플로팅 게이트와 오버랩(overlap)되고 컨트롤 게이트의 다른 부분이 기
판 표면에 수평으로 배치된 구조이다.

도 1a 내지 도 1f는 중래 기술에 의한 ETOX 셀 플래시 메모리의 자기정렬
STI 및 플로팅 게이트를 제조하는 과정을 나타낸 도면이다.

도 1a 내지 도 1f를 참조하면, 먼저, 도 1a에 도시된 바와 같이 반도체 기판
(1)의 활성 영역 위에 터널 산화막(tunnel oxide)(2)과, 그 위에 플로팅 게이트의
1차 폴리(Poly) 실리콘막(3)을 형성한 후, 하드 마스크(Hard Mask)로 질화막(산화
막)(4)을 형성한 다음 포토 레지스트(Photo Resist)로 마스크(5)를 형성한다. 그런
다음 도 1b에 도시된 바와 같이 포토 레지스트 마스크를 이용하여 하드 마스크를
형성해서 STI(6)를 형성하여 STI 마스크를 제작한다.

STI 마스크를 제작이 완료되면, 도 1c에 도시된 바와 같이 절연(Isolation)
을 형성하기 위해 절연막으로 갭필(Gap Fill)(7)을 실시하고, 하드 마스크인 절연
막(4)을 제거하여 1차 폴로팅 케이트를 형성한다.

그런 다음, 도 1d에 도시된 바와 같이 2차 폴로팅 케이트용 2차 폴리(Poly)
실리콘막(8)을 형성하고, 포토 레지스트 마스크(9)를 만든 후, 도 1e에 도시된 바
와 같이 폴리 식각(Poly Etch)을 하여 2차 폴로팅 케이트(10)를 형성한다.
그리고, 도 1f에 도시된 바와 같이 2차 플로팅 게이트 상에 ONO(11)를 형성하고, 컨트롤 게이트(12)를 형성하여 스테크 게이트를 최종 완성한다.

그러나, 상기와 같은 자기정렬 STI형성 방법을 통한 플로팅 게이트를 형성하는 기술은 STI형성시 사용한 1폴리 실리콘막으로는 커플링비율(CR : Coupling Ratio)을 크게 할 수 없어서 2폴리 실리콘막을 이용하여 플로팅 게이트를 형성하는 데, 이로 인해 플로팅 게이트를 형성하는 마스크가 추가로 필요하여 제조비용이 높고, 향후 디자인의 축소시 오버레이 마진(Overlay Margin)이 점점 부족해져서 물리적인 한계에 봉착하는 문제점이 있었다.

【발명이 이루고자 하는 기술적 과제】

본 발명의 목적은 상기와 같은 종래 기술의 문제점을 해결하기 위하여 STI와 플로팅 게이트의 형성을 1개의 마스크만을 가지고 한번에 자기정렬 방식으로 형성함으로써 마스크 사용을 절감하여 제조 원가 비용을 절감할 수 있고, 공정 재작업율을 없앨 수 있으며, 오버레이 마진을 해결할 수 있도록 하는 ETOX 셀 플래시 메모리의 자기정렬 STI 및 플로팅 게이트 제조 방법을 제공하는 데 있다.

또한, 본 발명의 다른 목적은 또한 필드 형성시 셀필을 하지 않고 산화막을 형성하여 필드를 형성시 셀필과 CMP(Chemical Mechanical Polishing)공정이 불필요하도록 함으로써 아주 단순한 공정을 제공할 수 있는 ETOX 셀 플래시 메모리의 자기정렬 STI 및 플로팅 게이트 제조 방법을 제공하는 데 있다.
【발명의 구성】

상기와 같은 목적을 달성하기 위한 본 발명은, 반도체 기판상의 활성 영역 위에 터널 산화막(tunnel oxide)과, 플로팅 게이트의 폴리(Poly) 실리콘막과, 절화막과, 포토 레지스트(Photo Resist)로 마스크를 형성한 후 식각하는 단계; 활성 영역의 산화시 상기 플로팅 게이트가 산화되는 것을 차단하도록 산화 방지용 절화막을 중착시켜 하드 마스크를 형성하는 단계; 하드 마스크를 이용하여 STI를 형성하고 STI측벽을 산화시킴과 동시에 STI 젤필(Gap Fill)을 형성하여 STI 마스크를 제조하는 단계; 하드 마스크를 이용한 상기 절화막을 제거하여 플로팅 게이트를 형성하는 단계; 및 상기 플로팅 게이트 상에 ONO와 컨트롤 게이트를 순차적으로 형성하는 단계를 포함하는 ETOX 셀 플래시 메모리의 자기정렬 STI 및 플로팅 게이트 제조 방 법에 관한 것이다.

본 발명에서 상기 STI 젤필은 공간(void)이 미형성되는 것을 특징으로 한다.

이하, 첨부된 도면을 참조하여 본 발명의 실시예를 상세하게 설명한다.

본 발명이 속하는 기술 분야에 의한 알려져 있고 본 발명과 직접적으로 관련이 없는 기술 내용에 대해서는 설명을 생략한다. 이는 불필요한 설명을 생략함으로써 본 발명의 요지를 흐리지 않고 더욱 명확히 전달하기 위함이다.

도 2a 내지 도 2f는 본 발명에 의한 ETOX 셀 플래시 메모리의 자기정렬 STI 및 플로팅 게이트를 제조하는 과정을 나타낸 도면이다.

먼저, 도 2a에 도시된 바와 같이 반도체 기판(100)상의 활성 영역(active
area) 위에 터널 산화막(tunnel oxide)(110)과, 플로팅 게이트의 폴리(Poly) 실리콘막(120) 및 결화막(130)을 순차적으로 형성한 후, 포토 레지스트(Photo Resist)로 마스크(140)를 형성한 후 식각공정을 수행하여 식각한다. 여기서, 터널 산화막(110)은 SiO2, SiON, La2O3, ZrO2 또는 Al2O3 막, 또는 이들 중 적어도 두 개의 적층막으로 30Å~300Å 범위에서 성장 내지는 중착하여 형성할 수 있고, 폴리 실리콘막(120)으로는 플로팅 게이트 형성을 위해 폴리 실리콘(poly-silicon)을 통상의 LP-CVD(Low Pressure-Chemical Vapor Deposition)방법을 사용하여 100 내지 1500Å 범위에서 중착하는 것이 바람직하다. 또한, 결화막(130)은 SiO2의 산화막 또는 SiN의 결화막으로 형성될 수 있다. 또, 결화막(130) 상에 소스/드레인 영역을 정의하기 위한 포토레지스트 패턴을 이용하는 식각공정을 수행하여 반도체 기판(100) 상의 터널 산화막(110)까지 제거함으로써 반도체 기판(100)을 노출한 후, 소스/드레인 영역(도시하지 않음)을 형성하기 위한 도편트를 주입(implantation)할 수 있다.

이러한 포토레지스트 패턴을 이용하는 식각공정에 따라 터널 산화막(110)까지 제거하지 않고 폴리 실리콘막(120)까지 식각공정을 수행하여 터널 산화막(110)을 노출시킬 수 있다.

<29>
이어서, 도 2b에 도시된 바와 같이 활성 영역의 산화시 폴로팅 게이트가 산화되는 것을 차단하도록 산화 방지용 결화막(150)을 중착시켜 하드 마스크를 형성한다. 여기서, 산화 방지용 결화막(150)은 SiO2의 산화막 또는 SiN의 결화막으로 형성될 수 있다.

<30>
이와 같이 산화 방지용 결화막(150)의 중착을 수행한 후 도 2c에 도시된 바
와 같이 하드 마스크(Hard Mask)를 이용하여 실리콘 기판(110)을 일정 깊이로 식각
공정을 수행하여 STI(160)를 형성한 후, 도 2d에 도시된 바와 같이 산화물(Oxide)
산화 방식을 이용하여 STI(160)층벽을 산화시킴과 동시에 STI 캐필(Gap Fill)(170)
을 형성하여 STI 마스크를 제조하는 데, 이때, STI 캐필(170)에는 STI(160)층벽
을 산화물(Oxide) 산화 방식으로 산화시키기 때문에 틈공간(void)이 미형성된다.

STI 마스크를 제조가 완료되면, 도 2e에 도시된 바와 같이 하드 마스크로 있던 절화막(130)을 제거하여 폴로팅 게이트(180)를 형성한다.

그리고, 도 2f에 도시된 바와 같이 폴로팅 게이트(180) 상에 ONO(190)와 컨트롤 게이트(200)를 순차적으로 형성하는 데, 커플링 비율을 확보할 수 있도록 터널 산화막(110)보다 폴로팅 게이트(190)의 면적을 최대화하는 형상을 만든다. 여기서, 콘트롤 게이트(200)의 재질은 폴리 실리콘, 탱스텐(W), 실리콘게르마늄(SiGe), 실리콘게르마늄카바이드(SiGeC), 물리브텐(Mo), 물리브텐실리사이드(MoSi2), 티타늄(Ti), 티타늄실리사이드(TiSi2) 및 티타늄나이트라이트(TiN) 중 선택된 적어도
하나의 재질을 이용하는 것이 바람직하다.

이와 같이 본 발명의 실시예에 따라 폴로팅 게이트와 터널 산화막간의 미스
얼라인(Misalign)이 발생하는 것을 방지할 수 있고, STI와 폴로팅 게이트를 1개의
마스크만을 사용해서 만들 수 있으며, 터널 산화막보다 넓은 면적의 폴로팅 게이트
를 확보할 수 있어서 큰 커플링 비율을 확보할 수 있고, STI 캐필을 산화물 산화
방식으로 형성하기 때문에 틈공간이 발생하는 것을 차단할 수 있으며, STI CMP 공
정이 배제되기 때문에 공정을 단순화시킬 수 있다.
본 발명의 기술사항은 상기 바람직한 실시예에 따라 구체적으로 기술되었으나, 전술한 실시예들의 그 설명을 위한 것이며, 그 제한을 위한 것이 아니며 주의하여야 한다.

또한, 본 발명의 기술분야의 통상의 전문가라면 본 발명의 기술사항의 범위 내에서 다양한 실시가 가능할을 이해할 수 있을 것이다.

【발명의 효과】

상기한 바와 같이 본 발명인 ETOX 셀 플래시 메모리의 자기정렬 STI 및 플로팅 게이트 제조 방법에 따르면 플래시 메모리의 ETOX(EPROM Thin OXide) 셀내 플로팅 게이트와 컨트롤 게이트간의 커플링 비율(coupling ratio)을 증가시킬 수 있다.
【특허청구범위】

【청구항 1】
반도체 기판상의 활성 영역 위에 터널 산화막(tunnel oxide)과, 플로팅 게이트의 폴리(Poly) 실리콘막과, 질화막과, 포토 레지스트(Photo Resist)로 마스크를 형성한 후 식각하는 단계;

활성 영역의 산화시 상기 플로팅 게이트가 산화되는 것을 차단하도록 산화 방지용 질화막을 증착시켜 하드 마스크를 형성하는 단계;

하드 마스크로 인해 상기 질화막을 제거하여 플로팅 게이트를 형성하는 단계; 및

상기 플로팅 게이트 상에 ONO와 컨트롤 게이트를 순차적으로 형성하는 단계

를 포함하는 ETOX 셀 플래시 메모리의 자기정렬 STI 및 플로팅 게이트 제조 방법.

【청구항 2】
제 1 항에 있어서,

상기 STI 마스크를 제조하는 단계에서,

산화물(Oxide) 산화 방식을 이용하여 STI측벽을 산화시킴과 동시에 STI 깽필(Gap Fill)을 형성하는 것을 특징으로 하는 ETOX 셀 플래시 메모리의 자기정렬 STI
및 풀로팅 게이트 제조 방법.

【청구항 3】

제 2 항에 있어서,

상기 STI 절편은,

빈공간(void)이 미형성되는 것을 특징으로 하는 ETOX 셀 플래시 메모리의 자기정렬 STI 및 풀로팅 게이트 제조 방법.

【청구항 4】

제 1 항에 있어서,

상기 풀로팅 게이트 상에 ONO와 컨트롤 게이트를 형성하는 단계에서,

커플링 비율을 확보할 수 있도록 상기 터널 산화막(tunnel oxide)보다 풀로팅 게이트를 더 넓은 면적으로 형성하는 것을 특징으로 하는 ETOX 셀 플래시 메모리의 자기정렬 STI 및 풀로팅 게이트 제조 방법.
[도면]

【도 1a】

【도 1b】
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CONFIRMATION NO. 6118

FILING RECEIPT

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Date Mailed: 09/14/2007

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections.

Applicant(s)  
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Power of Attorney: None

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Foreign Applications  
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Non-Publication Request: No

Early Publication Request: No

Title

METHOD OF FABRICATING FLASH MEMORY DEVICE

Preliminary Class
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DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION
(37 CFR 1.63)

X Declaration Submitted With Initial Filing

Attorney Docket Number 904-0075

First Named Inventor Bang-Woo NAM

Application Number COMPLETE IF KNOWN

Filing Date September 4, 2007

Art Unit TBA

Examiner Name TBA

I hereby declare that:

Each inventor’s residence, mailing address, and citizenship are as stated below next to their name.

I believe the inventor(s) named below to be the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD OF FABRICATING FLASH MEMORY DEVICE

(Title of the Invention)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (e), or 365(b) of any foreign application(s) for patent, inventor’s or plant breeder’s rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent, inventor’s or plant breeder’s rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)

Country

Foreign Filing Date

Priority

Certified Copy Attached?

10-2006-000453B

KOREA

September 4, 2006

Not Claimed

YES

Additional foreign application numbers are listed on a supplemental priority data sheet FTOSN00188 attached hereto.
DECLARATION — Utility or Design Patent Application

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

NAME OF SOLE OR FIRST INVENTOR: [ ] A petition has been filed for this unsigned inventor

Given Name (first and middle if any) Family Name or Surname
Sang-Woo NAM

Inventor's Signature: Sang-Woo NAM Date: Sep 7, 2009

Residence: City State Country Citizenship
Chungcheongbuk-do Republic of Korea Korean

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City State Zip Country
Chungcheongbuk-do Republic of Korea

[ ] Additional inventors or a legal representative are being named on the supplemental sheet(s) PTO/SB/20A or OBLR attached hereto.
METHOD OF FABRICATING FLASH MEMORY DEVICE


BACKGROUND

Generally, flash memory devices are advantageous in that stored data is not lost even when its power supply is stopped. For this reason, flash memory devices are widely used for data storage of a PC BIOS, a set-top box, a printer and a network server. Recently, flash memory devices have also been used in digital cameras and mobile phones.

Among the different types of flash memory devices, an EEPROM (Electrically Erasable Programmable Read-Only Memory) type flash memory device may completely erase data from memory cells, or may erase data from memory cells by each unit sector.

In such an EEPROM type flash memory device, when in a programming mode, a channel hot electron is generated at a drain side, and the channel hot electron is stored in a floating gate, whereby a threshold voltage of the cell transistor increases.

Alternatively, when in an erasing mode of this EEPROM type flash memory device, a high voltage is generated between the floating gate and source/substrate, and the channel hot electron stored in the floating gate is discharged, thereby lowering the threshold voltage of the cell transistor.
The EEPROM type flash memory device may have an ETOX (EPROM Thin Oxide) cell or a split gate type cell. At this time, the ETOX cell is formed as a simple stack structure. In case of the split gate type cell, two transistors are formed in each cell. Specifically, in case of the ETOX cell, one memory cell has the stack structure of a floating gate and a control gate, wherein the floating gate stores charges therein, and the control gate receives a driving power.

Meanwhile, the split gate type cell is comprised of the two transistors, that is, a selection transistor and a cell transistor. Both the selection and cell transistors use one control gate, wherein some of the control gate is overlapped with the floating gate and the other is positioned in parallel to the surface of substrate.

Example FIGs. 1A to 1F are cross section views to illustrate a method of fabricating a self-alignment STI and a floating gate in a flash memory, which illustrate an ETOX cell-structure flash memory.

First, as shown in example FIG. 1A, a tunnel oxide film 2 is formed on an active area of a semiconductor substrate 1, and a first polysilicon film 3 for a floating gate is formed on the tunnel oxide film 2. After that, a nitride film (or oxide film) 4 is formed on the first polysilicon film 3, wherein the nitride film 4 functions as a hard mask. Then, a photoresist 5 which serves as a mask is formed on the nitride film 4.

Referring to example FIG. 1B, a STI (Shallow Trench Isolation) 6 is formed by using the photoresist 5 as the mask.

As shown in example FIG. 1C, the STI 6 is gap-filled with an insulation material, thereby forming an insulation film 7. After that, a first floating gate is formed by removing the nitride film 4 of the hard mask.
Thereon, a second polysilicon film 8 for a second floating gate is formed as shown in example FIG. 1D, and a photoresist mask 9 is formed on the second polysilicon film 8.

After that, the second polysilicon film 8 is etched by using the photoresist mask 9, to thereby form a second floating gate 10 as shown in example FIG. 1E.

As shown in example FIG. 1F, an ONO film 11 is formed on the second floating gate 10, and a control gate 12 is formed on the ONO film 11. Through these steps, a gate stack is completed.

However, when forming the floating gate of the device having the aforementioned self-alignment STI, it is impossible to realize a large coupling ratio (CR) with the first polysilicon film 3 used when forming the STI. Accordingly, use of the second polysilicon film 8 is required to form the floating gate. That is, there is a requirement for the additional mask to form the floating gate, whereby the fabrication cost and complexity increase. Furthermore, as design sizes are reduced it may be physically impossible to achieve the necessary overlay margins between the films.

**SUMMARY**

Embodiments relate to a flash memory device that includes a floating gate including a tunnel oxide film and a polysilicon film on an active area of a semiconductor substrate; an STI wherein the sidewalls of the STI are oxidized in an oxide-oxidization method, and then the STI is gap-filled to prevent forming voids therein; and an ONO film and a control gate sequentially formed on the floating gate.
Embodiments relate to a method of fabricating a flash memory device comprising: sequentially forming a tunnel oxide film, a polysilicon film and a first insulation film on an active area of a semiconductor substrate; performing an etching process on the first insulation film; forming a hard mask on the semiconductor substrate; forming an STI by using the hard mask; oxidizing sidewalls of the STI and gap-filling the STI; forming a floating gate by removing the hard mask; and sequentially forming an ONO film and a control gate on the floating gate.

DRAWINGS

Example FIGs. 1A to 1F are cross section views to illustrate a method of forming a self-alignment STI and a floating gate in a flash memory device.

Example FIGs. 2A to 2F are cross section views to illustrate a method of forming a self-alignment STI and a floating gate in a flash memory device according to embodiments described herein.

DESCRIPTION

Hereinafter, a method of fabricating a flash memory device according to the embodiments will be described with reference to the accompanying drawings.

Example FIGs. 2A to 2F are cross section views to illustrate a method of forming a self-alignment STI and a floating gate in a flash memory device according to the embodiments described herein, which illustrate an ETOX cell-structure flash memory device.
First, as shown in example FIG. 2A, a tunnel oxide film 110 is formed on an active area of a semiconductor substrate 100. Then, a polysilicon film 120 and an insulation film 130 for a floating gate are sequentially formed on the tunnel oxide film 110.

Then, a photoresist 140 which serves as a mask is formed on the insulation film 130, and an etching process is applied thereto.

At this time, the tunnel oxide film 110 may be formed of SiO₂, SiON, La₂O₃, ZrO₂ or Al₂O₃, or may be formed of a stack structure inclusive of at least two of the aforementioned oxides. Also, the tunnel oxide film 110 may be formed at a thickness between approximately 30Å and approximately 300Å by growing or deposition.

The polysilicon film 120 is for formation of the floating gate. The polysilicon film 120 is deposited at a thickness between approximately 100Å and approximately 1500Å by LPCVD (Low Pressure Chemical Vapor Deposition).

The insulation film 130 may be formed of an oxide film of SiO₂ or a nitride film of SiN.

An etching process is applied to the insulation film 130 by using a photoresist pattern, to thereby define source and drain regions. This etching process is performed until the tunnel oxide film 110 on the semiconductor substrate 100 is removed, to thereby expose the semiconductor substrate 100.

At this time, a dopant is implanted into the defined source and drain regions, thereby forming source and drain regions (not shown).
As an additional example, the tunnel oxide film 110 may be exposed by the etching process to the polysilicon film 120, instead of the etching process to the tunnel oxide film 110 using the photoresist pattern.

As shown in example FIG. 2B, an oxidizing-prevention insulation film 150 is deposited to prevent the floating gate from being oxidized during the oxidation process for the active area. After that, a hard mask is formed from the oxidizing-prevention insulation film 150; this hard mask is formed with the oxidizing-prevention insulation film 150 remaining at the lateral side of stack structure inclusive of the polysilicon film 120 and the insulation film 130.

The oxidizing-prevention insulation film 150 may be formed of an oxide film of SiO₂ or a nitride film of SiN.

After depositing the oxidizing-prevention insulation film 150, the silicon substrate is etched to a predetermined depth by using the hard mask. Through this etching process, an STI 160 is formed as shown in example FIG. 2C.

As shown in example FIG. 2D, the sidewalls of STI 160 are oxidized in an oxide-oxidization method. At this same time, the STI 160 is gap-filled, thereby completing an STI mask.

Since the sidewalls of STI 160 are oxidized in the oxide-oxidization method before the gap-filling for the STI, there are no voids.

After completing the STI mask, as shown in example FIG. 2E, the insulation film 130 which serves as the hard mask is removed, thereby forming a floating gate 180.

As shown in example FIG. 2F, an ONO film 200 and a control gate 190 are sequentially formed on the floating gate 180. To obtain a coupling ratio between the
floating gate 180 and the control gate 190 in a cell, the floating gate 180 is larger than the tunnel oxide film 110 in size. For example, the area of floating gate 180 is maximized as compared with the area of tunnel oxide film 110.

Preferably, the control gate 190 may be formed of at least any one among polysilicon, tungsten (W), silicon germanium (SiGe), silicon germanium carbide (SiGeC), molybdenum (Mo), molybdenum silicide (MoSi2), titanium (Ti), titanium silicide (TiSi2) and titanium nitride (TiN).

The embodiments can prevent misalignment between the floating gate and the tunnel oxide film. Also, the STI and the floating gate can be formed with one mask.

In the embodiments, the floating gate 180 is larger than the tunnel oxide film 110, thereby obtaining the large coupling ratio.

Because the STI gap-filling is realized in the oxide-oxidization method, the forming of voids is prevented. Furthermore, since there is no STI CMP process, the embodiments result in a simplified process.

As mentioned above, the method of fabricating the flash memory device as described has the following advantage: the coupling ratio is increased between the floating gate and the control gate in the ETOX (EPROM Thin Oxide) cell of the flash memory device.

Also, the STI and the floating gate for the flash memory device are formed with one mask by self-alignment. Accordingly, the fabrication cost is decreased owing to the decreased number of masks used, and the re-operation possibility is also lowered. In addition, both problems in relation with an overlay margin and physical limitations resulting from reduced design size can be overcome.
Also, since the oxide film is formed without the gap-filling on formation of the field oxide, it is unnecessary to apply a CMP (Chemical Mechanical Polishing) process as well as the gap-filling on formation of the field oxide, thereby realizing the simplified process.
WHAT IS CLAIMED IS:

1. A method of fabricating a flash memory device comprising:

   sequentially forming a tunnel oxide film, a polysilicon film and a first insulation film on an active area of a semiconductor substrate;

   performing an etching process on the first insulation film;

   forming a hard mask on the semiconductor substrate;

   forming an STI by using the hard mask;

   oxidizing sidewalls of the STI and gap-filling the STI;

   forming a floating gate by removing the hard mask; and

   sequentially forming an ONO film and a control gate on the floating gate.

2. The method of claim 1, wherein performing the etching process includes forming a photoresist as a mask on the first insulation film, and performing the etching process using the photoresist as the mask.

3. The method of claim 1, wherein forming the hard mask includes depositing a second insulation film on the semiconductor substrate.

4. The method of claim 3, wherein the second insulation film prevents oxidation.
5. The method of claim 3, wherein removing the hard mask includes removing the second insulation film remaining as the hard mask.

6. The method of claim 2, wherein the first insulation film and the polysilicon film are etched by using the photoresist as the mask.

7. The method of claim 1, wherein the tunnel oxide film has a thickness between approximately 30Å and approximately 300Å.

8. The method of claim 7, wherein the tunnel oxide film is grown.

9. The method of claim 7, wherein the tunnel oxide film is deposited.

10. The method of claim 3, wherein the first and second insulation films are formed of oxide films of SiO₂.

11. The method of claim 3, wherein the first and second insulation films are formed of nitride films of SiN.

12. The method of claim 1, wherein the sidewalls of the STI are oxidized in an oxide-oxidization method.
13.  The method of claim 1, wherein the sidewalls of the STI are oxidized in an oxide-oxidization method, and then the STI is gap-filled to prevent forming voids therein.

14.  The method of claim 1, wherein the floating gate is larger than the tunnel oxide film in size of area, to obtain a coupling ratio between the floating gate and the control gate.

15.  The method of claim 1, wherein the flash memory device has an ETOX (EPROM Thin Oxide) cell structure.

16.  A flash memory device comprising:

a floating gate including a tunnel oxide film and a polysilicon film on an active area of a semiconductor substrate;

an STI wherein the sidewalls of the STI are oxidized in an oxide-oxidization method, and then the STI is gap-filled to prevent forming voids therein; and

an ONO film and a control gate sequentially formed on the floating gate.

17.  The flash memory device of claim 16, wherein the floating gate is larger than the tunnel oxide film in size of area, to obtain a coupling ratio between the floating gate and the control gate.

18.  The flash memory device of claim 16, wherein the tunnel oxide film has a thickness between approximately 30Å and approximately 300Å.
19. The flash memory device of claim 16, wherein the flash memory device has an ETOX (EPROM Thin Oxide) cell structure.

20. The flash memory device of claim 16, wherein a top surface of the tunnel oxide film and a bottom surface of the floating gate are coplanar across substantially their entire area.
ABSTRACT

A method of fabricating a flash memory which increases a coupling ratio between a floating gate and a control gate in a cell. The method comprises sequentially forming a tunnel oxide film, and polysilicon and first insulation films for a floating gate on an active area of a semiconductor substrate; forming a photoresist as a mask on the first insulation film, and performing an etching process using the photoresist as the mask; forming a hard mask by depositing a second insulation film for prevention of oxidation on the semiconductor substrate; forming an STI by using the hard mask; oxidizing sidewalls of the STI and gap-filling the STI; forming a floating gate by removing the second insulation film remaining as the hard mask; and sequentially forming an ONO film and a control gate on the floating gate.
# Electronic Patent Application Fee Transmittal

**Application Number:**

**Filing Date:**

**Title of Invention:** METHOD OF FABRICATING FLASH MEMORY DEVICE

**First Named Inventor/Applicant Name:** Sang-Woo Nam

**Filer:** Daniel Hilary Sherr

**Attorney Docket Number:** 604-0075

Filed as Large Entity

## Utility Filing Fees

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**New International Application Filed with the USPTO as a Receiving Office**

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### PATENT APPLICATION FEE DETERMINATION RECORD

**Substitute for Form PTO-875**

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**MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))**

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**TOTAL**

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<td><strong>FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))</strong></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**SMALL ENTITY**

<table>
<thead>
<tr>
<th>RATE ($)</th>
<th>ADDITIONAL FEE ($)</th>
</tr>
</thead>
<tbody>
<tr>
<td>X =</td>
<td></td>
</tr>
</tbody>
</table>

**OTHER THAN SMALL ENTITY**

<table>
<thead>
<tr>
<th>RATE ($)</th>
<th>ADDITIONAL FEE ($)</th>
</tr>
</thead>
<tbody>
<tr>
<td>X =</td>
<td></td>
</tr>
</tbody>
</table>

**TOTAL ADD'T FEE**

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* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Paten and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

*If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.*