WAFER CARRIER, WAFER LEVEL PACKAGING, AND MEMS

Gredmann Taiwan Ltd.

Initial Bidding Guidance: Low-to-Mid Six Figures

With a 2001 priority date, the disclosed portfolio describes systems and methods for wafer level packaging and fabricating cap structures, forming a wafer backside interconnecting wire, Wafer-level packaging cutting method capable of protecting contact pads, an integration manufacturing process for MEMS devices, for making a planar coil, fabricating a diaphragm of a capacitive microphone device. This portfolio includes the following:

Abstract (US 6,359,718)

An actuating mechanism for rotating a micro-mirror is disclosed. The actuating mechanism includes a first linking rod consisting of a first and a second portions, a second linking rod consisting of a third and a fourth portions, a first fulcrum positioned between the first and second portions, and a second fulcrum positioned at one side of the fourth portion opposite to the third portion. The first and third portions are flexibly connected to a shaft that the micro-mirror rotates with, and the second and fourth portions are coupled to respective actuators. When actuating forces are applied to move the second and fourth portions, the first and third portions are levered to rotate the shaft and thus the micro-mirror due to the effect of the fulcrums.

Abstract (US 7,002,725)

The micro grating structure is provided. The micro grating structure includes a substrate; a first supporting structure and a second supporting structure; a first structure post and a second structure post, wherein the first structure post and the second structure post are mounted on the substrate between the first supporting structure and the second supporting structure; and a grating mounted between the first structure post and the second structure post and comprising a first, a second, a third and a fourth torsion beams, wherein the first and the second torsion beams are connected to the first and the second supporting structures respectively, the third and the fourth torsion beams are connected to the first and the second structure posts respectively, and the first, the second, the third and the fourth torsion beams are twisted by an electrostatic force so as to enable the grating to be inclined at an angle with respect to the substrate.

Abstract (US 7,008,821)

A method of forming a wafer backside interconnecting wire includes forming a mask layer on the back surface, the mask layer including at least an opening corresponding to the bonding pad, performing a first etching process from the back surface to remove the wafer unprotected by the mask layer to form a recess, removing the mask layer, and forming an interconnecting wire on the back surface.

Abstract (US 7,045,463)

A method of etching cavities having different aspect ratios. An etching stop layer is formed on the bottom surface of a substrate, and a mask pattern is formed on the top surface of the substrate. The mask pattern includes a plurality of sacrificial patterns positioned on both a first cavity predetermined region and a second cavity predetermined region. Then, an etching process is performed to remove the substrate not covered by the mask layer. Then, the etching stop layer is removed, as well as the sacrificial patterns and the substrate covered by the sacrificial patterns.

Abstract (US 7,258,806 & US 7,585,417)

A method of fabricating a diaphragm of a capacitive microphone device. First, a substrate is provided, and a dielectric layer on a first surface of the substrate is formed. Than, a plurality of silicon spacers are formed on a surface of the dielectric layer, and a diaphragm layer is formed on a surface

ICAP PATENT BROKERAGE

TECHNOLOGY
SEMICONDUCTORS

IMPORTANCE
IMPORTANT PORTFOLIO FOR SEMICONDUCTOR COMPANIES

NUMBER OF ASSETS
33

PATENTS (20)
US 6359718
US 7002725
US 7008821
US 7045463
US 7258806
US 7361284
US 7505118
US 7533564
US 7582511
US 7585417
US 7598125
US 7605970
US 7622334
US 7987588
US 8030111
US 8114699
US 8310328
US 8318511
US 8453318
US 8456724

OTHER PATENTS (13)
TW 480346
TW I256940
TW I363414
TW I284966
TW I278045
TW I229377
TW I305998
TW I305474
TW I234261
TW I222534
TW I275416
TW I242255
TW I376739

of the silicon spacers and the surface of the dielectric layer. Subsequently, a planarization layer is formed on the diaphragm layer, and a second surface of the substrate is etched to form a plurality of openings corresponding to the diaphragm layer disposed on the surface of the dielectric layer. Thereafter, the dielectric layer exposed through the openings is removed, and planarization layer is removed.

Abstract (US 7,361,284)

A method for wafer-level package. A cap wafer having cavities is bonded to a support wafer, and a portion of the cap wafer is etched through. The cap wafer is released from the support wafer, and bonded to a transparent wafer, and a portion of the cap wafer corresponding to the cavities is removed so that the remaining cap wafer forms a plurality of support blocks. A device wafer is provided, and the support blocks are bonded to the device wafer so that the support blocks and the transparent wafer hermitically seal the devices disposed in the device wafer.

Abstract (US 8,030,111; US 8,114,699; US 8,318,511)

A method for manufacturing an MEMS device is provided. The method includes steps of a) providing a first substrate having a concavity located thereon, b) providing a second substrate having a connecting area and an actuating area respectively located thereon, c) forming plural microstructures in the actuating area, d) mounting a conducting element in the connecting area and the actuating area, e) forming an insulating layer on the conducting element and f) connecting the first substrate to the connecting area to form the MEMS device. The concavity contains the plural microstructures.

Abstract (US 8,310,328 & US 8,453,318)

A method of making a planar coil is disclosed in the present invention. First, a substrate having a trench is provided. Then, a barrier and a seed layer are formed on the substrate in sequence. An isolative layer is used for guiding a conductive material to flow into a lower portion of the trench such that accumulation of the conductive material at opening of the trench is prevented before the lower portion of the trench is completely filled up, thereby avoiding gap formation in the trench.

Abstract (US 7,505,118)

A wafer carrier for carrying a wafer includes a transparent base and a conducting layer. The transparent base has dimensions similar to that of the wafer, and bonds the wafer with a bonding layer. The conducting layer is transparent, and can be attracted by an electrostatic chuck so that the electrostatic chuck can deliver the wafer.

Abstract (US 7,533,564)

A micro sample heating apparatus has a substrate, a micro heating device disposed on a first surface of the substrate, a cavity having a vertical sidewall and corresponding to the micro heating device positioned in a second surface of the substrate, and an isolation structure positioned on the second surface of the substrate. The isolation structure has an opening corresponding to the cavity, and the cavity and the opening form a sample room.

Abstract (US 7,598,125)

A cap wafer with cavities is etched through areas not covered by a patterned photoresist to form a plurality of openings. The cap wafer is bonded to a transparent wafer at the surface having the cavities and is segmented around the cavities to form a plurality of cap structures. The cap structures are hermetically sealed to a device wafer to form hermetic windows over devices and pads located on the device wafer.

Abstract (US 7,582,511)

The present invention provides a Wafer Level Chip Scale Packaging structure including a die, at least one passive component, a combining layer, an isolating layer, at least one connecting wire, an internal pad and a passivation layer. The die includes a shallow connecting pad, an internal pad and an

electrical component. The passive component is formed on one side of the die. The combining layer increases the binding force between the passive component and the die. The part surface on the other side of the die is overlaid with the isolation layer. The part surface of the isolation layer and the internal pad is overlaid with the connecting wire to electrically connect to the internal pad, and the passivation layer is used for protecting the die.

Abstract (US 7,605,970)

A tunable laser system is provided. The tunable laser system includes a light source, a grating, a corner mirror array, and a receiver. In which, the light source emits a beam, and the grating is located in front of the light source for reflecting the beam to form a first reflective beam. Also, the corner mirror array is located in front of the grating for receiving the first reflective beam and forms a second reflective beam accordingly. In addition, the receiver is used to receive a third reflective beam formed from reflecting the second reflective beam through the grating.

Abstract (US 7,622,334)

A cutting method for wafer-level packaging capable of protecting the contact pad, in which several cavities and precutting lines are formed at the front surface of a cap wafer, and the depth of each precutting line is lesser than the thickness of the cap wafer, followed by the bonding of the cap wafer to the device wafer, which has several devices and several bonding pads disposed on the surface of the device wafer, followed by performing a wafer dicing process, along the precutting lines cutting through the cap wafer, and after removing a portion of the cap wafer that is not bonded to the device wafer, for exposing the bonding pads at the surface of the device wafer, and finally performing a dicing process for forming many packaged dies.

Abstract (US 7,987,588)

The invention discloses an interposer used for connecting a plurality of chips. The interposer includes a connective substrate and at least a through via disposed in the connective substrate. The connective substrate has a first surface and a second surface. The through via acts as a connector, and is electrically connected to the first surface and the second surface. The first surface and the second surface are electrically connected to at least a first chip and a second chip respectively. In addition, the first chip and the second chip are electrically connected by the through via.

Earliest Priority Date: 2-1-2001

Representative Claims: US 7,361,284 – Claim #1

1. A method for wafer-level package, comprising: providing a cap wafer; forming a plurality of cavities in a first surface of the cap wafer; bonding the first surface of the cap wafer to a support wafer; etching through a portion of the cap wafer surrounding the cavities from a second surface of the cap wafer; removing the cap wafer from the support wafer, and bonding the first surface of the cap wafer to a transparent wafer; removing a portion of the cap wafer corresponding to the cavities from the second surface of the cap wafer so that the remaining cap wafer form a plurality of support blocks; providing a device wafer comprising a plurality of devices and a plurality of contact pads; and bonding the support blocks to the device wafer so that the support blocks and the transparent wafer hermitically seal the devices.

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