With a 2006 priority date, the disclosed portfolio describes a broad range of memory chip technologies related to EPROM, EEPROM, Flash Memory and CIS, including:

US 8,648,406 — Single poly eeprom having a tunnel oxide layer
A single poly EEPROM (Electrically Erasable Programmable Read Only Memory), which may include at least one of the following: (1) A second conductive type well formed on and/or over a semiconductor substrate. (2) A first conductive type source and drain regions formed in the second conductive type well. The single poly EEPROM may include at least one of: (a) A tunnel oxide layer formed on and/or over the second conductive type well. (b) A floating gate formed on and/or over the tunnel oxide layer and doped with second conductive type impurity ions. (c) A first conductive type impurity region formed in the second conductive type well adjacent to the floating gate. The floating gate may be configured such that a concentration of a region of the floating gate adjacent to the drain region is higher than that of the other region of the floating gate adjacent to the impurity region.

US 8,264,030 — Flash memory device and manufacturing method of the same
A flash memory device and a method for manufacturing the same are provided. The flash memory device can include first and second memory gates on a substrate, an oxide layer on sides of and on the substrate outside of the first and second memory gates, a source poly contact between the first and second memory gates, first and second select gates outside the first and second memory gates, a drain region outside the first and second select gates, and a metal contact on the drain region and the source poly contact.

US 8,258,566 — Eeprom device and method of manufacturing the same
An EEPROM device may have, at the region where the control gate is formed, a gate oxide layer having a relatively smaller thickness than the gate oxide layer of the tunneling region by removing the gate oxide layer, at a predetermined thickness, at the region where the control gate is formed. Thus, integration of an EEPROM device may be maximized as a result of minimizing the area of the control gate.

US 8,217,447 — Flash memory device with a plurality of source plates
A flash memory device and a method of manufacturing a flash memory device. A flash memory device may include an isolation layer and/or an active area over a semiconductor substrate, a memory gate formed over an active area, a control gate formed over a semiconductor substrate including a memory gate, and/or a common source line contact formed over a semiconductor substrate including a control gate. A flash memory device may include a source plate having substantially the same interval as an interval of an active area of a bit line. A source plate may include an active area in which a common source line contact may be formed. A common source line contact may include a long butting contact extending in a direction traversing an active area.

US 8,193,052 — Flash memory device and method of manufacturing the same
Disclosed is a flash memory device and a method of manufacturing the same. The flash memory
A flash memory device may include a device isolation layer and an active area formed over a semiconductor substrate, a memory gate formed over the active area, and a control gate formed over the semiconductor substrate including the memory gate, wherein the active area, where a source contact is to be formed, has the same interval spacing as a bit line, and a common source line area, where the source contact is to be formed, has an impurity area connecting neighboring active areas.

A method of fabricating non-volatile memory device with concavely depressed electron injection region

Provided are a non-volatile memory device and a method of fabricating the same. The non-volatile memory device comprises: a control gate region formed by doping a semiconductor substrate with second impurities; an electron injection region formed by doping the semiconductor substrate with first impurities, where a top surface of the electron injection region includes a tip portion at an edge; a floating gate electrode covering at least a portion of the control gate region and the tip portion of the electron injection region; a first tunnel oxide layer interposed between the floating gate electrode and the control gate region; a second tunnel oxide layer interposed between the floating gate electrode and the electron injection region; a trench surrounding the electron injection region in the semiconductor substrate; and a device isolation layer pattern filled in the trench.

A method of manufacturing flash memory device

A method of manufacturing a flash memory device includes preparing a semiconductor substrate comprising a cell area and a peripheral area, forming a first well and an oxide-nitride-oxide (ONO) layer in the cell area, forming a second well in the peripheral area of the semiconductor substrate comprising the first well and forming a first oxide layer in the peripheral area, forming a first polysilicon layer over the ONO layer and the first oxide layer and performing a first etch process to form a memory gate comprising an ONO layer pattern and a first polysilicon pattern in the cell area, forming a second oxide layer pattern and a second polysilicon pattern over either sidewall of the memory gate and forming a gate in the peripheral area, performing a third etch process so that the second oxide layer pattern and the second polysilicon pattern remain over only the one sidewall of the memory gate to form a select gate, and forming a first impurity area in the semiconductor substrate between the memory gates adjacent to each other.

A method of manufacturing flash memory device

A method of manufacturing a flash memory device that prevents generation of voids when forming an interlayer dielectric film. The method may include forming a gate on a semiconductor substrate, and then sequentially stacking a first dielectric film and a second dielectric film on the semiconductor substrate, and then forming a first spacer comprising a first dielectric film pattern and a second dielectric film pattern on sidewalls of the gate by performing a first etching process, and then forming source and drain areas in the semiconductor substrate, and then removing the second dielectric film, and then sequentially stacking a third dielectric film and a fourth dielectric film on the semiconductor substrate, and then forming a second spacer comprising the first dielectric pattern and a third dielectric pattern on the sidewalls of the gate by performing a second etching process, and then forming an interlayer dielectric film on the semiconductor substrate including the gate and the first spacer.
US 7,618,863 — Method of fabricating flash memory device with increased coupling ratio
A method of fabricating a flash memory which increases a coupling ratio between a floating gate and a control gate in a cell. The method comprises sequentially forming a tunnel oxide film, and polysilicon and first insulation films for a floating gate on an active area of a semiconductor substrate; forming a photoresist as a mask on the first insulation film, and performing an etching process using the photoresist as the mask; forming a hard mask by depositing a second insulation film for prevention of oxidation on the semiconductor substrate; forming an STI by using the hard mask; oxidizing sidewalls of the STI and gap-filling the STI; forming a floating gate by removing the second insulation film remaining as the hard mask; and sequentially forming an ONO film and a control gate on the floating gate.

Sample Forward Citing Companies: Renesas Electronics Corporation, Samsung Electronics

Earliest Priority Date: 9-4-2006

Representative Claim: US 7,883,952 – Claim #1
A method comprising: forming a gate on a semiconductor substrate; and then sequentially stacking a first dielectric film and a second dielectric film on the semiconductor substrate; and then forming a first spacer comprising a first dielectric film pattern and a second dielectric film pattern on sidewalls of the gate by performing a first etching process; and then forming source and drain areas in the semiconductor substrate; and then removing the second dielectric film; and then sequentially stacking a third dielectric film and a fourth dielectric film on the semiconductor substrate; and then forming a second spacer comprising the first dielectric pattern and a third dielectric pattern on the sidewalls of the gate by performing a second etching process, wherein forming the second spacer comprises performing the second etching process removing a portion of the third dielectric film and the entire fourth dielectric film; and then forming an interlayer dielectric film on the semiconductor substrate including the gate and the first spacer.

Contact:
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