ICAP PATENT BROKERAGE

Enhanced Digital Signal Processing

Divan Industries, LLC

Initial Bidding Guidance: Low 6 Figures

With priority dates from 1998, this portfolio offers benefits for performing and enhancing digital signal processing operations, including:

1. Methods and apparatus for improving the way in which digital signal processors perform a wide variety of common operations including cross-correlation, sorting, finite impulse response filtering, in addition to other operations which use multiply, add, subtract, compare and/or store functionality. *[6,401,106; 6,754,805]*

2. Methods and apparatus for simultaneously and efficiently transferring synchronous and asynchronous signals among broadband access devices using a minimum number of lines. The patent covers a bus which includes a data bus, a clock bus, and a plurality of control lines which are used to indicate the type of data being carried on the data bus. Data is transferred on the bus in a repeating frame having a plurality of slots, each slot being defined as one bus clock cycle. Each slot may contain a synchronous or asynchronous data signal and one or more of the control lines are asserted during the slot time of the data to indicate the type of data. *[7,313,151]*

3. Methods and apparatus for handling maintenance messages in extended superframe T1 telephone circuits which makes efficient use of FIFO buffers. *[6,539,023]*

4. Methods and apparatus for calculating a pointer leak rate for retiming a SONET signal which (i) can switch between slower and faster leak rates and (ii) which efficiently absorbs short-term pointer bursts and; (iii) provides a leak rate substantially slower than the net asking rate. *[7,349,444]*

5. A method and apparatus for reliably detecting both AIS and AIS-CI signals in the presence of a bit error ratio up to 1×10−3 includes an AIS detector having an AIS indication output, a CI detector having a CI indication output, and a two signal AND gate having its inputs coupled to the respective outputs of the detectors and having an output indicative of an AIS-CI detection. *[6,456,595]*

6. A method and apparatus for (i) digitally correcting imperfectly equalized bipolar signals; (ii) eliminating erroneous pulses from an over-equalized bipolar signal; (iii) correcting the pulse width of an equalized bipolar signal and; (iv) eliminate erroneous bipolar violations from an equalized bipolar signal. *[6,271,698]*

7. Methods and apparatus for managing traffic in an ATM network by queuing ATM cells in an ATM switch. Further, the patent covers methods and apparatus for allocating available bandwidth according to fairness mechanisms. *[6,243,359]*

Earliest Priority Date: 9-28-1998

Sample Forward Citing Companies: Airbus, Alcatel-Lucent, Altera, Arista Networks, Atrenta, Broadcom, Cisco, Ericsson, Fujitsu, Hewlett-Packard, IBM, Intel, LG, Locution Pitch LLC, Mercury Computer Systems Inc., NXP Semiconductors, PACT XPP Technologies, Qualcomm, Sony

TECHNOLOGY

TELECOMMUNICATIONS; DSP

NOVELTY

METHODS AND APPARATUS FOR PERFORMING DIGITAL SIGNAL PROCESSING OPERATIONS AND, MORE SPECIFICALLY, TO METHODS AND APPARATUS FOR ENHANCING DIGITAL SIGNAL PROCESSORS

IMPORTANCE

A VALUABLE PORTFOLIO FOR TELECOMMUNICATION AND NETWORKING COMPANIES AS WELL AS COMPANIES WITH LARGE DATA CENTERS AND CLOUD NETWORKS

NUMBER OF ASSETS

33

PATENTS (13)

US 6,243,359
US 6,271,698
US 6,401,106
US 6,456,595
US 6,539,023
US 6,577,651
US 6,754,805
US 7,313,151
US 7,349,444
BE 1360787
EP 1360787
FR 1360787
GB 1360787

APPLICATIONS (20)

AT 20020714788
AU 20010078172
AU 20010079208
CA 19992283609
CA 19992283611
CA 20002371567
CA 20002388002
CN 2000809412
CN 2000815656
CN 2002804083
EP 20000926114
EP 20000993004
IL 149710
IN/PCT/2002/703/CHE
JP 20000616146
PCT/US00/10474
PCT/US00/41974
PCT/US01/24666
PCT/US01/24667
PCT/US02/02253

Representative Claim: US 6,456,595 – Claim #1

An apparatus for detecting AIS and AIS-CI signals in a DS1 data stream, said apparatus comprising: a) an adjustable threshold AIS detector having a threshold adjustment means for raising its zero error threshold and an AIS indication output, said AIS detector being coupled to the DS1 data stream; b) a CI code word detector having a first output coupled to said threshold adjustment means and a CI indication output; and c) logical AND means coupled to said AIS indication output and said CI indication output, said logical AND means for providing an indication when said AIS indication output and said CI indication output are both activated.

Contact:

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