

AVAILABLE PORTFOLIOS SEMICONDUCTORS

PS 511	SYSTEM-ON-CHIP & NOISE REDUCTION TECHNIQUES <i>iKoa Corporation</i>
PS 558	MICROFLUIDIC LAB-ON-A-CHIP DEVICES <i>Siemens Aktiengesellschaft</i>
PS 577	GAS & ISOTOPE SEPARATION TECHNIQUES <i>Armington Technologies, LLC</i>
PS 591	DIAMOND SEMICONDUCTOR SYSTEM, PROCESS, METHOD, & DEVICES <i>AKHAN Technologies, Inc.</i>
PS 593	ISOTOPICALLY PURE SEMICONDUCTOR MATERIALS <i>Armington Technologies, LLC</i>

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SYSTEM-ON-CHIP & NOISE REDUCTION TECHNIQUES

iKoa Corporation

This patent portfolio discloses techniques for implementing System-on-Chip (SOC) technologies for stateful, transaction-oriented applications. This portfolio also discloses techniques for suppressing noise in audio signals.

SOC is an integrated chip that combines all the components of an electronic system together such as processors and memory. SOC is widely used in electronic devices such as laptops, computers, televisions, and embedded system devices. Advancements in the semiconductor industry have made significant cost impacts in SOC design cycle time and product quality. Further, SOC implementations of stateful, transaction-oriented applications depend heavily on on-chip memory bandwidth, capacity for performance, and power savings. However, placement of a large number of memory modules on the SOC is a major bottleneck in SOC physical design. Computer Aided Design techniques have had limited success in addressing the advanced design requirements for these systems, therefore, there is a need for a cost-effective methodology to implement SOC for stateful, transaction-oriented applications. Noise reduction technology is another market covered by the assets in this portfolio and is used to reduce or suppress noise in audio signals in devices such as mobile phones, laptops, microphones, and headphones.

Value Proposition: This portfolio discloses techniques that include:

- Performing in-memory computations for stateful, transaction-oriented applications and systems. These techniques disclose a device that includes a multi-level array of memory storage cells and logic circuits. These storage cells can have multiple configurable access paths and are capable of being simultaneously accessed to read and write. This portfolio offers a solution to traditional CAD techniques by offering a cost-effective way to implement SOC while addressing advanced design requirements.
- An audio signal enhancement device having two microphones and facing in opposing directions. A speech signal is detected by one microphone and the undesired noise signals not originating in the proximity of the device are detected from the other microphone. Pressure gradient of the signals on the microphones are determined and used to process the signals to suppress noise.

Priority Date: 06-27-2005

Representative Claim: US 7,614,020 – Claim #1

A structurally reconfigurable semiconductor circuit device for in-memory processing of stateful, transaction-oriented applications, comprising: a multiple level array of memory storage cells and logic circuits, the storage cells having multiple configurable access paths, the storage cells capable of being simultaneously accessed for being read from and written into; a plurality of configurable, packetized interface ports capable of receiving data packets, the packetized interface ports having access to the multiple level array; a plurality of configurable commute elements distributed within the multiple level array, each of the plurality of configurable commute element configured to move data within the multiple level array of storage cells through one of the multiple configurable access paths; a plurality of configurable Compute elements within the multiple level array, each of the plurality of configurable Compute elements configured to transform data within a portion of the multiple level array of storage cells via the multiple configurable access paths; and a pool of redundant features for repairing a defective feature within the multiple level array, wherein levels of the multiple level array associated with a higher defect density have more redundant features available for repair relative to levels associated with a lower defect density.

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TECHNOLOGY

SEMICONDUCTORS &
ELECTRONIC DEVICES

NOVELTY

ADVANCED SYSTEM-
ON-CHIP (SOC)
TECHNOLOGIES AND
NOISE REDUCTION
TECHNIQUES

IMPORTANCE

PORTFOLIO HAS
SIGNIFICANT POTENTIAL
IN THE MULTI-BILLION
DOLLAR GLOBAL SOC
MARKET AS WELL AS FOR
COMPANIES DEVELOPING
ELECTRONIC DEVICES

NUMBER OF ASSETS

5

US PATENTS (3)

7,614,020
7,676,783
7,849,441

US APPLICATIONS (2)

11/757,110
12/573,827

**PS
511**

MICROFLUIDIC LAB-ON-A-CHIP DEVICES

Siemens Aktiengesellschaft

This patent portfolio discloses technologies related to Lab-on-a-chip (LOC) devices.

The inventions in this portfolio have laid the foundation for minute, portable, robust analysis systems in credit-card format. Cost-efficient laboratory diagnostics and rapid on-site analysis, for example, to detect toxins, are possible with the LOC technologies. The principle of the electric biochip can also be applied to food analysis, pharmaceuticals, agricultural, and environmental analyses.

The goal of this project was to design sensor systems that are economic, efficient, and capable of being manufactured on a large scale for use as miniature labs. This technology becomes a “Lab-on-a-Chip” when liquids and reagents are applied to the sensor surfaces. The entire innovation consists of a combination of silicon chip technology, biotechnology, and miniaturized fluidic technology.

Using a biochip, biomolecules such as nucleic acids or proteins, can be traced in watery solutions. Biomolecules anchored on the chip – so-called catchers – accurately bind certain other molecules. This produces a highly sensitive sensor for DNA or proteins. Reading of the results with a light beam, however, has usually been technically complex and expensive, so this was replaced with a simpler and cost-efficient technology. The results are read on the chip by means of electrical measurements. The basis for this method is the discovery that as soon as it has found its counterpart, a catcher molecule emits an electrical signal which can be directly analyzed.

Value Proposition: This portfolio addresses market limitations by disclosing:

- Techniques for manufacturing cost-effective sensor arrangements. Further, these arrangements are powered with increased detection sensitivity of detecting particles (or molecules) possibly contained in any analyte. Such sensor arrangements have potentially diverse applications in medical diagnosis, pharmacology (e.g. for pharmacological screening, “high throughput screening” HTS), the chemical industry, as well as ecological and foodstuffs technologies.
- Techniques for detecting Nucleotide sequences (DNA/RNA) using electrophoresis, SNP analysis, isolation of magnetic beads and thermocycling with the polymerase chain reaction (PCR) for sensor applications, e.g. DNA Sensor or Microsystems engineering applications such as micro-electrophoresis. This type of micro sensor chip is useful in the medical diagnostics industry.
- Techniques for extraction of a smear sample (complete DNA or protein) via microfluidic systems of biochip-based cartridge and its detection and analysis through electrochemical measurement by PCR. Also a useful innovation within the medical diagnostics industry.

Forward Citing Companies: Infineon Technologies, Renesas Electric Corporation, Wafergen

TECHNOLOGY

SEMICONDUCTORS;
MICROFLUIDICS

NOVELTY

ECONOMIC AND EFFICIENT
MINIATURE LAB SENSOR
SYSTEMS

IMPORTANCE

STRATEGIC IP FOR LAB-
ON-A-CHIP MARKET
THAT SHOULD BE OF
INTEREST TO CHEMICAL,
MEDICAL, FOOD, AND
PHARMACOLOGICAL
INDUSTRIES

NUMBER OF ASSETS

200+

US PATENTS (19)

6,922,081
7,030,340
7,398,671
7,432,068
7,488,578
7,510,839
7,566,968
7,572,624
7,591,938
7,642,053
7,670,557
7,756,560
7,851,227
7,914,655
7,932,082

4 other applications have
been allowed. Not yet
granted a patent number.

*Please inquire for a
complete asset listing.*

Representative Patents and Claims

1. US patent 7,432,068 – Biosensor and method for detecting macromolecular biopolymers using a biosensor

Priority Date: 03-30-2000

Representative Claim: Claim #1

A biosensor comprising: a first electrode device, which has a holding region for holding probe molecules which can bind macromolecular biopolymers; and a second electrode device; a control unit for controlling the first and the second electrode device; wherein the first electrode device and/or the second electrode device is/are divided into a plurality of electrode segments, the electrode segments are electrically insulated from one another but can be electrically coupled to one another for adjusting the size of the effective electrode face area as a function of the electrode segments selected and coupled, wherein the control unit controls the size of the effective electrode face area, adjusting the size of the effective electrode face area to the strength of the electrical signals from the electrode devices by coupling or decoupling the electrode segments to each other or from each other.

2. US patent 7,566,968 – Biosensor with smart card configuration

Priority Date: 02-05-2003

Representative Claim: Claim #1

A biosensor comprising: a semiconductor chip including a bioactive structure and contact areas disposed on a first side of the semiconductor chip; and a rewiring substrate including contact pads, external contact areas and rewiring lines that electrically connect the contact pads to the external contact areas; wherein the rewiring substrate is directly positioned on and covers a portion of the first side of the semiconductor chip without covering the bioactive structure such that the rewiring substrate overlaps the contact areas of the semiconductor chip, and the contact pads of the rewiring substrate and the contact areas of the semiconductor chip are positioned directly on, aligned with and electrically connected to each other.

3. US patent 7,572,624 – DNA chip comprising a microarray made of an microelectrode system

Priority Date: 12-19-2002

Representative Claim: Claim #1

A DNA chip, comprising: a carrier; and a microarray of spots, arranged on the carrier, containing immobilized catcher molecules, each spot containing a thin-film four pole system for the impedance-spectroscopic detection of binding events between the catcher molecules and target molecules of an analyte solution applied to the spots the thin-film four-pole system including two polarization electrodes for generating an alternating electromagnetic field and two sensor electrodes for measuring a voltage drop in the analyte.

4. US Patent 7,488,578 – Method for detecting DNA point mutations (single nucleotide polymorphism (SNP) analysis) and associated arrangement

Priority Date: 05-30-2003

Representative Claim: Claim #1

A method for detecting DNA point mutations utilizing capture/target DNA hybrids at hybridization positions, the capture/target DNA hybrids formed by binding target DNA to be detected to capture DNA immobilized position-specifically on a DNA chip, the method comprising, performing a washing phase and a measurement phase alternately at different temperatures,

the washing phase including:

- a) passing a washing liquid at a controlled flow rate over the DNA chip,
- b) changing the temperature at the hybridization positions in a defined manner as a function of time, with a continuous increase in temperature as a function of time being carried out in ramps with subsequent temperature holding times, and
- c) melting the capture/target DNA hybrids temperature-dependently, and removing melted target DNA from the hybridization positions using the flowing washing liquid, such that non-melted target DNA remains on the DNA chip,

the measurement phase including:

- d) stopping the flow of washing liquid during the temperature holding times,

- e) position-specifically detecting the non-melted target DNA at a current temperature of the temperature holding time, and
- f) analyzing signals according to a predetermined program, the analyzed signals being used to detect the DNA point mutations.

5. US Patent 7,510,839 - Method for the combined isolation of magnet-beads from a liquid sample and subsequent thermocyclisation for the polymerase chain reaction (PCR) and associated arrangement

Priority Date: 10-15-2004

Representative Claim: Claim #5

An arrangement for the isolation of magnetic beads from a liquid sample and subsequent thermocycling for a PCR (polymerase chain reaction), in which the liquid sample can flow in a flow channel opening out to a sample chamber and the magnetic beads are isolatable there by a magnetic field with a field gradient in the direction of flow and subjectable in the sample chamber to thermocycling in accordance with a prescribed program, the arrangement comprising: means for generating a magnetic field gradient in the sample chamber; and means for permitting thermostatic control of the sample chamber.

6. US Patent 7,932,082 - Device and method for extracting a smear sample

Priority Date: 11-17-2005

Representative Claim: Claim #19

A device for extracting a smear sample, comprising: a cavity, into which a sample carrier carrying a smear sample is introducible; at least one liquid feed connected to the cavity, through which liquid is introducible into the cavity, wherein the cavity includes an inlet opening via which the liquid feed is fluidly connected to the cavity; at least one liquid discharge connected to the cavity, through which liquid is removable from the cavity. wherein the cavity includes an outlet opening via which the liquid discharge is fluidly connected to the cavity; and an interface to a microfluidic system, into which liquid is transferable, wherein in a region of the outlet opening, the cavity is tapered so that, when the sample carrier is introduced, the sample carrier is mechanically deformed such that the smear sample at least partially escapes.

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GAS & ISOTOPE SEPARATION TECHNIQUES

Armington Technologies, LLC

This patent portfolio discloses separation techniques used in such areas as natural gas processing, Organic Rankine Cycle power generation, refrigeration, and semiconductor production. Vast natural gas reserves remain unused due to the limitations of current natural gas processing methods. Accordingly, the refrigeration industry has long searched for a device to simultaneously expand the refrigerant and separate its liquid and gas phases. The recent industry wave of creating renewable energy systems from untapped waste heat (Organic Rankine Cycle) requires a device to expand and separate the liquid and gas phases of its work fluid. In this scenario, isotopically purifying semiconductor pre-cursor gases helps prevent debilitating heat build up.

Value Proposition: The portfolio discloses an aerodynamic separation nozzle that separates different constituents of gas or different phases from the same gas by using phase change, centrifugal forces and controlling different parameters. These parameters are mass differences of condensed particles and gas, velocity of flow in the nozzle, inlet temperature of the gas into the nozzle, length of expansion within the nozzle, radius of the nozzle, and temperature of the separation nozzle. The separation portfolio addresses market limitations by disclosing gas separation techniques for natural gas, Rankine and refrigeration cycles, and chemical processing, as well as for isotopically purifying the pre-cursor gases used to manufacture semiconductor wafers.

Priority Date: 07-14-2008

Representative Claim: US 8,016,901 – Claim 24

A device for separating constituents of a flow comprising: an inlet adapted to receive the flow; a throat fluidly coupled to said inlet and adapted to receive the flow from the inlet; a skimmer fluidly coupled to said throat via a separation flow path and adapted to separate the flow into a first stream and a second stream; a curved expansion nozzle disposed within at least a portion of said separation flow path, wherein said separation flow path defines a geometric gas expansion of less than about 5; and a device comprising a means for holding the temperature of said nozzle module at a desired nozzle temperature.

Animated description of this separation technology can be seen at:
http://www.youtube.com/watch?v=h4sZl8mws_E.

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TECHNOLOGY

SEMICONDUCTORS;
SEPARATION TECHNIQUES

NOVELTY

SEPARATION OF GASES AND ISOTOPES USING AN AERODYNAMIC SEPARATION NOZZLE AND A COMBINATION OF PHASE CHANGE CONDENSATION AND MASSIVE CENTRIFUGAL FORCES

IMPORTANCE

STRATEGIC PORTFOLIO FOR CHEMICAL AND PETROLEUM REFINING COMPANIES

NUMBER OF ASSETS

11

US PATENTS (1)

8,016,901

APPLICATIONS (10)

US 11/960,684
US 13/172,399
US 60/870,767
US 61/080,672
AU 20070333629
CA 20072710027
EP 20070869586
EP 20080825227
PCT/US07/88251
PCT/US08/79640

DIAMOND SEMICONDUCTOR SYSTEM, PROCESS, METHOD, & DEVICES

AKHAN Technologies, Inc.

The portfolio discloses a new and improved system and method for fabricating diamond semiconductor materials and devices, and in particular a first demonstration of genuine n-type diamond and n-type ohmic contact. Proprietary device materials demonstrate an n-type diamond material created over silicon with previously undemonstrated characteristics, such as shallow ionization energy of 250 meV, high carrier mobility (1841 cm²/Vs in nanocrystalline diamond thin films), no graphitic phases, and previously undemonstrated performance in low-voltage/high-current diode device applications (900 A/mm² current density at +2V forward bias). The creation of the material and its demonstrated application use in varying diode structures directly challenges the domination of silicon. Microchip devices fabricated from the disclosed techniques boast the capability to run electronics at higher speeds (1841 cm²/Vs versus <1400 cm²/Vs for electron mobility and 1000 cm²/Vs versus <450 cm²/Vs for hole mobility), with increased power handling capability (75 • W/mm demonstrated [DC] in low field), without overheating (600°C versus 150°C maximum operating junction temperature), and yielding system level application benefits like thinner/cheaper computers, longer lasting cell phone batteries, picture perfect TV screens, among others. All these while reducing the device and system level cost. The portfolio encompasses all required aspects of Front End and Back End Processing (FEOL & BEOL) to allow for complete commercialization and substantially favorable IP positioning.

Value Proposition: The value offering is segmented into four categories: a) the intellectual property covering the system, materials, and devices b) the intellectual property covering the metallization process and the ability to make electrical contact to the system, materials, and devices c) the intellectual property covering the etching process methods and the ability to shape features and devices from said materials and systems, and d) the intellectual property positioning allowing for key control over the emerging diamond semiconductor market through use of filed continuations and future application filings.

- a) This segment of the portfolio discloses a new and improved system and method for fabricating diamond semiconductors, as well as demonstrates via disclosed process techniques next-generation diode devices, enabling application use in a variety of markets including Power/RF, Monolithic Microwave Integrated Circuit (MMIC), Logic, and many others. The methods and processes disclosed allow for the creation of a number of electrical diamond junctions to serve functions traditionally served by silicon semiconductors. The demonstrated/fabricated devices show generational advances as compared to both previous diamond efforts and cutting-edge silicon devices with respect to both performance and cost, while maintaining compatibility with existing process lines (absolved need for specialized tooling). While the devices demonstrated are construed in the architecture of a bipolar diode, the techniques describe novel genuine n-type diamond material and novel p-type diamond material that may be used in multiple variations of electrical devices and monolithically formed combinations of the variations, including FETs and other switches, digital and analog, and light emitting bodies, and are not limited to the specific device implementations disclosed.
- b) This segment discloses novel process methods to address ohmic and schottky type contact to diamond semiconductor systems (p-type and n-type) and when applied to novel n-type thin films, allows for the first fabrication of a semiconductor device that can deliver both

TECHNOLOGY

SEMICONDUCTORS

NOVELTY

FIRST FABRICATION OF GENUINE N-TYPE DIAMOND MATERIAL, FIRST FABRICATION OF N-TYPE OHMIC CONTACT, AND FIRST FABRICATION OF COMMERCIALY VIABLE AND SUPERIOR DIAMOND SEMICONDUCTOR BIPOLEAR DEVICES.

IMPORTANCE

BREAKTHROUGH IP IS FIRST RESOLUTION TO LONG STANDING ISSUES PERTAINING TO A SIZEABLE MARKET SHARE OF THE GLOBAL SEMICONDUCTOR MARKET WITH NO PRIOR ART IN THE RELEVANT SPACE. FURTHER PORTFOLIO ENABLES FULL AND IMMEDIATE COMMERCIALIZATION.

NUMBER OF ASSETS

6

US APPLICATIONS (5)

13/273,467
61/513,569
61/578,364
61/578,371
61/583,841

TRADEMARKS (1)

85501875

high voltage and low voltage with variable current levels far exceeding current devices demonstrated, featuring previously undemonstrated n-type ohmic contact to diamond device.

- c) This segment of the portfolio discloses process methods to controllably etch thin film diamond materials and when applied to thin film polycrystalline diamond semiconductor films as demonstrated, produces highly uniform film structures, mirror like in crystallinity with very low surface roughness, and has the added ability of providing excellent electronic isolation of newly exposed etch-areas of said films, which is known necessary step in the semiconductor device fabrication process, thereby reducing overall proves time of any device process line requirements.
- d) The "Breakthrough" IP represents the resolution to several long standing (60+ years) issues such as the fabrication of genuine n-type diamond materials, the fabrication of n-type ohmic contact, and film smoothness. With the absence of prior art offering resolution to said issues, the portfolio allows for the buyer to maximize their earning potential as several continuations may be filed to allow for controlling position over the diamond semiconductor market for the life of the patent (20 years). Further, as demonstrated devices show not only improved performance compared to leading Silicon devices, but a reduction in cost (device and system level), and ease in fabrication, the portfolio represents highly disruptive positioning with respect to the existing global semiconductor market, estimated at \$310 Billion (USD) in 2010.

Priority Date: 07-30-2011

Representative Claims: US 13/273,267- Claim #1

A semiconductor system comprising: A diamond material having n-type donor atoms and a diamond lattice, wherein .16% of the donor atoms contribute conduction electrons with mobility greater than 770 cm²/Vs to the diamond lattice at 100kPa and 300K.

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ISOTOPICALLY PURE SEMICONDUCTOR MATERIALS

Armington Technologies, LLC

Various semiconductor materials (i.e. silicon, phosphor, germanium, and gallium compounds) used in semiconductor wafer fabrication exhibit heat build up and performance degradation due to the heterogeneous isotopic make up (non-isotopically pure) of these materials. Using silicon as an example, removing the 8% of the material that consists of Si29 and Si30 would render it purely Si28. In general terms, the electron waves would move through this isotopically pure material with less resistance and heat build up.

Value Proposition: This isotopically pure semiconductor portfolio discloses a number of manufacturing approaches including using wafer structures such as a Silicon On Insulator (SOI) sandwich structure that are fabricated by forming isotopically-enriched material on an electrically-insulating material (i.e. silicon dioxide or silicon nitride) on the substrate surface, or trapping hydrogen into a wafer to form a separation layer. In addition, the portfolio also discloses techniques for manufacturing isotopically enriched polysilicon by breaking a silicon halide in the presence of hydrogen ions that are produced from hydrogen gas as well as an application related to luminescent materials.

Priority Date: 07-05-2001

Forward Citing Companies: Canon, NASA, IBM, Panasonic

Representative Claims: US 7,119,400 – Claim 17

A multi-layer semiconductor wafer structure comprising: a silicon substrate composed of silicon having multiple crystal orientations; an insulating layer on said substrate; and a top device layer of semiconducting material on said insulating layer, wherein at least one of the substrate and insulating layer is comprised of isotopically enriched elements of silicon, germanium, or silicon-germanium alloys.

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TECHNOLOGY

SEMICONDUCTORS

NOVELTY

ISOTOPICALLY PURE SEMICONDUCTOR MATERIALS THAT PREVENT THE PROBLEMS ASSOCIATED WITH HEAT BUILD UP

IMPORTANCE

STRATEGIC PORTFOLIO FOR ALL COMPANIES INVOLVED IN THE MANUFACTURING OF COMPUTER CHIPS, SWITCHES, AND OTHER SEMICONDUCTOR DEVICES

NUMBER OF ASSETS

15

US PATENTS (6)

6,653,658
6,838,020
6,867,459
6,926,876
6,979,630
7,119,400

APPLICATIONS (9)

US 10/746,426
US 11/298,440
US 60/303,455
US 60/333,812
US 60/348,939
US 60/402,326
EP 20040811841
PCT/US04/39188
PCT/US04/41344

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